

17EC45

Fourth Semester B.E. Degree Examination, Aug./Sept.2020 **Linear Integrated Circuits** 

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

## Module-1

- Define the following parameters:
  - (i) Input Offset Voltage
  - (ii) CMRR
  - (iii) Slewrate

Mention their typical values for opamp 741.

(06 Marks)

- b. Suggest the circuit for two signal which are received as an input at the same time and output must be taken together. Sketch the circuit. Derive the equation for the output voltage. (Note: Output and Inputs are considered DC voltages). Explain the operation. (08 Marks)
- A non-inverting amplifier is to amplify a 100 mV signal to a level of 3V. Using a (06 Marks) 741 opamp, design a suitable circuit. (Let I<sub>Bmax</sub> = 500 nA).

- What is the significance of a typical gain versus frequency graph for an operational (06 Marks) amplifier? Sketch and explain. (06 Marks)
  - With a neat circuit diagram, explain basic operational amplifier circuit. b.

Which are different biasing methods used for opamp? Explain with neat diagram.

(04 Marks)

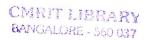
Compare emitter follower and voltage follower.

(04 Marks)

## Module-2

- Explain how the upper cutoff frequency can be set for inverting and non-inverting 3 (06 Marks) amplifiers.
  - b. Design High input impedance capacitor coupled voltage follower using as opamp having lower cutoff frequency of 50 Hz and maximum input bias current of 500 nA. The load resistance is 3.6 k $\Omega$ . If the open loop gain is  $2\times10^{5}$ , find value of input impedance of the (08 Marks)
  - With a neat circuit diagram explain the working of capacitor coupled difference amplifier. (06 Marks) Derive the equation.

- Realize the precision voltage source using opamp and explain. (06 Marks)
  - Draw the circuit diagram of current amplifier using opamp. Explain the circuit operation.
  - With a suitable circuit diagram, explain the operation of instrumentation amplifier consisting of a differential input/output amplifier input stage and a difference amplifier output stage. The circuit has adjustable voltage gain, common mode output nulling and dc output voltage (08 Marks) level shifting.



		$\frac{\text{Module-3}}{\text{Module-3}}$	Sunnly	
5	a.	Design a RC phase-shift oscillator with following specifications: $f_0 = 5 \text{ kHz}$	06 Marks)	
	b.	Explain the operation of an inverting Schmitt trigger circuit with different UTP	08 Marks)	
		levels. Also indicate the input/output characteristics for the circuit.	06 Marks)	
	c.	Explain sample and hold circuit with a neat circuit diagram using opamp.	UU IVIAI KS)	
	OR			
6	a.	Show the realization of logarithmic amplifier using an opamp. Obtain the expression	08 Marks)	
		output voltage.	06 Marks)	
	b.	Write a note on multiplier ic and its applications.	ou marks)	
	c.	With waveforms, explain the working of:	06 Marks)	
		(i) Zero-crossing detector (ii) Voltage-level detector.	UU IVIAI KS)	
	Module-4  Class to have expelled gain of 1 and a pass hand fr			
7	a.	Design a single-stage bandpass filter to have a voltage gain of 1 and a pass b	(06 Marks)	
	b.	Design a second order low pass filter using 741 for a cutoff frequency of 5 kHz.	(08 Marks)	
	c.	Show how a bandstop filter circuit can be constructed using low-pass and high-pa	(06 Marks)	
		Sketch the expected frequency response and explain.	(00 Marks)	
		OD		
		OR		
8	a.	State and explain the following terms for 3 pin IC regulators:		
		(i) Load regulation		
		(ii) Source regulation	(06 Marks)	
		(iii) Drop out voltage. Design an adjustable voltage regulator circuit to get $V_0 = 7.5V$ with load current		
	b.	Design an adjustable voltage regulator circuit to get $\sqrt{0} = 7.5 \text{ with load outline}$	(06 Marks)	
		neing (XII) regulation it., Chych in T.2 mil.	(08 Marks)	
	c.	With a neat schematic, explain the salient features of 723 regulator.	,	
		Module-5		
	9 a. Define capture range, lock-in range and pull-in time. Also specify which range is greater			
9	a.	Define capture range, lock-in range and pun-in time. This specify warms of	(08 Marks)	
		capture range or 'Lock-in range'? Explain about voltage to frequency conversion factor. Which IC can be used to conversion factor.		
	b.	Explain about voltage to frequency conversion factor. Which is the experient for that IC	(06 Marks)	
	par.	factor? Derive the equation for that IC.  What output voltage would be produced by a D/A converter whose output range is		
	c.	What output voltage would be produced by a Biri converse whose supplies a		
		and whose input binary number is		
		(i) 10 (for a 2-bit DAC)		
		(ii) 0110 (for a 4-bit DAC)	(06 Marks)	
		(ii) 0110 (for a 4-bit DAC) (iii) 10111100 (for a 8-bit DAC)  CMRIT LIBRARY  BANGALORE - 560 (137)		
		OR		
		Explain the working of a monostable multivibrator using 555 timer with a neat	functiona	
10	a.	diagram and waveforms. Derive the equations for its pulse width.	(08 Marks)	
	1	The state of a witch type analog phase detector.	(06 Marks)	
	b.	A 555 astable multivibrator has $R_A = 2.2 \text{ k}\Omega$ and $R_B = 6.8 \text{ k}\Omega$ and $C = 0.01 \mu\text{F}$ .	Calculate	
	c.		(06 Marks	
		(i) T <sub>on</sub> (ii) T <sub>off</sub> (iii) Free-running frequency (iv) Duty cycle, D.		