Fifth Semester B.E. Degree Examination, Aug./Sept. 2020 Fundamentals of CMOS VLSI

Time: 3 hrs.

Max. Marks: 100

BANGAROUS Note: Answer FIVE full questions, selecting at least TWO questions from each part.

PART - A

- 1 a. With neat diagram, explain the step by step procedure of fabrication steps of CMOS P-well process and write the mark sequence. (10 Marks)
 - b. Derive the necessary expressions for V_{out} in all the regions of CMOS inverter? Explain.

(10 Marks)

- 2 a. What is body effect? Which parameters are responsible for it? (08 Marks)
 - b. Explain the Pseudo-NMOS logic structure and their salient features with example. (08 Marks)
 - c. Compare CMOS and bipolar technologies. (04 Marks)
- a. Explain the operation of CMOS dynamic logic. Also discuss the cascading problem of dynamic CMOS logic. (10 Marks)
 - b. Implement using CMOS logic structure and its stick diagram:
 - (i) $Z = \overline{A + B + CD}$.
 - (ii) $Z = \overline{A(D+E) + BC}$

(10 Marks)

- 4 a. What are the scaling factors of,
 - (i) Parastic capacitance C_X.
 - (ii) Power dissipation per unit area P_a.

(04 Marks)

(10 Marks)

b. Two nMOS inverters are cascaded to drive capacitive load $C_L = 16C_g$ as shown in Fig. Q4(b). Calculate pair delay V_{in} to V_{out} interms of τ . (06 Marks)

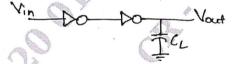


Fig. Q4 (b)

c. Explain with circuit diagram the super buffers with inverting type and non-inverting type of nMOS. (10 Marks)

PART - B

- 5 a. Explain structured design of bus arbitration logic for n-line bus. (10 Marks)
 - b. Discuss the architectural issues to be followed in the design of VLSI subsystems. (10 Marks)
- 6 a. Design a 4:1 multiplexer using nMOS logic and CMOS logic. (10 Marks)
 - b. Explain the implementation of ALU functions with a standard adder. (10 Marks)
- 7 a. How to read or write and hold the bit in SRAM cell? (10 Marks)
 - o. Discuss CMOS pseudo-static memory cell with stick diagram. (10 Marks)
- 8 a. Explain sensitized path based testing for combinational logic. BANGALORE 560 037 (10 Marks)
 - b. Write a note on testability and testing.

* * * * *