CBCS SCHEME

USN | | | | | | | | | | |

15EC53

Fifth Semester B.E. Degree Examination, Aug./Sept. 2020
Verilog HDL

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. What is HDL? Explain typical design flow for designing of VLSI IC circuits and importance of it. **(10 Marks)**

b. Define the following terms with examples :
i) Module ii) Instances iii) Instance name. **(06 Marks)**

OR

2 a. What is stimulus in verilog? Explain components of a simulation with an example of ripple carry counter. **(12 Marks)**

b. Explain trends in HDL's. **(04 Marks)**

Module-2

3 a. Explain the following lexical conventions
i) Whitespace ii) Operators iii) Strings iv) Keywords. **(08 Marks)**

b. Explain the system tasks in verilog with examples. **(08 Marks)**

OR

4 a. What is the module definition in verilog? And explain the components of a verilog module. **(10 Marks)**

b. What are the different ports is verilog? Explain internal and external port connection rules. **(06 Marks)**

Module-3

5 a. Design a 4-to-1 multiplexer using primitives in verilog and draw a logic diagram for it. **(10 Marks)**

b. What are rise, fall and turn-off delays? How they are specified in verilog? **(06 Marks)**

OR

6 a. Discuss the different assignment statements with example in verilog HDL. **(08 Marks)**

b. Explain the following : i) Bitwise operators ii) Concatenation
iii) Conditional operators iv) Replication operators. **(08 Marks)**

Module-4

7 a. Write the difference between blocking and non-blocking statement. **(06 Marks)**

b. Explain the following with proper examples
i) For loop statement ii) Repeat iii) Forever loop **(06 Marks)**

c. What is inferring latch? Explain casex and casez with examples. **(04 Marks)**

OR

8 a. Explain sequential and parallel blocks with examples. **(08 Marks)**

b. Write a verilog program for 4 to 1 mulitplexer using if-else-if conditional statement. **(08 Marks)**

Module-5

9 a. Explain the declaration of constant, veriable and signal in VHDL with example. **(08 Marks)**

b. Explain font convention in VHDL. **(08 Marks)**

OR

10 a. What are the different data types and attributes in VHDL and explain each. **(08 Marks)**

b. Write a VHDL program for 4-bit magnitude comparator. **(08 Marks)**

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