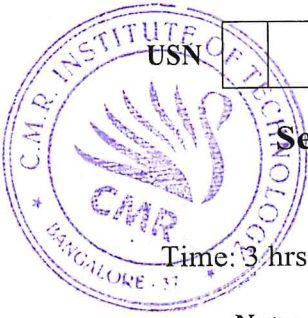


# CBCS SCHEME



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15TE73

**Seventh Semester B.E. Degree Examination, Aug./Sept.2020**

## **CMOS VLSI Design**

Time: 3 hrs.

Max. Marks: 80

*Note: Answer any FIVE full questions, choosing ONE full question from each module.*

### Module-1

- 1 a. State and explain Moore's law. (04 Marks)
- b. List the expressions for  $I_{ds}$  of an ideal MOS transistor for different regions of operation. (03 Marks)
- c. Explain the CMOS inverter DC characteristics highlighting the regions of operation. (09 Marks)

OR

- 2 a. With the help of neat diagrams, explain the cutoff, linear and saturation region channel formation in nMOS transistor with different values of  $V_{gs}$  and  $V_{ds}$ . (08 Marks)
- b. Briefly explain subthreshold condition and geometry dependence with respect to non-ideal I-V effects in MOS transistor with relevant expressions. (08 Marks)

### Module-2

- 3 a. Draw the stick diagrams for :
  - (i) Simple n-well based BiCMOS inverter
  - (ii) Logic function  $\bar{X} = A + B \cdot C$  in nMOS design style. (08 Marks)
- b. Draw and explain in brief the design rules for wires in CMOS ( $\lambda$  based). (08 Marks)

OR

- 4 a. With the help of relevant figures and expressions, briefly explain the rise time and fall-time estimations with respect to CMOS inverter. (08 Marks)
- b. With the help of a neat circuit diagram, explain the working of inverting type nMOS super buffer. (08 Marks)

### Module-3

- 5 a. Draw the scaled nMOS transistor highlighting the scaling factors. (06 Marks)
- b. Derive the scaling factors for the following device parameters:
  - (i) Gate Capacitance (05 Marks)
  - (ii) Maximum Operating Frequency (05 Marks)
- c. What are the problems associated with VLSI design? List the ways to reduce them. (05 Marks)

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OR

- 6 a. Briefly explain the different Bus architectures with necessary figures. (06 Marks)
- b. Implement the ALU functions line EX-OR, EX-NOR, AND and OR operations with an adder. Write the block diagram of 2-bit ALU using adder element. (10 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.  
2. Any revealing of identification, appeal to evaluator and /or equations written eg. 42+8 = 50, will be treated as malpractice.

**Module-4**

- 7 a. With respect to gate restoration logic, draw the circuit diagram and stick diagram of 2-input NAND gate in nMOS and CMOS logic (04 Marks)  
b. Briefly explain Pseudo-nMOS, Dynamic and Clocked CMOS logic. (06 Marks)  
c. Design a parity generator and draw its nMOS stick diagram. (06 Marks)

**OR**

- 8 a. Explain the architecture of FPGA. (08 Marks)  
b. With the help of a neat stick diagram, explain the working of 4:1 multiplexer. (08 Marks)

**Module-5**

- 9 a. Briefly explain the different fault models, observability and controllability with respect to manufacturing test principles. (10 Marks)  
b. List out the System Timing considerations. (06 Marks)

**OR**

- 10 a. Explain the working of three transistor dynamic memory cell along with its circuit diagram and stick diagram. (10 Marks)  
b. Briefly explain the Ad-hoc testing. (06 Marks)

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