CBCS SCHEME

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17ELN15/25

First/Second Semester B.E. Degree Examination, Aug./Sept.2020
Basic Electronics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain pn junction diode operation in both forward and reverse bias conditions with suitable diagrams. **(06 Marks)**

b. With a neat diagram and waveforms, explain the operation of bridge rectifier. **(08 Marks)**

c. Explain Zener diode voltage regulator with no load and with load. **(06 Marks)**

OR

2 a. With a neat circuit diagram, explain the operation of center tapped full wave rectifier. Draw the input and output waveforms. **(07 Marks)**

b. Sketch the transistor input and output characteristics of CE configuration and briefly explain the three regions of operation. Also calculate the value of I_C and β_{dc} for a transistor with $\alpha_{dc} = 0.98$ and $I_B = 120\ \mu A$. **(07 Marks)**

c. What is the need of capacitor filter? Explain the operation of C-filter for half wave rectifier. **(06 Marks)**

Module-2

3 a. Write the procedure for drawing dc load line on the transistor CE output characteristics. **(06 Marks)**

b. Derive an equation for output voltage of a non-inverting op-amp. Find the gain of op-amp if $R_F = 10\ K\Omega$ and $R_1 = 1\ K\Omega$. **(08 Marks)**

c. Design a base bias circuit with a 12V supply that uses a transistor with $h_{fe} = 70$ so that $I_C = 2$ mA and $V_{CE} = 9V$. Assume $R_E = 0$ and $V_{BE} = 0.7$ V. **(06 Marks)**

OR

4 a. With a neat circuit diagram, explain the voltage divider bias circuit using approximate analysis. Given $V_{CC} = 15$ V, $R_C = 2.7\ K\Omega$, $R_E = 2.2\ K\Omega$, $R_1 = 22\ K\Omega$, $R_2 = 12\ K\Omega$, $V_{BE} = 0.7$ V. Calculate V_E, V_C, I_C and V_{CE}. **(09 Marks)**

b. Derive an expression for output voltage of op-amp subtractor. **(07 Marks)**

c. An op-amp has a slew rate of 0.8 V/μsec. What is the maximum amplitude of undistorted sine wave that the op-amp can produce at a frequency of 40 kHz? What is the maximum frequency of the sine wave that op-amp can reproduce if the amplitude is 3V? **(04 Marks)**

Module-3

5 a. Perform the following operations:
(i) $(ABC.E5F)_{16} = (?)_{10}$ (ii) $(100.974)_{10} = (?)_2$ (iii) $(1100111.0101)_2 = (?)_8$ **(06 Marks)**

b. Design and implement full adder using logic gates. **(06 Marks)**

c. Using NOR gates realize NOT gate, OR gate, AND gate and NAND gate. **(08 Marks)**

OR

6 a. State and prove Demorgan's theorem. **(06 Marks)**

b. Subtract: (i) $(11011.11)_2 - (10101.11)_2$ using 1's complement method

(ii) $(10101.11)_2 - (11011.11)_2$ using 2's complement method. **(06 Marks)**

c. Simplify and realize the following Boolean expressions using NAND gates:

(i) $Y_1 = \overline{A}\overline{B}\overline{C} + ABC + \overline{A}BC + A\overline{B}C$ (ii) $Y_2 = (\overline{A} + \overline{B} + \overline{C})(A + \overline{B} + C)$ **(08 Marks)**

Module-4

7 a. Define flip-flop. Explain the operation of RS flip-flop. **(06 Marks)**

b. Explain the architecture of 8051 microcontroller with a neat block diagram. **(08 Marks)**

c. Explain the operation of NAND gate latch. **(06 Marks)**

OR

8 a. Explain the operation of clocked RS flip-flop. **(06 Marks)**

b. Write the features of 8051 microcontroller. **(08 Marks)**

c. With a neat interfacing diagram, explain how stepper motor is interfaced to 8051 microcontroller. **(06 Marks)**

Module-5

9 a. Explain the elements of communication system with the help of neat block diagram. **(06 Marks)**

b. Define modulation. With suitable equations and waveforms, explain frequency modulation. **(08 Marks)**

c. What are passive and active transducers? Explain Seebeck effect and Peltier effect. **(06 Marks)**

OR

10 a. With circuit diagram and waveform, explain the AM detection. **(06 Marks)**

b. A 1 MHz carrier of 1 KW power is amplitude modulated with a message signal of 2 kHz. The depth of modulation is 60%. Determine the total power, sideband frequencies and power in sidebands of the AM wave. **(06 Marks)**

c. Explain the construction and operation of LVDT. **(08 Marks)**

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