CBCS SCHEME

USN | | | | | | | | | |

18EVE/ELD15

First Semester M.Tech. Degree Examination, Aug./Sept. 2020
Digital VLSI Design

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain the MOS system under internal bias with respect to the cross sectional view and energy band diagram. **(10 Marks)**

b. Derive the expression for drain current in linear region and saturation region. **(10 Marks)**

OR

2 a. Derive the general expression of the threshold voltage. **(08 Marks)**

b. Discuss the operation of the Resistive load inverter with circuit diagram and voltage transfer characteristics. Derive the expression for V_{IL} and V_{IH}. **(12 Marks)**

Module-2

3 a. Explain CMOS inverter with reference to operating regions of NMOS and PMOS transistors. Also derive the expression for inverter threshold voltage V_{th}. **(10 Marks)**

b. Explain propagation delay times with reference to input-output voltage waveform of a typical inverter. Derive the expression for the propagation delay time for high-to-law output transition (τ_{PHL}) **(10 Marks)**

OR

4 a. Derive the expression for V_{IL} and V_{IH} of CMOS inverter. **(10 Marks)**

b. Explain switching power dissipation of CMOS inverter. Also derive the expression for average switching power dissipation over one period. **(10 Marks)**

Module-3

5 a. Discuss the operation of Three-Transistor DRAM cell and typical voltage waveforms during four consecutive operations of write "1", read "1", write "0" and read "0". **(12 Marks)**

b. Explain data programming and erasing methods in the flash memory. **(08 Marks)**

OR

6 a. Explain Full CMOS SRAM cell with read and write operations. **(10 Marks)**

b. Discuss 4bit × 4bit NOR based ROM array with necessary diagram. Also draw the layout for the same. **(10 Marks)**

Module-4

7 a. Explain Logic "1" Transfer with respect to pass transistor circuits with necessary derivation. **(08 Marks)**

b. Discus NORA CMOS logic with necessary diagrams. Also explain a pipelined NORA CMOS system. **(12 Marks)**

OR

8 a. Explain three stages of a depletion load NMOS dynamic shift register circuit driven with two phase clocking. **(08 Marks)**

b. Discuss the operation of BiCMOS inverter during transient output pull-up event and pull-down event. **(08 Marks)**

c. Draw the circuit diagram of BiCMOS NAND2 gate. **(04 Marks)**

Module-5

9 a. Explain Human body model, machine model and charged device model for ESD testing. **(10 Marks)**

b. Explain Latch-up with necessary diagrams and equations. Also write guidelines for avoiding latch-up. **(10 Marks)**

OR

10 a. Explain on-chip clock generation and Distribution networks. **(10 Marks)**

b. Explain performance modeling procedure for developing a model. **(10 Marks)**

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