CBCS SCHEME

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18EVE21

Second Semester M.Tech. Degree Examination, Aug./Sept. 2020
Design of Analog and Mixed Mode VLSI Circuit

Time: 3 hrs. Max. Marks: 100

Note: ***Answer FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Derive the expression for output drain current of NMOSFET for all operating regions. **(10 Marks)**

b. What is transconductance? With derivation of equations for gm dram the variations of gm as function of overdrive and drain current. **(07 Marks)**

c. Draw the complete small signal model for NMOSFT. **(03 Marks)**

OR

2 a. With derivation for gain equation, explain the operation of common source amplifier with resistive load. **(08 Marks)**

b. What is the limitation of CS amplifier with resistive load? **(02 Marks)**

c. What is source degeneration resistor? With derivation of gain equation show that the drain current is a linearized function of the input voltage for CS with source degeneration. **(10 Marks)**

Module-2

3 a. Derive the gain equation for CG stage along with its input–output characteristic. **(10 Marks)**

b. Write the circuit for folded cascade amplifier with proper biasing and discuss its input–output characteristics. **(08 Marks)**

c. What are the disadvantages of single stage op-amp? **(02 Marks)**

OR

4 a. State and prove half–circuit concept. **(06 Marks)**

b. Using above derive the expression for small signal differential voltage gain for MOS differential pair. **(04 Marks)**

c. What is Gilbert cell? Derive the Gilbert cell starting from the MOS differential pair, with elaboration on common mode voltage limitation. **(10 Marks)**

Module-3

5 a. What is the effect of channel length modulation in basic current mirror circuit? **(10 Marks)**

b. Explain the large analysis of differential pair with active current mirror. **(10 Marks)**

OR

6 a. Explain various performance parameters of an op-amp. **(07 Marks)**

b. What is the necessary of two stage op-amp, explain with block diagram approach. **(03 Marks)**

c. Write a note on :

i) Telescopic cascade op-amp

ii) Folded cascade op-amp. **(10 Marks)**

Module-4

7 a. In detail explain the slewing in an op-amp circuit. **(10 Marks)**

b. With an example, explain the concept of Delayed – Locked Loops. **(07 Marks)**

c. State two advantage of DLL over PLL. **(03 Marks)**

OR

8 a. With relevant equations explain the dynamics of simple PLL. **(10 Marks)**

b. Write a note on follow in PLL application :
   i) Jitter reduction
   ii) Skew reduction
   iii) Frequency multiplication. **(10 Marks)**

Module-5

9 a. List and explain all specifications of DAC. **(10 Marks)**

b. Explain charge scaling DAC architecture with the help of block diagram. What is its disadvantage are how it is eliminated? **(10 Marks)**

OR

10 a. With neat block diagram and equation explain the operation of single slope ADC architecture. **(10 Marks)**

b. With neat diagram explain the operation of successive approximation ADC with step by step algorithm. **(10 Marks)**

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