CBCS SCHEME

USN | | | | | | | | | | |

18EVE31

Third Semester M.Tech. Degree Examination, Jan./Feb. 2021
CAD of Digital Systems

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain different design domains to describe the VLSI design process. **(08 Marks)**
b. Explain verification methods of checking the correctness of an integrated circuit. **(06 Marks)**
c. Discuss the structural and logic design used in VLSI design. **(06 Marks)**

OR

2 a. Explain the pseudo-code description of Dijkstra's shortest path algorithm. **(06 Marks)**
b. Discuss two types of computational complexity. **(06 Marks)**
c. Explain P, NP and NPC classes of decision problems in the field of complexity theory. **(08 Marks)**

Module-2

3 a. Write a pseudo-code of an algorithm for an exhaustive search by means of back tracking. **(06 Marks)**
b. Write a pseudo-code description of local search. **(06 Marks)**
c. Describe tabu search method with a pseudo-code description. **(08 Marks)**

OR

4 a. Explain pseudo-code description of search by genetic algorithm. **(08 Marks)**
b. Explain minimum-distance design rules on a Lambda Grid. **(06 Marks)**
c. Explain an algorithm which is an alternative to the Liao-Wong algorithm with pseudo-code. **(06 Marks)**

Module-3

5 a. Explain data structures definitions for circuit representation. **(06 Marks)**
b. Explain with neat figures, the types of placement problems. **(06 Marks)**
c. Explain constructive placement approaches using figures. **(08 Marks)**

OR

6 a. Discuss the Kernighan-Lin partitioning algorithm. **(06 Marks)**
b. Explain the various optimization problems related to floor planning. **(06 Marks)**
c. Explain the method for floor plan sizing and formulate the sizing algorithm for slicing floor plans. **(08 Marks)**

Module-4

7 a. Discuss the various parameters which defines the different routing problems. **(06 Marks)**
b. Explain global routing and standard cell layout. **(06 Marks)**
c. Explain channel routing and channel routing models. **(08 Marks)**

OR

8 a. Explain Signal Modeling and Gate Modeling. **(06 Marks)**
b. Write a pseudo-code of a switch-level simulation algorithm. **(06 Marks)**
c. Explain the static and dynamic partitioning of a CMOS network into unidirectional sub-circuits. **(08 Marks)**

Module-5

9 a. Explain ROBDD principles, implementation and construction. **(10 Marks)**
b. Explain two aspects of two level logic synthesis. **(10 Marks)**

OR

10 a. Explain ASAP scheduling with advantages and disadvantages. **(06 Marks)**
b. Explain various sub problems of assignment problem. **(06 Marks)**
c. Explain in detail assignment by clique partitioning. **(08 Marks)**

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