CBCS SCHEME

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18EVE15

First Semester M.Tech. Degree Examination, Jan./Feb. 2021
Digital VLSI Design

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. With an aid of suitable cross sectional view and energy diagrams, explain MOS structure operating in accumulation, depletion and inversion modes under bias voltage. **(10 Marks)**

b. Compare constant electric field and constant power supply voltage scaling. Show analytically by using equations how (i) delay time (ii) power dissipation (iii) power density are affected in terms of scale factor 'S'? **(10 Marks)**

OR

2 a. Assume suitable gradual channel approximations and derive the expression for drain current of MOSFET in (i) Linear (ii) Saturation regions. **(10 Marks)**

b. Consider a MOS system with the following parameters:
$T_{ox} = 200$ A°, $\phi_{GC} = -0.85$ V, $N_A = 2 \times 10^{15}$ cm^3, $Q_{OX} = q \times 2 \times 10^{11}$ C/cm^2 ($q = 1.6 \times 10^{-19}$ C) $n_i = 1.45 \times 10^{10}$, $\epsilon_{ox} = 3.97\ \epsilon_0$ ($\epsilon_0 = 8.85 \times 10^{-14}$), $\epsilon_{si} = 11.7\ \epsilon_0$.
Determine the threshold voltage V_{TO} under zero bias at room temperature (T = 300 K). **(10 Marks)**

Module-2

3 a. With an aid of diagram, discuss a typical CMOS inverter voltage transfer characteristics mentioning the regions of operations and critical input and output voltages. **(10 Marks)**

b. Explain how the three-stage ring oscillator circuit consisting of identical inverters behaves as Astable in digital circuits. Draw typical voltage waveforms. Derive the relation between oscillation period in terms of average propagation delay. **(10 Marks)**

OR

4 a. Define propagation delays and derive the expression for propagation delay time for high-to-low of a CMOS inverter using differential equation method. **(10 Marks)**

b. Derive the expression for the dynamic power consumption of the CMOS inverter. Draw the CMOS inverter circuit used in analysis and typical input and output voltage waveforms and capacitor current waveforms during switching of CMOS inverter. **(10 Marks)**

Module-3

5 a. Describe the operation of three-transistor DRAM cell with pull-up and Read/Write circuitry. Explain with typical waveforms during the operations: Write '1' Read '1' Write '0', Read '0'. **(10 Marks)**

b. Explain the 4 bit × 4 bit 'NOR' based ROM array and 'NAND' based ROM array. Draw necessary circuit diagrams and tabular columns. **(10 Marks)**

OR

6 a. With the aid of circuit topology, explain Read and Write operations of a CMOS SRAM cell. Discuss on its advantages and disadvantages. **(10 Marks)**

b. With the aid of schematic cross-section views of a FLASH memory, explain data programming and Erasing methods. Draw the capacitive coupling circuits of a FLASH memory. **(10 Marks)**

Module-4

7 a. Define Boot voltage strapping. Draw dynamic boot strapping arrangement and explain its principle of operation. Derive the expression to prove that voltage boot strapping can boost the voltage level. **(10 Marks)**

b. Realize the following functions using BiCMOS circuits: (i) $Y = \overline{A \cdot B}$ (ii) $Y = \overline{A(B + C)}$ **(10 Marks)**

OR

8 a. Discuss the charge sharing problem in CMOS circuits. Explain the various techniques used in domino CMOS logic for solving charge sharing problem. **(10 Marks)**

b. Describe the operation of a Bi-CMOS investor transient output pull-up event. Draw necessary circuit and equivalent circuit used for the pull-up delay analysis. **(10 Marks)**

Module-5

9 a. Explain the different models for ESD testing. **(10 Marks)**

b. Describe the following design of manufacturability of integrated circuits:
(i) Factorial design
(ii) Control composite design **(10 Marks)**

OR

10 a. With neat cross-sectional view of CMOS inverter with parasitic bipolar transistor, explain Latch-up problem in CMOS. Mention any five guidelines for avoiding Latch-up. **(10 Marks)**

b. With an aid of diagram, explain the performance modeling procedure. **(10 Marks)**

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