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Seventh Semester B.E. Degree Examination, Jan./Feb.2021
Advanced Computer Architecture

Time: 3 hrs.

Max. Marks: 100

Note: Answer FIVE full questions, selecting at least TWO questions from each part.

PART – A

- 1 a. Define Instruction Set Architecture (ISA). Illustrate the seven dimensions of an ISA. (08 Marks)
- b. State and explain Amdahl's law. Also represent speedup ratio. (05 Marks)
- c. Find the die yield for dies that are 1.5 cm on a side and 1.0 cm on a side, assuming a defect density of 0.4 per cm² and α is 4. (05 Marks)
- d. Define module reliability and availability. (02 Marks)
- 2 a. Define data hazard. Explain how to minimize data hazard stall by forwarding technique. (07 Marks)
- b. List the four schemes used to reduce pipeline branch penalties. Illustrate delayed branch technique in detail. (08 Marks)
- c. List and explain five different ways of classifying exceptions in a computer system. (05 Marks)
- 3 a. Illustrate the basic compiler techniques for exposing instruction level parallelism for the following code :
for (i = 1000; i > 0; i = i - 1)
X[i] = X[i] + S ; (06 Marks)
- b. Explain 2-bit dynamic branch prediction scheme with a state transition diagram. (04 Marks)
- c. With a neat diagram, explain basic structure of a MIPS floating-point unit using Tomasulo's algorithm. Also define various fields of reservation station. (10 Marks)
- 4 a. Explain Branch Target Buffer (BTB), with a neat diagram. Also explain the steps involved in handling an instruction with a BTB. (12 Marks)
- b. Explain in detail, the issues in implementing advanced techniques for speculation. (08 Marks)

PART – B

- 5 a. Explain the different taxonomy of parallel architecture proposed by Flynn. (04 Marks)
- b. With a state transition diagram, explain a write invalidate, Cache Coherence Snooping Protocol for a write-back cache. (10 Marks)
- c. Explain the basic hardware primitives to implement synchronization in multiprocessor architectures. (06 Marks)
- 6 a. Describe the six basic cache optimization techniques. (10 Marks)
- b. Explain in detail the four common questions for the first level of the memory hierarchy. (10 Marks)

- 7 a. List the advanced optimization techniques of cache performance. Also explain in detail, compiler optimizations to reduce miss rate. (10 Marks)
- b. With a block diagram, explain DRAM technology. (05 Marks)
- c. Explain protection via virtual memory. (05 Marks)
- 8 a. Find all the true dependences, output dependences and antidependences and eliminate the output dependences and antidependences by renaming in the following code:
- ```

for (i = 1; i <= 100; i = i + 1) {
 Y[i] = X[i] / C; /*S1*/
 X[i] = X[i] + C; /*S2*/
 Z[i] = Y[i] + C; /*S3*/
 Y[i] = C - Y[i]; /*S4*/
}

```
- (08 Marks)
- b. Explain software pipelining in detail. (08 Marks)
- c. Explain predicated instructions. (04 Marks)

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