CBCS SCHEME

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15CS32

Third Semester B.E. Degree Examination, Jan./Feb. 2021
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain the construction and working of JEFT. **(10 Marks)**

b. Explain the opamp window comparator circuit. **(06 Marks)**

OR

2 a. Explain the working of opamp Schmitt trigger. **(08 Marks)**

b. Explain 555 timer based Astable Multivibrator. **(08 Marks)**

Module-2

3 a. Define hazard. Explain static1 and static 0 hazard. **(06 Marks)**

b. Simplify the Boolean function using Quine-McClusky method:
$Y = F(A, B, C, D) = \Sigma m(2, 3, 7, 9, 11, 13) + d(1, 10, 15)$ **(10 Marks)**

OR

4 a. Write the verilog code for the logic circuit given in Fig.Q4(a) using structural and behavioral models.

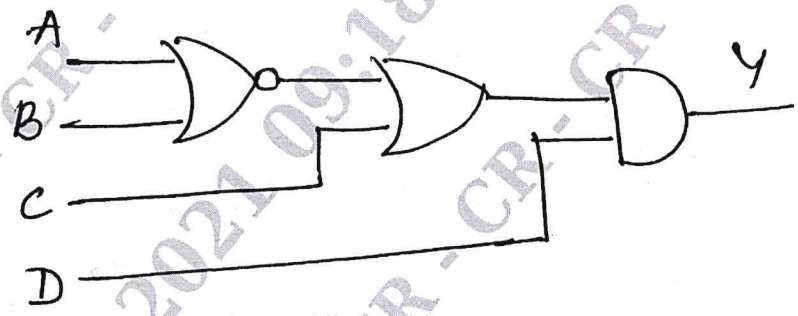

Fig.Q4(a) **(08 Marks)**

b. For the expression given below, use entered variable map technique and simplify the expression. Also draw the logic circuit using basic gates
$f(A, B, C, D) = Y = \Sigma m (1, 5, 10, 11, 12, 13)$ **(08 Marks)**

Module-3

5 a. Define a multiplexer. Analyze a 32:1 multiplexer using 4:1 multiplexers. Give detailed design and connections for the logic circuit. Use one 2:1 MUX. **(10 Marks)**

b. Explain the odd parity checker and generator circuit. **(06 Marks)**

OR

6 a. Implement 7-segment decoder using PLA. **(06 Marks)**

b. Explain n-bit Magnitude Comparator. **(06 Marks)**

c. Write verilog code to implement a 4:1 Multiplxer. **(04 Marks)**

Module-4

7 a. Explain with timing diagram, working of JK Master Slave flip flop. Also give the state transition diagram. **(06 Marks)**

b. Draw the logic diagram for a 4 bit serial-in-serial-out shift register using edge triggered J-K flip flop and explain the circuit with waveform and the truth table. **(10 Marks)**

OR

8 a. Mention two differences between asynchronous and synchronous counter. With a neat block diagram, timing diagram and truth table, explain a 3 bit binary ripple down counter using negative-edge triggered JK flip flop. **(10 Marks)**

b. Explain how a modulus 10 counter can be converted to modulus 8 counter using 7490 IC. **(06 Marks)**

Module-5

9 a. Write the verilog code to implement mod-8 up down counter. **(06 Marks)**

b. Explain the dual slope ADC circuit. **(10 Marks)**

OR

10 a. Explain binary ladder network type DAC. **(08 Marks)**

b. Explain the block diagram of digital clock constructed using counter cascading. **(08 Marks)**

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