USN

15CS34

Third Semester B.E. Degree Examination, Jan./Feb. 2021
Computer Organization

Time: 3 hrs.

Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Explain with a neat diagram, the different functional units of a digital compruter. **(08 Marks)**
   b. Explain the basic operational concepts between the processor and memory, with a neat diagram. **(08 Marks)**

OR

2 a. Explain the following : i) Byte addressability   ii) Big – endian assignment
   iii) Little – endian assignment   iv) Word alignment of a machine. **(08 Marks)**
   b. Registers R_1 and R_2 of a computer contain the decimal value 1200 and 4600, what is the effective address of the source operand in each of the following instruction :
   [R_1, R_2 and R_5 are registers]
   Load   20(R_1) , R_5
   Move # 3000, R_5
   Store R_5, 30(R_1, R_2)
   Add   - (R_2), R_5. **(08 Marks)**

Module-2

3 a. What is Interrupt? With example, explain the concept of interrupts. **(08 Marks)**
   b. What are the different methods of DMA transfer? Explain any one. **(08 Marks)**

OR

4 a. Why is bus arbitration required? Explain with block diagram, bus arbitration using Daisy – Chain. **(08 Marks)**
   b. Explain Serial port and a Serial interface. **(08 Marks)**

Module-3

5 a. Define and explain the following : i) Memory access time   ii) Memory cycle time
   iii) Random Access Memory (RAM)   iv) Read Only Memory (ROM). **(08 Marks)**
   b. Discuss the Internal organization of a 2M × 8 asynchronous DRAM chip. **(08 Marks)**

OR

6 a. Draw a neat block diagram of memory hierarchy in a contemporary computer system. Also indicate relative variation of size, speed and cost per bit, in the hierarchy. **(08 Marks)**
   b. Explain Associative mapping technique and Set Associative mapping technique, with a neat diagram. **(08 Marks)**

Module-4

7 a. Design a 4 – bit binary adder / subtractor and explain its functions. **(08 Marks)**
   b. Explain with diagram, Look – ahead Carry generator. **(08 Marks)**

OR

8 a. Perform Multiplication for (-13) and (+09) using Booth's Algorithm. **(08 Marks)**
b. Perform Multiplication of (+13) and (-6) using Bit Pair recoding method. **(08 Marks)**

Module-5
9 a. With a diagram, explain typical single bus processor data path. **(08 Marks)**
b. Write the control sequence for an unconditional branch instruction. **(08 Marks)**

OR
10 a. Explain the 3 – bus organization of the data path with a neat diagram and write the control sequence for the instruction ADD R_4, R_5, R_6 for the 3 – bus organization. **(08 Marks)**
b. Draw and explain typical hard wired control unit. **(08 Marks)**

* * * * *