USN ☐☐☐☐☐☐☐☐

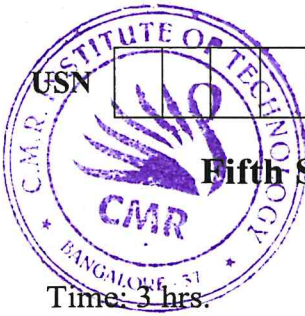### Fifth Semester B.E. Degree Examination, Jan./Feb. 2021
Verilog HDL

Time: 3 hrs.   Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Explain the design flow of VLSI IC circuit steps with a neat flow chart. **(08 Marks)**
   b. List the useful features of verilog HDL for hardware design. **(05 Marks)**
   c. Explain the importance of HDL compared to traditional schematic based design. **(03Marks)**

OR

2 a. Explain TOP-down methodology applying to design of 4 bit Ripple carry counter. **(08 Marks)**
   b. Explain the components of simulation. **(08 Marks)**

Module-2

3 a. Explain any four datatypes in vertilog. **(08 Marks)**
   b. Explain in brief the system task and compiler directives. **(08 Marks)**

OR

4 a. Explain the concept of mapping of ports to external signals with one example. **(08 Marks)**
   b. Declare top level module stimulus. Define REG – IN(4 bit) and CLK(1 bit) as reg register variables and REG – OUT (4 bit) as wire. Instantiate module shift-reg and call it sr1. Write hierarchical names for variables, REG – IN, CLK and REG – OUT. Also write hierarchical name for instance sr1. **(08 Marks)**

Module-3

5 a. Write a design block and stimulus block for 4 : 1 MUX using gate level modeling. **(08 Marks)**
   b. Write a verilog code for function f = (ab + c) with specified delay and also draw neatly the simulated output waveform.(Ref. Fig.Q5(b)).
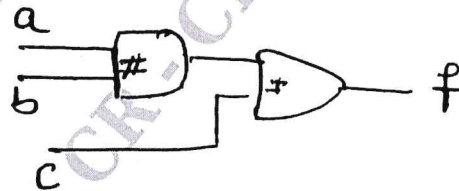

Fig.Q5(b)   **(08 Marks)**

OR

6 a. Explain relational, equality and bitwise operators in verilog with example. **(06 Marks)**
   b. Write data flow modeling for 4 bit FA with carry look ahead. **(10 Marks)**

Module-4

7 a. Describe multiway branching using case, case X, case Z with example. **(09 Marks)**
   b. Write Behavioral modeling for 4 : 1 MUX using case statement. **(07 Marks)**

OR

8	a.	Describe while, for, forever statements in verilog with syntax.	(09 Marks)
	b.	Write behavioral modeling for 4 bit counter program in verilog.	(07 Marks)

Module-5

9	a.	Explain in brief the design process of using VHDL for design synthesis.	(10 Marks)
	b.	Explain the EDA tool flow with neat diagram.	(06 Marks)

OR

10	a.	Discuss the scalar data types used in VHDL.	(08 Marks)
	b.	Write a note on atlributes in VHDL.	(08 Marks)

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