CBCS SCHEME

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15TE73

Seventh Semester B.E. Degree Examination, Jan./Feb.2021
CMOS VLSI Design

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain the DC transfer characteristics of CMOS inverter and mark all the regions of operation with necessary expressions for V_{Out} in each region. **(08 Marks)**

b. Explain with a neat diagram, enhancement mode transistor action of nMOS transistor. **(08 Marks)**

OR

2 a. Using neat diagram, describe fabrication steps for n-MOS transistor. **(08 Marks)**

b. Elaborate the concept of n-well fabrication with neat sketches. **(08 Marks)**

Module-2

3 a. List the colour, stick encoding, mask layout encoding for n-diffusion, P-diffusion polysilicon, metal 1. **(08 Marks)**

b. With the truth table, draw the schematic, stick diagram and physical layout for 2 : 1 mux. **(08 Marks)**

OR

4 a. Describe the delay unit τ in terms of sheet resistance and area capacitance for the CMOS inverter pair shown in Fig. Q4 (a). Calculate the total delay. **(08 Marks)**

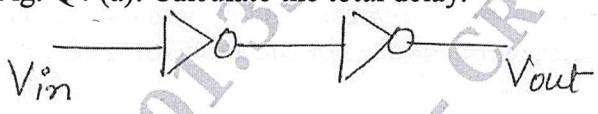

Fig. Q4 (a)

b. Calculate the area of capacitance of a multilayer structure shown in Fig. Q4 (b), if feature size = 5 μm and relative value of metal to substrate = 0.075, polysilicon = 0.1, diffusion = 0.25. **(08 Marks)**

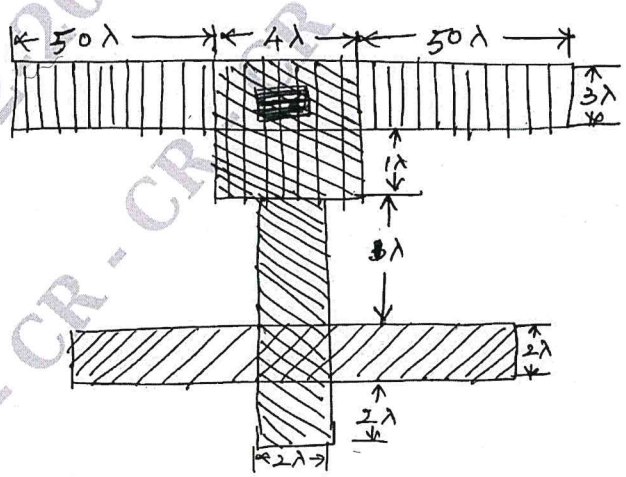

Fig. Q4 (b)

Module-3

5 a. What are the scaling factors for the following device parameters:
(i) Gate capacitance Cg (ii) Max-operating frequency f_0
(iii) Current density (iv) Power dissipation per gate Pg. **(08 Marks)**
b. Discuss general considerations in the design of subsystem design process. **(08 Marks)**

OR

6 a. How to implement arithmetic and logic operation with a standard adder? Explain with the help of logic expression. **(08 Marks)**
b. Explain FPGA architecture using block diagram. **(08 Marks)**

Module-4

7 a. Give the basic concept of parity generator and draw its stick diagram, using n-MOS technology. **(10 Marks)**
b. Obtain the logic implementation of 4-way multiplexer (selector) using nMOS switches with necessary diagrams. **(06 Marks)**

OR

8 a. Discuss the architectural issues to be followed in the design of a VLSI subsystem. **(08 Marks)**
b. Discuss carry look ahead adder with suitable equations and structure design. **(08 Marks)**

Module-5

9 a. Discuss the various system timing considerations. **(04 Marks)**
b. Explain 3 transistor dynamic RAM cell. **(06 Marks)**
c. Draw the schematic of 6 transistor SRAM cell. Discuss read/write operations with appropriate schematic diagrams. **(06 Marks)**

OR

10 a. Mention the types of I/O pads and discuss their functionalities. **(08 Marks)**
b. What are the ground rules for successful design? **(08 Marks)**

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