CBCS SCHEME

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15EE35

Third Semester B.E. Degree Examination, Jan./Feb.2021
Digital System Design

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Define the following terms with an example:
(i) Minterm (ii) Canonical product of sums. **(04 Marks)**

b. Expand $f_1(x,y,z)=\left[x+\overline{xz}(y+\bar{z})\right]$ into minterms and $f_2(a,b,c)=(a+b)(b+c)(\bar{c}+a)$ into maxterms. **(06 Marks)**

c. Simplify the following functions using K-map :
(i) $P=f(a,b,c,d)=\sum m(2,3,4,5,13,15)+\sum d(8,9,10,11)$
(ii) $R=f(a,b,c,d)=\prod M(0,1,2,5,8,9,10)$ **(06 Marks)**

OR

2 a. Find a minimal sum for the following Boolean function using Quine-McCluskey minimization technique
$f(w, x, y, z)=\sum m(2,4,5,9,12,13)$. **(08 Marks)**

b. Simplify the following function using MEV technique and realize the simplified function using basic gates.
$f(a,b,c,d)=\sum m(2,4,5,10,11,14)+\sum d(7,8,9,12,13,15)$
Consider 'd' as a map entered variable. **(08 Marks)**

Module-2

3 a. With the aid of block diagram, clearly distinguish between a decoder and encoder. **(04 Marks)**

b. Implement full adder using 3 : 8 decoder with active low outputs. **(06 Marks)**

c. Design 5 : 32 line decoder using one 2 : 4 and four 3 : 8 decoders which has the active low enable inputs and active low outputs. Explain the operation. **(06 Marks)**

OR

4 a. Implement $f(a,b,c,d)=\sum m(0,1,5,6,7,9,10,15)$ using
(i) 16 : 1 MUX with a, b, c and d as select lines.
(ii) 8 : 1 MUX with b, c and d as select lines.
(iii) 4 : 1 MUX with c and d as select lines **(08 Marks)**

b. Design two bit binary comparator and implement with suitable logic gates. **(08 Marks)**

Module-3

5 a. Explain the operation of gated SR latch with a logic diagram, logic symbol and truth table. **(08 Marks)**

b. Explain the working of a master-slave JK flip-flop with the help of logic diagram function table, logic symbol and timing diagram. **(08 Marks)**

OR

6 a. Differentiate between synchronous counter and asynchronous counter. **(04 Marks)**
b. Derive the characteristic equation of D and T flip flop. **(04 Marks)**
c. Explain 4-bit universal shift register with the help of logic diagram, mode control table. **(08 Marks)**

Module-4

7 a. Explain the Mealy model of a sequential circuit. **(06 Marks)**
b. A sequential circuit has one input and one output. The state diagram as shown in Fig. Q7 (b). Design the sequential circuit with J-K flip-flop. **(10 Marks)**

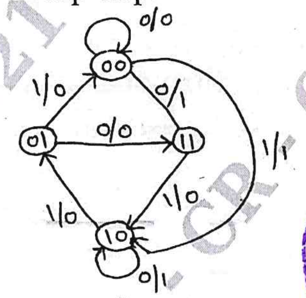

Fig. Q7 (b)

OR

8 a. Explain the Moore model of sequential circuit. **(06 Marks)**
b. Design a synchronous counter using J-K flip-flops to count the sequence, 0, 1, 2, 4, 5, 6, 0, 1, 2,….. Use state diagram and state table. **(10 Marks)**

Module-5

9 a. Mention the types of HDL descriptions. Explain data flow and behavioural descriptions with an example. **(10 Marks)**
b. Differentiate the VHDL and verilog. **(06 Marks)**

OR

10 a. Explain the following :
(i) Signal declaration and assignment statements.
(ii) Concurrent signal assignment statements.
(iii) Constant declaration and assignment statements. **(12 Marks)**
b. Explain the vector data type with an example. **(04 Marks)**

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