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## Seventh Semester B.E. Degree Examination, Jan./Feb.2021 Advanced Computer Architectures

Time: 3 hrs.

Max. Marks: 100

**Note: Answer any FIVE full questions, choosing ONE full question from each module.**

### Module-1

1. a. With the help of block diagrams, explain Flynn's classification of computer architectures. (10 Marks)
- b. Describe the shared-memory multiprocessor models. (10 Marks)

OR

2. a. Define the types of data dependence. Also compute the dependence graph for the following code segment: (10 Marks)  
 $S_1$ : Load R1, A  
 $S_2$ : Add R2, R1  
 $S_3$ : Move R1, R3  
 $S_4$ : Store B, R1
- b. Explain the characteristics of the following static connection networks : (10 Marks)  
 (i) Linear array.      (ii) Ring.      (iii) Binary tree.      (iv) Mesh.

### Module-2

3. a. Distinguish between RISC and CISC processor architectures, with block diagrams. (10 Marks)
  - b. Explain VLIW processor architecture and its pipeline operations. (10 Marks)
- OR
4. a. Compare the two virtual memory models for multiprocessor systems. (10 Marks)
  - b. Illustrate four level memory hierarchy. (04 Marks)
  - c. Define the various page replacement policies. (06 Marks)

### Module-3

5. a. Illustrate daisy-chained and distributed arbitration techniques. (10 Marks)
- b. List the various Cache mapping schemes. Also explain any two schemes. (10 Marks)

OR

6. a. Consider the following pipeline reservation table:

		Time →						
		1	2	3	4	5	6	7
Stages	$S_1$	X						X
	$S_2$		X		X			
	$S_3$			X		X		

- (i) What are the forbidden latencies? (10 Marks)
  - (ii) What is the initial collision vector? (06 Marks)
  - (iii) Draw the state transition diagram (04 Marks)
  - (iv) List all the simple cycles.
  - (v) List all the greedy cycles.
  - (vi) Determine the minimal average Latency.
- b. Explain the usage of prefetch buffers in instruction pipelining. (06 Marks)
  - c. Illustrate internal data forwarding technique. (04 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.  
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

**Module-4**

- 7 a. Define the two approaches of snoopy bus cache coherence protocol. Also write the state transition graphs for write through and write back cache. (10 Marks)
- b. Explain in detail, three types of cache directory protocols. (10 Marks)

OR

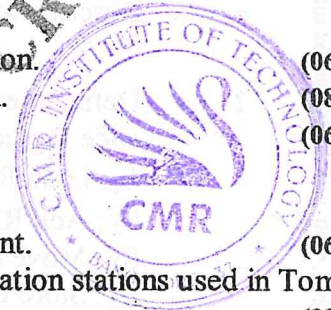
- 8 a. Explain the flow control methods for resolving a collision between two packets requesting the same outgoing channel. (10 Marks)
- b. Distinguish between store-and-forward routing and wormhole routing schemes. (04 Marks)
- c. Define the various vector instruction types. (06 Marks)

**Module-5**

- 9 a. Explain the mechanisms used for interprocess communication. (06 Marks)
- b. Describe the compilation phases in parallel code generation. (08 Marks)
- c. Explain the sole-access protocols used in synchronization. (06 Marks)

OR

- 10 a. Explain the concept of recorder buffer as a processor element. (06 Marks)
- b. With the help of a block diagram, explain the role of reservation stations used in Tomasulo's algorithm. (08 Marks)
- c. Write and explain state transition diagram of 2 bit branch predictor. (06 Marks)



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