

CBCS SCHEME

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17TE73

Seventh Semester B.E. Degree Examination, Jan./Feb. 2021

CMOS VLSI Design

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- Derive the expression for current in Cutoff, Linear and Saturation region for nMOS Transistor with neat diagram. (10 Marks)
 - Describe with a neat sketch the CMOS P well process steps to fabricate a CMOS inverter. (10 Marks)

OR

- Compare Cmos and bipolar Technologies. (06 Marks)
 - Discuss : i) Velocity saturation. (08 Marks)
ii) Mobility degradation effect due to increase in saturation current. (06 Marks)
 - Demonstrate the operation of Noise margin with neat diagram. (06 Marks)

Module-2

- Discuss the λ – based design rules for i) nMOS encoding ii) Butting contact. (10 Marks)
 - Draw the Stick Diagram and Layout for the CMOS implementation of the two input NAND gate. (10 Marks)

OR

- Estimate the rise time and fall time for a CMOS Inverter. (08 Marks)
 - Derive the expression for delay interms of τ for CMOS Inverter pair. (06 Marks)
 - Define Sheet Resistance 'Rs' and the standard unit or Capacitance \square Cg. (06 Marks)

Module-3

- Determine the scaling factors for the following :
i) Gate Area (A_g) ii) Parasitic Capacitance (C_x)
iii) Maximum Operating frequency (f_0) iv) Power dissipation per gate (P_g)
v) Power Speed product (P_T). (10 Marks)
 - Explain Carry Look Ahead Adder (CLA) and represent the 4 bit block CLA unit. (10 Marks)

OR

- What are the observations that has to be kept in mind during the design process of VLSI? Define Regularity. Find the regularity for 4-bit and 8-bit barrel shifter. (10 Marks)
 - Explain with neat diagram and equations : i) The Manchester Carry Chain (10 Marks)
ii) Carry select adders.

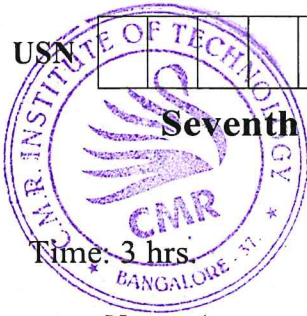
Module-4

- Explain Parity Generator with necessary equations and also draw the stick diagram for nMOS and CMOS blocks. (10 Marks)
 - With a neat diagram, explain the Architecture of FPGA. (10 Marks)

OR

1 of 2

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.



- 8 a. Explain with neat diagram : i) Dynamic CMOS logic ii) CMOS Domino logic. (10 Marks)
b. Explain Switch logic of a 4 – way multiplexer for nMOS switches. (04 Marks)
c. Explain in detail the goals and techniques of FPGA. (06 Marks)

Module-5

- 9 a. Explain Pseudo – Static RAM/register cell with neat diagram. Also comment on the Area, Dissipation and its Volatility. (10 Marks)
b. Discuss the following : (10 Marks)
i) BIST ii) Adhoc Testing.

OR

- 10 a. Write a note on :
i) Stuck – at faults and ii) Open and short circuit Faults. (06 Marks)
b. What are the Timing consideration requirements in system design? (06 Marks)
c. Explain the working of a three transistor dynamic RAM cell and draw the layout with respect to nMOS structure. (08 Marks)