CBCS SCHEME

USN | | | | | | | | | | |

15EC33

Third Semester B.E. Degree Examination, Jan./Feb. 2021
Digital Electronics

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Write the following equation in proper canonical form:

i) $P = f(a,b,c) = a\bar{b} + \bar{a}b + bc$

ii) $T = f(a,b,c) = (a + \bar{b}).(\bar{b} + c)$ **(06 Marks)**

b. Find all the prime-implicant and essential prime implicant for the given function.

i) $D = f(a, b, c, d) = \sum_m(6, 7, 9, 10, 13) + \sum_d(1, 4, 5, 11, 15)$ using K-map and draw the logic diagram.

ii) $P = \pi_m(0, 1, 2, 3, 7, 8, 10, 11, 15).\ \pi_d(9, 14)$ using K-map and draw the logic diagram. **(10 Marks)**

OR

2 a. Simplify the following three-variable equation using K-map. List all the prime-implicant and essential prime implicants. $J = F(x, y, z) = \sum(0, 2, 3, 4, 5, 7)$ **(04 Marks)**

b. Find all the prime implicant and essential prime implicant of the function $S = f(a, b, c, d) = \sum(1, 3, 13, 15) + \sum_d(8, 9, 10, 11)$ using Quine-McClusky's algorithm. Draw the logic diagram. **(12 Marks)**

Module-2

3 a. Implement the following multiple output function using 74LS138 3:8 decoder and external gates

$F_1(A, B, C) = \sum_m(1, 4, 5, 7)$

$F_2(A, B, C) = \pi_m(2, 3, 6, 7)$ **(06 Marks)**

b. What do you mean by priority encoder? Explain 8 to 3 encoder, with highest number having the highest priority with the help of a truth table. (No need of logic circuit). **(06 Marks)**

c. Design a 1-bit comparator using logic gates. **(04 Marks)**

OR

4 a. Implement full-Adder using 4:1 Multiplexer. **(06 Marks)**

b. Design a 4-bit ripple parallel adder using full adder-blocks. **(05 Marks)**

c. Design a full-subtractor using logic gates. **(05 Marks)**

Module-3

5 a. Explain the working of switch debouncer using SR latch. **(06 Marks)**

b. Obtain the characteristic equation of i)SR flip-flops ii) JK flip-flops. **(04 Marks)**

c. Explain clocked SR flip-flop using NAND gates. **(06 Marks)**

OR

6 a. Explain the working of Master-Slave JK flip-flop with functional table and timing diagram. Show how race around condition is overcome. **(12 Marks)**

b. What is meant by triggering of flip-flops? Name the different triggering methods. **(04 Marks)**

Module-4

7 a. Explain the different types of shift register SISO, PISO, SIPO, PIPO with relevant circuit diagram. **(10 Marks)**

b. Design 4-bit asynchronous down counter and explain, using negative edge triggered JK flip flops. **(06 Marks)**

OR

8 a. Design synchronous MOD-8 counter using clocked JK flip-flops. **(08 Marks)**

b. Design synchronous MOD-6 counter using clocked T-flip-flops. **(08 Marks)**

Module-5

9 a. Explain the Mealy model and Moore model of a clocked synchronous sequential network. **(08 Marks)**

b. Design a clocked sequential circuit that operates according to the state diagram shown in Fig.9(b). Implement the circuit using D-flip-flop. **(08 Marks)**

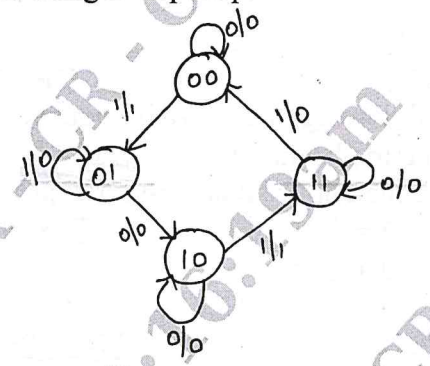

Fig.9(b)

OR

10 a. Give recommended steps for the design of a clocked synchronous sequential networks. **(06 Marks)**

b. Design a synchronous counter using JK flip-flops to count the sequence 0, 1, 2, 4, 5, 6, 0, 1, 2. Use state diagram and state table. **(10 Marks)**

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