CBCS SCHEME

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Sixth Semester B.E. Degree Examination, Jan./Feb. 2021
VLSI Design

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Explain the nmos enhancement mode transistor operation for different values of V_{GS} and V_{DS}. **(06 Marks)**

b. Obtain the transfer characteristics of a CMOS inverter mark all the region, showing the status of PMOS and nmos transistor. **(10 Marks)**

OR

2 a. Explain the fabrication steps of CMOS P-well process with neat diagram, and write all the mask sequence. **(10 Marks)**

b. Distinguish between CMOS and bipolar technologies **(06 Marks)**

Module-2

3 a. With neat diagram, describe the design rules i) Transistor ii) wires iii) contact cut. **(08 Marks)**

b. Draw the Schematic and Mask Layout for the expression $Y = \overline{AB + CD}$. **(08 Marks)**

OR

4 a. Derive the expression for the Rise time and fall time for CMOS inverter. **(10 Marks)**

b. Two MOS inverters are cascaded to drive a capacitive load C_L = 14cg as shown in Fig Q4(b). Calculate the pair delays V_{in} to V_{out} in terms of τ.

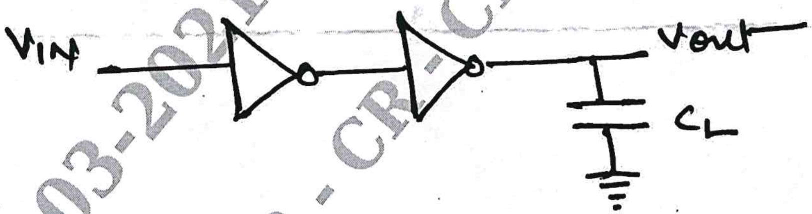

Fig Q4(b) **(06 Marks)**

Module-3

5 a. Why do we require scaling of MOS circuits? **(04 Marks)**

b. Find the scaling factors for the following :

i) Gate capacitance (C_g) ii) Saturation current (I_{ds})
iii) Gate capacitance per unit area (C_{ox}) iv) Carrier density in channel (Q_{ON})
v) Maximum frequency of operation (f_0) vi) Speed power product (P_T) **(12 Marks)**

OR

6 a. Discuss the General considerations of the subsystem Design process. **(06 Marks)**
b. Explain a standard Adder element using nmos version of adder logic. **(10 Marks)**

Module-4

7 a. Explain the multiplexer/Data selections with layout. **(10 Marks)**
b. Explain parity Generator with stick diagram. **(06 Marks)**

OR

8 a. Briefly explain Architecture of FPGA. **(10 Marks)**
b. Explain Antifuse base FPGA. **(06 Marks)**

Module-5

9 a. Explain one transistor DRAM. **(08 Marks)**
b. Explain Three Transistors DRAM. **(08 Marks)**

OR

10 a. Explain objectives of Functional Testing. **(06 Marks)**
b. Define fault model, explain the
i) Stuck – at Faults
ii) Stuck – open and stuck – short Fault
iii) Stuck – open Fault **(10 Marks)**

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