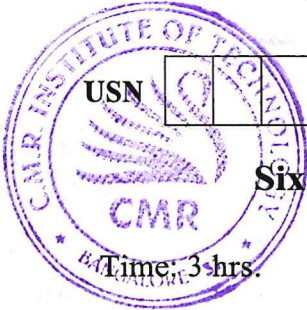


# CBCS SCHEME



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15EC663

Sixth Semester B.E. Degree Examination, Jan./Feb.2021

## Digital System Design Using Verilog

Time: 3 hrs.

Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

### Module-1

- 1 a. Construct with neat diagram, the simple design methodology and describe functions. (08 Marks)
- b. Compute a design methodology for Hardware or Software codesign used in embedded system. (08 Marks)

OR

- 2 a. Construct and write verilog code for the Burglar alarm to be a priority Encoder, with zone 1 having highest priority, down to zone 8 having lowest priority, using truth table. (08 Marks)
- b. Develop Data Path and Verilog model of the complex multiplier. (08 Marks)

### Module-2

- 3 a. Design 64K\*8 bit composite memory using four 16K\*8 bit components. (08 Marks)
- b. Describe all types of ROM. (08 Marks)

OR

- 4 a. Explain ECC code and compute whether there is an error in the ECC word 000111000100, if so, correct it. (08 Marks)
- b. Design and develop a verilog model of 7-segment decoder with blanking input using ROM. (08 Marks)

### Module-3

- 5 a. With neat diagram, describe the Application Specific Integrated Circuits (ASICs). (06 Marks)
- b. Compute design of Programmable Array Logic (PAL). (10 Marks)

OR

- 6 a. Compute the design of Field Programmable Gate Arrays (FPGA). (10 Marks)
- b. Design a priority encoder has 16 inputs I[0:15]; four-bit encoded output Z[3:0]; & a valid output is 1, when any input I[0] has the highest priority and I[15]. The lowest priority. Express in verilog. (06 Marks)

### Module-4

- 7 a. Describe all parallel buses used in digital circuits I/O devices. (08 Marks)
- b. Describe all serial interface standard for connecting I/O devices. (08 Marks)

OR

- 8 a. Describe all types of interrupts used in I/O interfacing. (08 Marks)
- b. Design an I/P controller that has 8-bit binary coded input from a sensor. The value can be read from an 8-bit input register. The controller should interrupt the embedded Gumnut core when the input value change. The controller is the only interrupt source in the system and design a verilog model of the input controller. (08 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.  
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

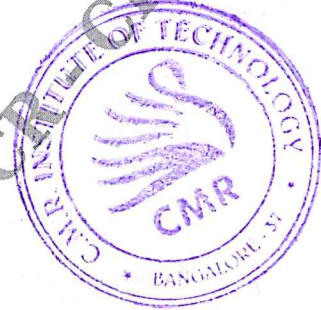
Module-5

- 9 a. Describe area and time optimization used in design optimization. (08 Marks)
- b. Describe scan design and boundary system. (08 Marks)

OR

- 10 a. Describe Built-In Self Test (BIST) using in Design methodology. (08 Marks)
- b. Describe physical Design using in design flow. (08 Marks)

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