CBCS SCHEME

USN | | | | | | | | | | |

17EE35

Third Semester B.E. Degree Examination, Jan./Feb. 2021
Digital System Design

Time: 3 hrs. Max. Marks: 100

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Define the following terms with example :
i) Literal ii) Maxterm iii) Sumterm iii) Product of sum v) Canonical sum of products. **(05 Marks)**

b. Reduce the following function using K-map technique and implement using NAND gates only i) $f_1 (P, Q, R, S) = \sum m (0, 1, 4, 7, 8, 9, 10) + d (2, 11)$
ii) $f_2 (A, B, C, D) = \pi (0, 2, 4, 10, 11, 14, 15)$ **(10 Marks)**

c. Reduce the following function using K-map and implement using NOR gate only
$f_3 (A, B, C, D) = \sum m (0, 5, 7, 8, 10, 13) + d (2, 4, 14, 15)$ **(05 Marks)**

OR

2 Reduce the following function using Quine - McClusky method and shall all the tables including Reduced prime implicant table
$Q_1 = f (a, b, c, d, e) = \sum (1, 3, 4, 5, 6, 7, 10, 11, 12, 13, 14, 15, 18, 19, 20, 21, 22, 23, 26, 27)$ **(20 Marks)**

Module-2

3 a. Implement the following multiple output function using single 74LS138 (3 to 8 decoder) and external gates.
$F_1 (A, B, C) = \overline{A}B + AB\overline{C} + AC$
$F_2 (A, B, C) = \pi M (2, 3, 6, 7)$ **(04 Marks)**

b. Implement the following function
i) $f_1 (A, B, C, D) = \sum m (0, 2, 6, 10, 11, 12, 13) + d (3, 8, 14)$ using 74LS151 (8:1 MUX) considering Lower order inputs as select inputs.
ii) $f_2 (A, B, C, D) = \sum m (0, 2, 3, 4, 6, 7, 9, 11, 13, 15)$ using 74LS153 (4:1MUX) considering higher order inputs as select inputs. **(08 Marks)**

c. Develop the following combinational logic
i) Construct full subtracter using 74LS153
ii) Construct 4 to 16 decoder using 2 to 4 decoders only. **(08 Marks)**

OR

4 a. Draw the full Adder ckt from truth table. Construct a four bit adder and explain it. **(06 Marks)**

b. Draw a 1 bit comparator and explain. **(04 Marks)**

c. Develop a look ahead carry adder from full adder. Draw the compute structure including look ahead carry generator and final Adder. **(10 Marks)**

Module-3

5 a. Analyze the application of SRFF as switch debouncer with waveforms. **(04 Marks)**

b. Explain the working principles of gated SR latch with truth table next state table, excitation table and characteristic equation. **(08 Marks)**

c. Draw the Master – Slave JK flip-flop and explain its working. Draw the truth table, what is race around condition? How it can overcome? **(08 Marks)**

OR

6 a. Draw and explain universal shift Registers. **(12 Marks)**
b. Design and draw Mod 6 Asynchronous counter. **(08 Marks)**

Module-4

7 a. Construct the sequential logic circuit of following state diagram using JKFF. Clearly show the state table, transition table, excitation table, expression and sequential logic diagrams.

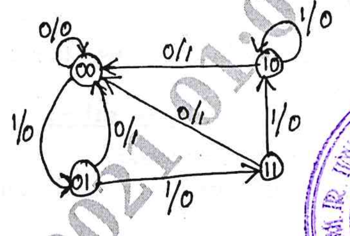

Fig Q7(a) **(10 Marks)**

b. Analyze the sequential circuit below :
   i) Derive the state table
   ii) Sketch the transition state diagram
   iii) Describe in words the functionality of the circuit

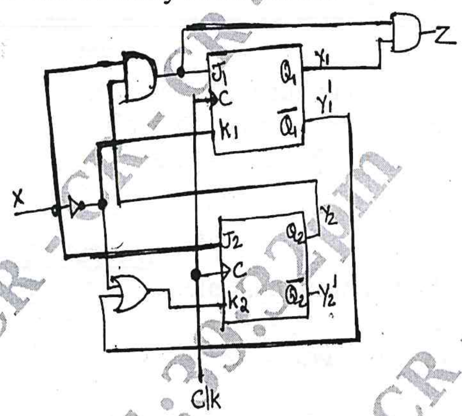

Fig Q7(b) **(10 Marks)**

OR

8 a. Design Mod 4 synchronous up down counter using JKFF. **(10 Marks)**
b. Design a synchronous counter that counts the following sequence

0-2-4-6-0

(10 Marks)

Module-5

9 a. What are the different VHDL Descriptions? **(05 Marks)**
b. Write the VHDL program for Half Adder in
   i) Behavioral Descriptions
   ii) Structural Descriptions
   iii) Dataflow Descriptions **(15 Marks)**

OR

10 a. Explain the structure of Data-flow Descriptions. **(07 Marks)**
b. What are the different operators and data types in VHDL? **(08 Marks)**
c. Compare VHDL and Verilog. **(05 Marks)**

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