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Internal Assessment Test 2 – November 2020

Sub:	Analog and Digital Electronics					Sub Code:	18CS33	Branch:	ISE	
Date:	02.11.2020	Duration:	90 mins	Max Marks:	50	Sem/Sec:	3 – A, B, C		OBE	

Answer **any FIVE FULL** Questions

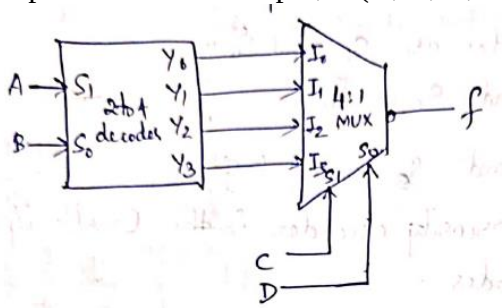
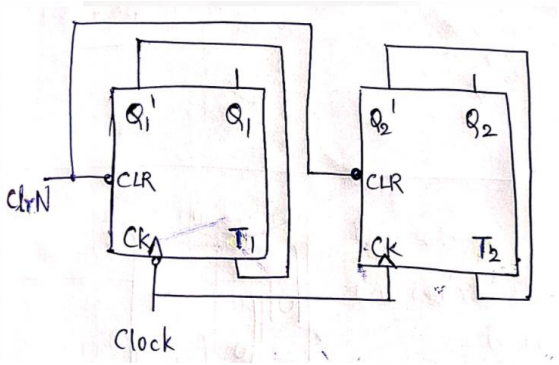
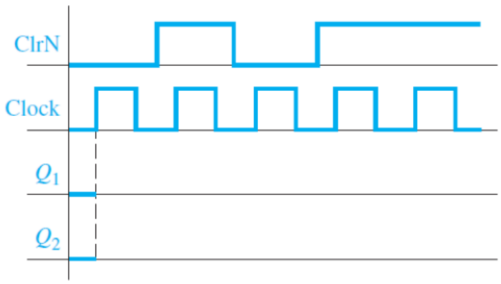
		MARKS	CO	RBT
1	(a) Find any two minimum AND-OR circuits for the given function F: $F(A, B, C, D) = \sum m (0, 2, 5, 6, 7, 8, 9, 12, 13, 15)$ Identify two hazards in each of the circuits. Also find AND-OR circuits for the same that has no hazards. (b) Find a minimum OR-AND circuit for the function G given below: $G(A, B, C, D) = \Pi M (2, 5, 6, 7, 8, 9, 12, 13, 15)$ Identify the hazard, and also find an OR-AND circuit for G that has no hazards.	[5+5]	CO4	L3
2	(a) Implement a full subtracter using two 4:1 MUXes and one inverter. Use B_{in} and Y as control inputs of the MUXes and connect 1's, 0's, X or X' to each data input. (b) Implement an 8:1 MUX using two 4:1 MUXes, two 3-state buffers and one inverter.	[5+5]	CO4	L3
3	(a) Implement an 8 to 3 priority encoder using two 4 to 2 priority encoders and any additional necessary gates. (b) The circuit below has a 2 to 4 decoder with active high outputs connected to a 4:1 MUX with an active low output. Derive a minimum SOP expression for the output, F (A, B, C, D). 	[5+5]	CO4	L4
4	Implement the following functions using a 4x5x4 PLA: $F1(a, b, c, d) = \sum m(1, 2, 4, 5, 6, 8, 10, 12, 14)$ $F2(a, b, c, d) = \sum m(2, 4, 6, 8, 10, 11, 12, 14, 15)$	10	CO4	L3
5	(a) With necessary diagrams and proper explanation, derive the truth table, state transition diagram, characteristic equation and excitation	[5+5]	CO4	L3

	table for a JK flip-flop. (b) Complete the timing diagram for the following circuit.   			
6	(a) Explain the working of an SR latch using NAND gate. (b) Explain in detail, how an SR latch can be used to eliminate the switch contact bounce.	[5+5]	CO4	L2

Scheme of Evaluation

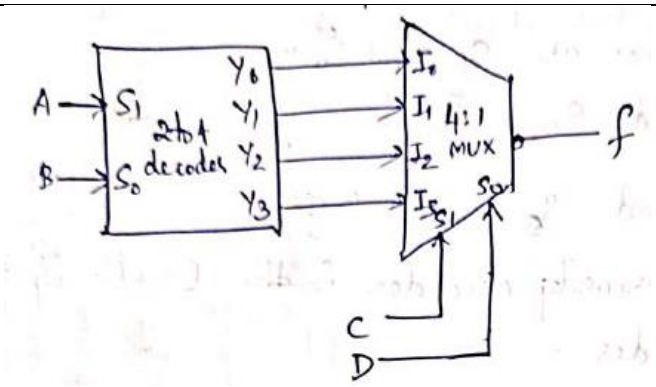
Internal Assessment Test 2 – Nov 2020

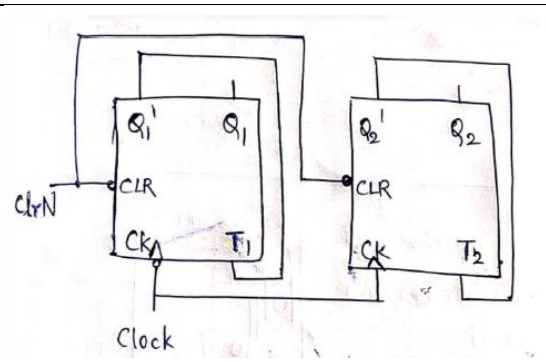
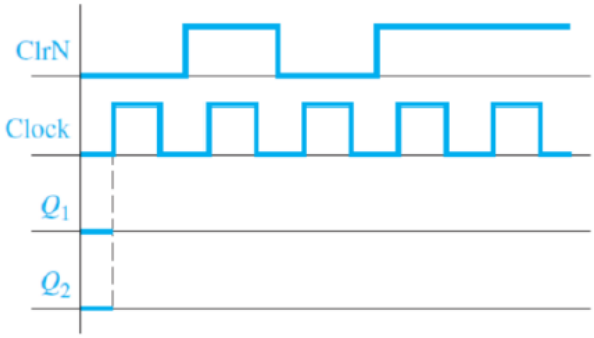
Sub:	Analog and Digital Electronics							**Code:**	18CS33
Date**:**	02.11.2020	Duration:	90mins	Max Marks:	50	**Sem:**	III	**Branch:**	ISE

Note: Answer Any Five Questions

Question #	**Description**	**Marks Distribution**	**Max Marks**
1	(a) Find any two minimum AND-OR circuits for the given function F: F (A, B, C, D) = Σ m (0, 2, 5, 6, 7, 8, 9, 12, 13, 15) Identify two hazards in each of the circuits. Also find AND-OR circuits for the same that has no hazards. • Plot a K-Map for the function F, putting 1's in place of the minterms given. • Find any 2 minimum solutions for F in the SOP form. • Draw AND-OR circuits for the minimum solutions. • Locate 2 hazards each in the 2 solutions & find the product terms corresponding to the hazards. • Redraw the AND-OR circuits including the hazard terms. (b) Find a minimum OR-AND circuit for the function G given below: G (A, B, C, D) = Π M (2, 5, 6, 7, 8, 9, 12, 13, 15) Identify the hazard, and also find an OR-AND circuit for G that has no hazards. • Plot a K-Map for the function G putting 0's in place of the maxterms given. • Find a minimum solution for G in the POS form. • Draw an OR-AND circuit for the minimum solution.	[5+5]	10

	• Locate 1 hazard each in the solution & find the sum term corresponding to the hazard. • Redraw the OR-AND circuit including the hazard term.		
2	(a) Implement a full subtracter using two 4:1 MUXes and one inverter. Use B_{in} and Y as control inputs of the MUXes and connect 1's, 0's, X or X' to each data input. • Obtain the truth table for a full subtracter with inputs X, Y and B_{in}. • Obtain the expressions for Difference and Borrow. • Show the implementation of the full subtracter using two 4:1 MUXes where B_{in} and Y are connected as select lines to both the MUXes. • Express Difference and Borrow in terms of input X through the connections. (b) Implement an 8:1 MUX using two 4:1 MUXes, two 3-state buffers and one inverter. • Show the implementation with necessary explanation detailing the working of this specific type of implementation.	[5+5]	10
3	(a) Implement an 8 to 3 priority encoder using two 4 to 2 priority encoders and any additional necessary gates. • Show the implementation with necessary explanation detailing the working of this specific type of implementation. (b) The circuit below has a 2 to 4 decoder with active high outputs connected to a 4:1 MUX with an active low output. Derive a minimum SOP expression for the output, F (A, B, C, D).	[5+5]	10

	 • Obtain expressions for decoder outputs Y_0, Y_1, Y_2 & Y_3. • Using truth table and K-Map, derive an SOP expression for the output of the MUX, f.		
4	Implement the following functions using a 4x5x4 PLA: $F_1(a, b, c, d) = \Sigma m (1, 2, 4, 5, 6, 8, 10, 12, 14)$ $F_2(a, b, c, d) = \Sigma m (2, 4, 6, 8, 10, 11, 12, 14, 15)$ • Represent the given functions in a truth table. • Using K-Maps, obtain minimum solutions for F_1 & F_2 with common terms between them. • Obtain the PLA program table • Show the implementation of functions using a 4x5x4 PLA.	[2+3+2+3]	10
5	(a) With necessary diagrams and proper explanation, derive the truth table, state transition diagram, characteristic equation and excitation table for a JK flip-flop. • Give the truth table, state transition diagram, characteristic equation and excitation table for a JK flip-flop with necessary diagrams and explanation. (b) Complete the timing diagram for the following circuit.	[5+5]	10

	  • Using the truth table of a T flip-flop and considering the active edges of the clock for each flip-flop, complete the timing diagram. Also consider the ClrN input given to the flip-flops.		
6	(a) Explain the working of an SR latch using NAND gate. • Explain each input combination for an SR latch with a diagrammatic representation using truth table of NAND gate. • Obtain the truth table for the SR latch. (b) Explain in detail, how an SR latch can be used to eliminate the switch contact bounce. • Explain the contact bounce issue with diagrams • Explain how SR latch can be used to overcome the same, with diagrams.	[5+5]	10

1a. Find any two minimum AND-OR circuits for the given function F:

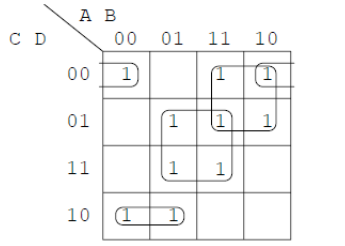
F (A, B, C, D) = Σ m (0, 2, 5, 6, 7, 8, 9, 12, 13, 15)

Identify two hazards in each of the circuits. Also find AND-OR circuits for the same that has no hazards.

Answer:

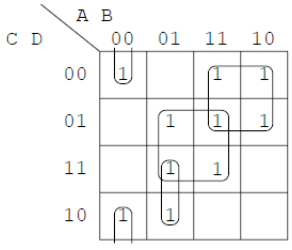
$F(A, B, C, D) = \sum m(0, 2, 5, 6, 7, 8, 9, 12, 13, 15)$

There are 3 different minimum AND-OR solutions to this problem. The problem asks for any two of these.



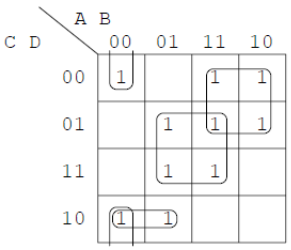
F = B D + A C' + A'C D' + B'C'D'

Solution 1: 1-hazards are between 0000↔0010 and 0111↔0110



F = B D + A C' + A'B'D' + A'B C

Solution 2: 1-hazards are between 0010↔0110 and 0000↔1000



F = B D + A C' + A'B'D' + A'C D'

Solution 3: 1-hazards are between 0111↔0110 and 0000↔1000

Without hazards:

$F^t = BD + AC' + B'C'D' + A'CD' + A'B'D' + A'BC$

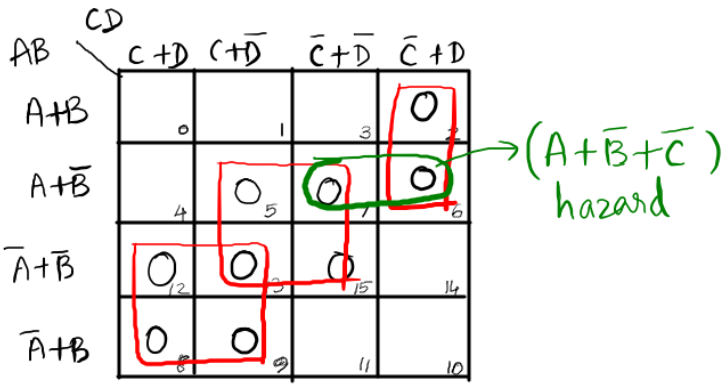
[Show the circuit diagrams for any 2 of the above solutions including the hazard terms. This forms the hazard-free circuits.]

1b. Find a minimum OR-AND circuit for the function G given below:

G (A, B, C, D) = Π M (2, 5, 6, 7, 8, 9, 12, 13, 15)

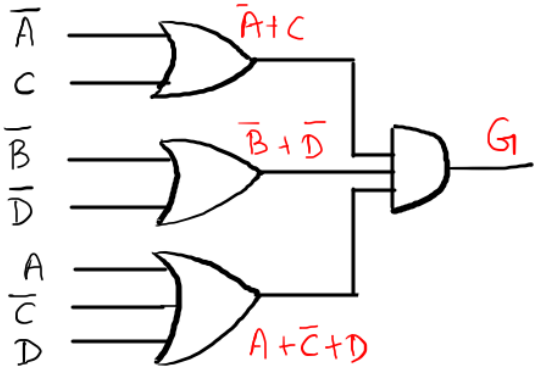
Identify the hazard, and also find an OR-AND circuit for G that has no hazards.

Answer:

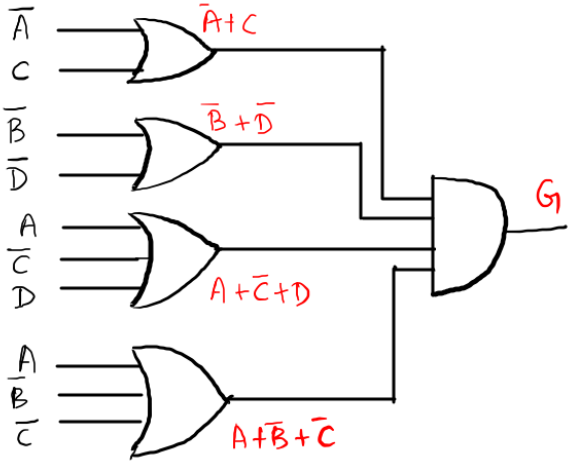


The hazard is caused by maxterms M6 & M7. It is a Static-0-hazard. The term corresponding to the hazard is (A+B'+C').

The minimum solution for the function G is (A'+C) (B'+D') (A+C'+D). Its circuit diagram si shown below.



The hazard-free expression for G is (A'+C) (B'+D') (A+C'+D) (A+B'+C'). Its OR-AND circuit diagram is shown below.



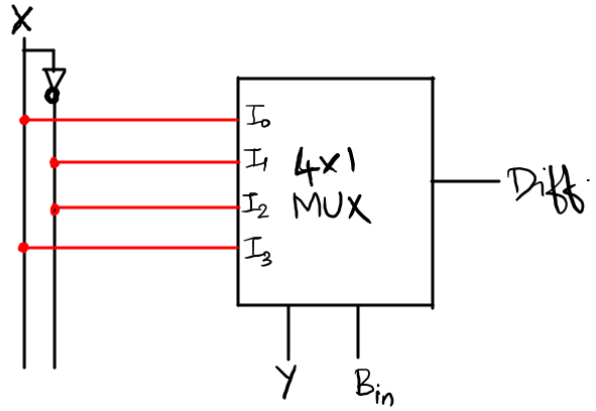
2a. Implement a full subtracter using two 4:1 MUXes and one inverter. Use B_{in} and Y as control inputs of the MUXes and connect 1's, 0's, X or X' to each data input.

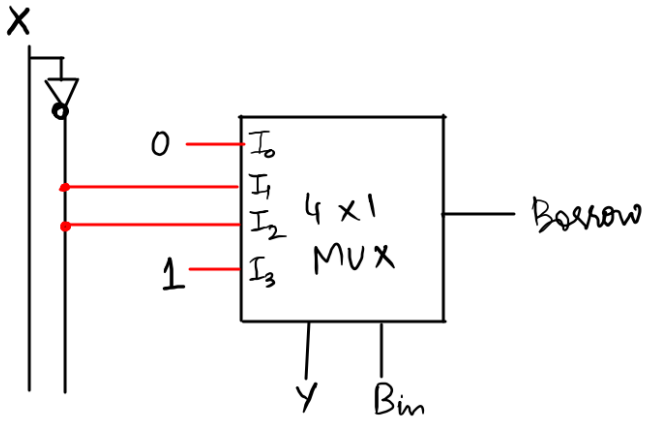
Answer:

Difference, Diff = $\sum$ m (1, 2, 4, 7)

Borrow, B_{out} = $\sum$ m (1, 2, 3, 7)

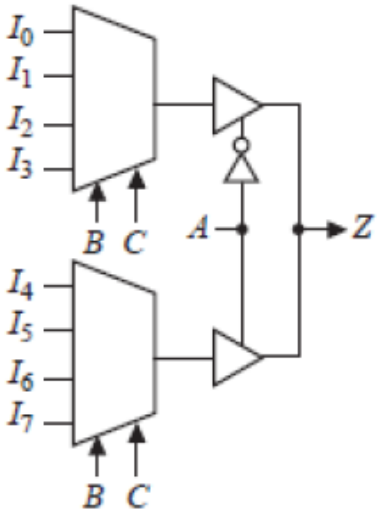
$x\ y\ b_{in}$	$Diff\ B_{out}$
0 0 0	0 0
0 0 1	1 1
0 1 0	1 1
0 1 1	0 1
1 0 0	1 0
1 0 1	0 0
1 1 0	0 0
1 1 1	1 1





2b. Implement an 8:1 MUX using two 4:1 MUXes, two 3-state buffers and one inverter.

Answer:



An 8:1 MUX requires 8 inputs (I0, I1, I2, I3, I4, I5, I6 and I7), 3 select lines (A, B, C) and 1 output Z.

The 8 inputs to the 8:1 MUX are given 4 each through each of the 4:1 MUXes. Since a 4:1 MUX requires only 2 select lines, the lower significant bits of the select lines, B and C are given to each of the 4:1 MUXes.

The remaining 3rd select line A is given through two 3-state buffers to each of the 4:1 MUXes so that A can be used to control which MUX gives the output. For this, one 3-state buffer is connected with an active low enable input, and the other 3-state buffer with an active high enable input.

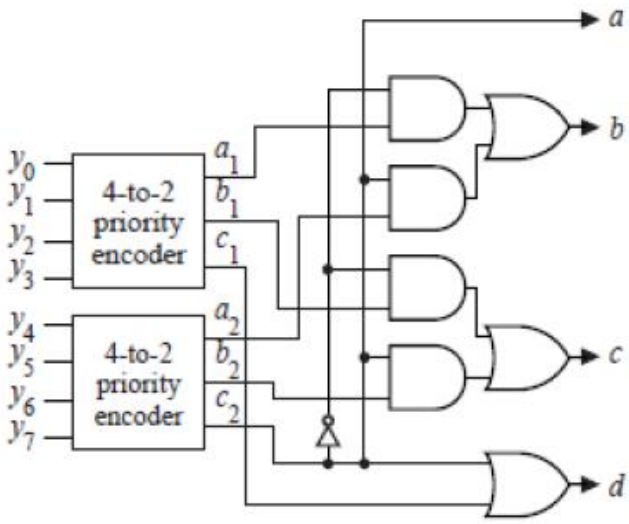
The output of the 8:1 MUX, Z is taken through the outputs of the two 3-state buffers that are connected together.

When A=0, the top MUX will give the output from any of its inputs (I0 to I3) based on values of B and C.

When A=1, the bottom MUX will give the output from any of its inputs (I4 to I7) based on the values of B and C.

3a. Implement an 8 to 3 priority encoder using two 4 to 2 priority encoders and any additional necessary gates.

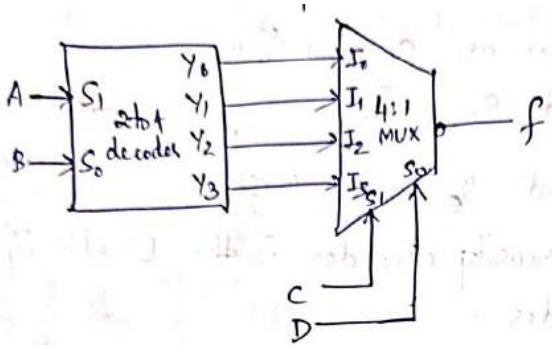
Answer:



If any of the inputs y_0 through y_7 is 1, then d of the 8-to-3 decoder should be 1. But in that case, c_1 or c_2 of one of the 4-to-2 decoders will be 1. So $d = c_1 + c_2$.

If one of the inputs y_4, y_5, y_6, and y_7 is 1, then a should be 1, and b and c should correspond to a_2 and b_2, respectively. Otherwise, a should be 0, and b and c should corresond to a_1 and b_1, respectively. So $a = c_2$, $b = c_2a_2 + c_2'a_1$, and $c = c_2b_2 + c_2'b_1$.

3b. The circuit below has a 2 to 4 decoder with active high outputs connected to a 4:1 MUX with an active low output. Derive a minimum SOP expression for the output, F (A, B, C, D).



Answer:

Ans:- Decoder o/ps are:

(a) $Y_0 = \bar{A}\bar{B}$, $Y_1 = \bar{A}B$, $Y_2 = A\bar{B}$ & $Y_3 = AB$.

These are same as i/ps to the 4:1 MUX.

$\therefore I_0 = \bar{A}\bar{B}$, $I_1 = \bar{A}B$, $I_2 = A\bar{B}$ & $I_3 = AB$.

$S_1 = C$ & $S_0 = D$ are the 2 select lines for the 4:1 MUX.

$\therefore$

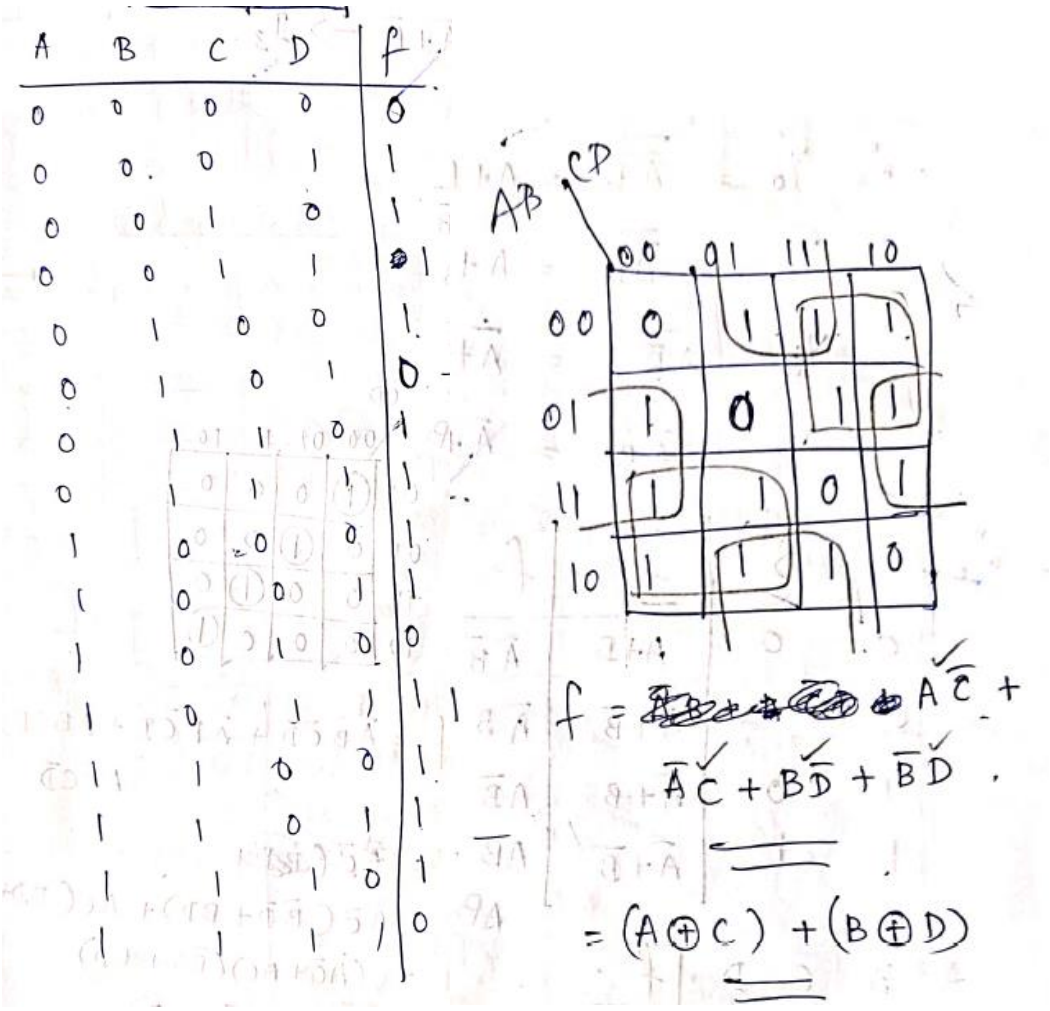
C	D	$\bar{f}$	f
0	0	$I_0 = \bar{A}\bar{B}$	$A+B$
0	1	$I_1 = \bar{A}B$	$A+\bar{B}$
1	0	$I_2 = A\bar{B}$	$\bar{A}+B$
1	1	$I_3 = AB$	$\bar{A}+\bar{B}$

$\overline{\bar{A}\bar{B}} = \bar{\bar{A}} + \bar{\bar{B}}$
$= A+B$

$\overline{\bar{A}B} = \bar{\bar{A}} + \bar{B}$
$= A+\bar{B}$

$\overline{A\bar{B}} = \bar{A} + \bar{\bar{B}}$
$= \bar{A}+B$

$\overline{AB} = \bar{A}+\bar{B}$



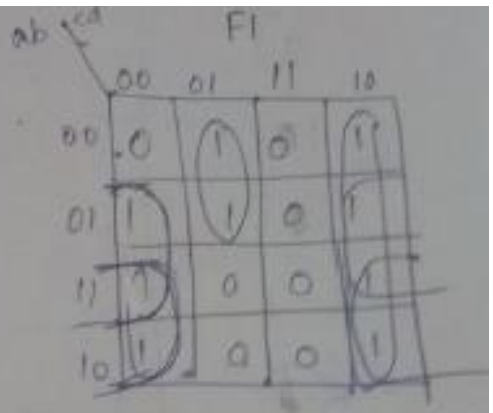
4. Implement the following functions using a 4x5x4 PLA:

F1(a, b, c, d) = Σ m(1, 2, 4, 5, 6, 8, 10, 12, 14)

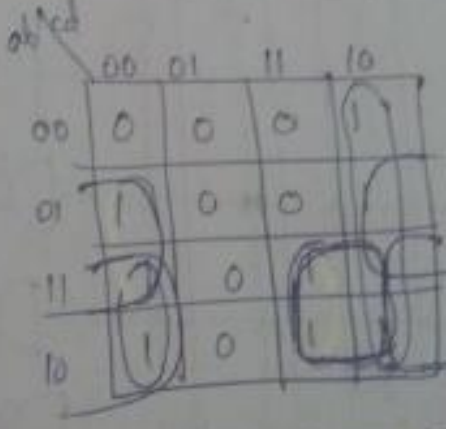
F2(a, b, c, d) = Σ m(2, 4, 6, 8, 10, 11, 12, 14, 15)

Answer:

a	b	c	d	F_1	F_2
0	0	0	0	0	0
0	0	0	1	1	0
0	0	1	0	1	1
0	0	1	1	0	0
0	1	0	0	1	1
0	1	0	1	1	0
0	1	1	0	1	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	0	1	0	0
1	0	1	0	1	1
1	0	1	1	0	1
1	1	0	0	1	1
1	1	0	1	0	0
1	1	1	0	1	1
1	1	1	1	0	1



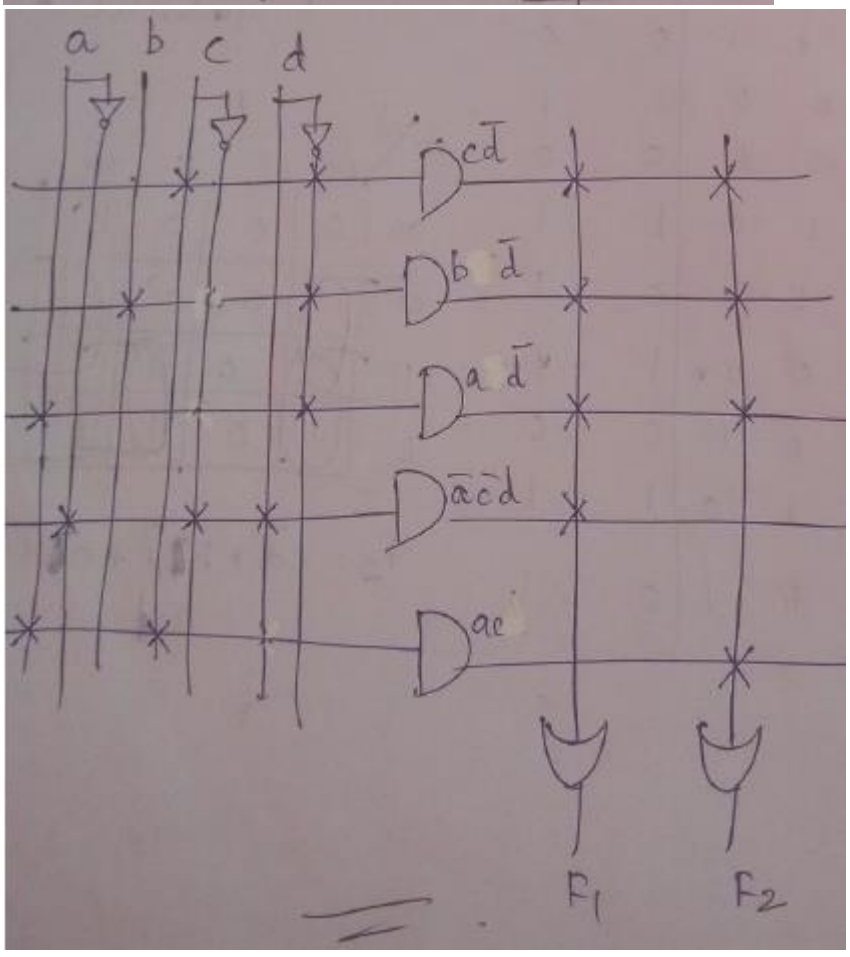
$F_1 = a\bar{c}\bar{d} + b\bar{d} + a\bar{d} + \bar{a}\bar{c}d$



$F_2 = c\bar{d} + b\bar{d} + a\bar{d}$

PLA programtable

Product terms	i/ps a	b	c	d	o/ps F_1	F_2
$c\bar{d}$	-	-	1	0	1	1
$b\bar{d}$	-	1	-	0	1	1
$a\bar{d}$	1	-	-	0	1	1
$\bar{a}\bar{c}d$	0	-	0	1	1	0
ac	1	-	1	-	0	1



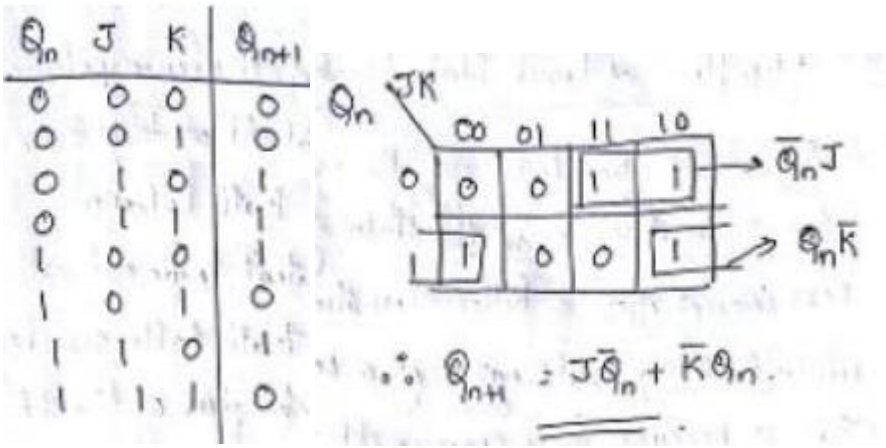
5a. With necessary diagrams and proper explanation, derive the truth table, state transition diagram, characteristic equation and excitation table for a JK flip-flop.

Answer:

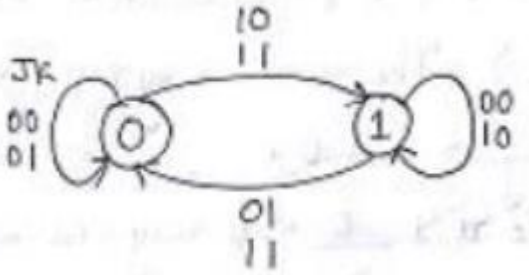
Truth Table

J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\overline{Q}_0$ (toggles)

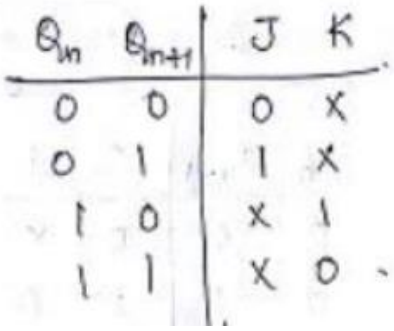
Characteristic equation of JK FF:



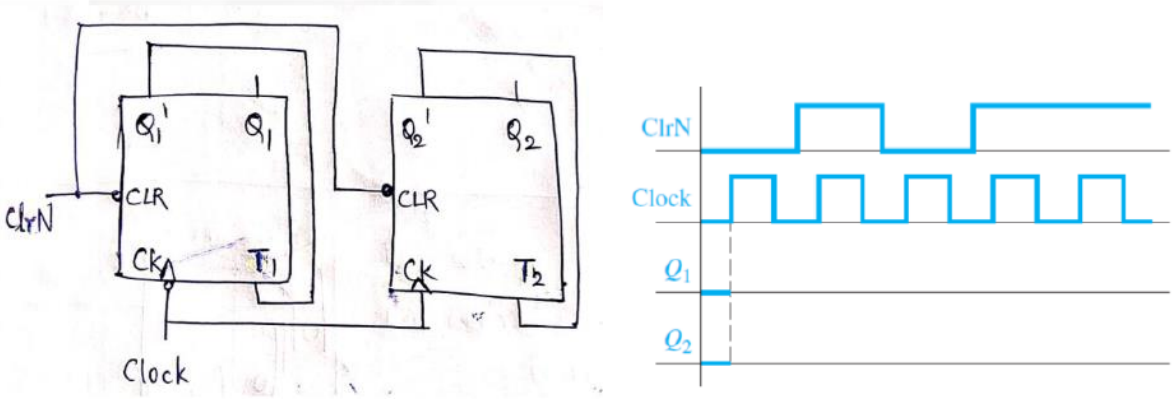
State transition diagram of JK FF:



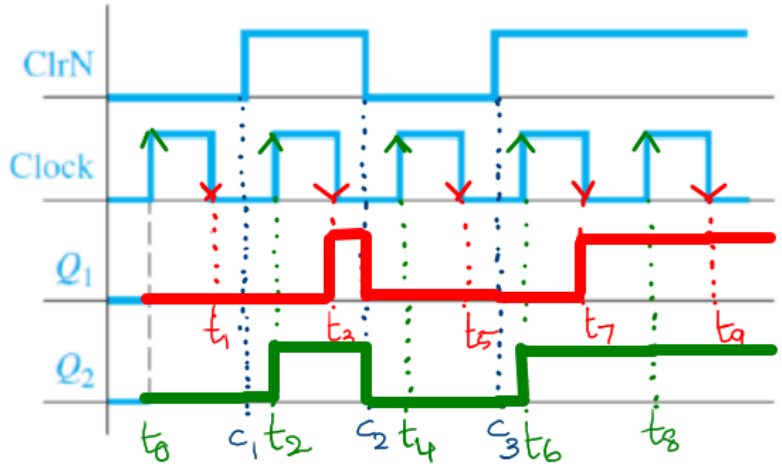
Excitation Table of JK FF



5b. Complete the timing diagram for the following circuit.



Answer:

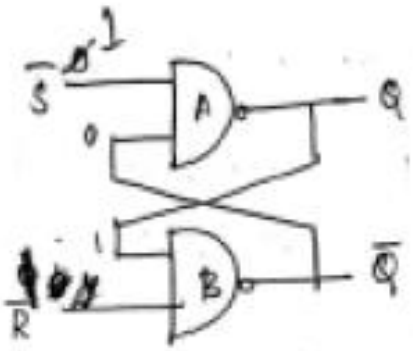


6a. Explain the working of an SR latch using NAND gate.

Answer:

(2) NAND gate Latch

→ This is slightly different from the NOR gate latch.
→ Called as $\overline{SR}$ FF.
→ An active low SR latch can be constructed using 2 cross-coupled NAND gates.



A	B	NAND gate o/p
0	0	1
0	1	1
1	0	1
1	1	0

1) $\bar{S}=0$, $\bar{R}=0$

$Q=1, \bar{Q}=0$: i/ps to A are 0 & 0 ⇒ o/p 1
i/ps to B are 1 & 0 ⇒ o/p 1

$Q=0, \bar{Q}=1$: i/ps to A are 0 & 1 ⇒ o/p 1
i/ps to B are 0 & 1 ⇒ o/p 1.

⇒ Invalid

2) $\bar{S}=0$, $\bar{R}=1$.

$Q=1, \bar{Q}=0$ i/ps to A are 0 & 0 ⇒ o/p 1
i/ps to B are 1 & 1 ⇒ o/p 0

i.e $Q=1$, $\bar{Q}=0$.

$Q=0, \bar{Q}=1$. i/ps to A are 0 & 1 ⇒ o/p 1
i/ps to B are 1 & 1 ⇒ o/p 0

i.e, $Q=1$, $\bar{Q}=0$

⇒ SET state

3) $\bar{S} = 1$, $\bar{R} = 0$.

$Q = 1$, $\bar{Q} = 0$ i/ps to B are 1 & 0 ⇒ o/p 1

i/ps to A are 1 & 1 ⇒ o/p 0

$Q = 0$, $\bar{Q} = 1$

$Q = 0$, $\bar{Q} = 1$. i/ps to A are 1 & 1 ⇒ o/p 0

i/ps to B are 0 & 0 ⇒ o/p 1 .

a) $Q = 0$, $\bar{Q} = 1$

⇒ RESET state

4) $\bar{S} = 1$, $\bar{R} = 1$

$Q = 1$, $\bar{Q} = 0$. i/ps to B are 1 & 1 ⇒ o/p 0 .

i/ps to A are 1 and 0 ⇒ o/p 1

a) $Q = 1$, $\bar{Q} = 0$.

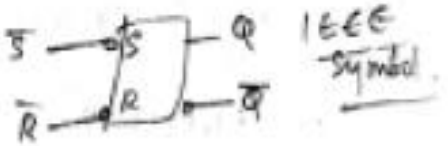
$Q = 0$, $\bar{Q} = 1$. i/ps to B are 0 & 1 ⇒ o/p 1 .

i/ps to A are 1 and 1 ⇒ o/p 0 .

a) $Q = 0$, $\bar{Q} = 1$.

⇒ No change state .

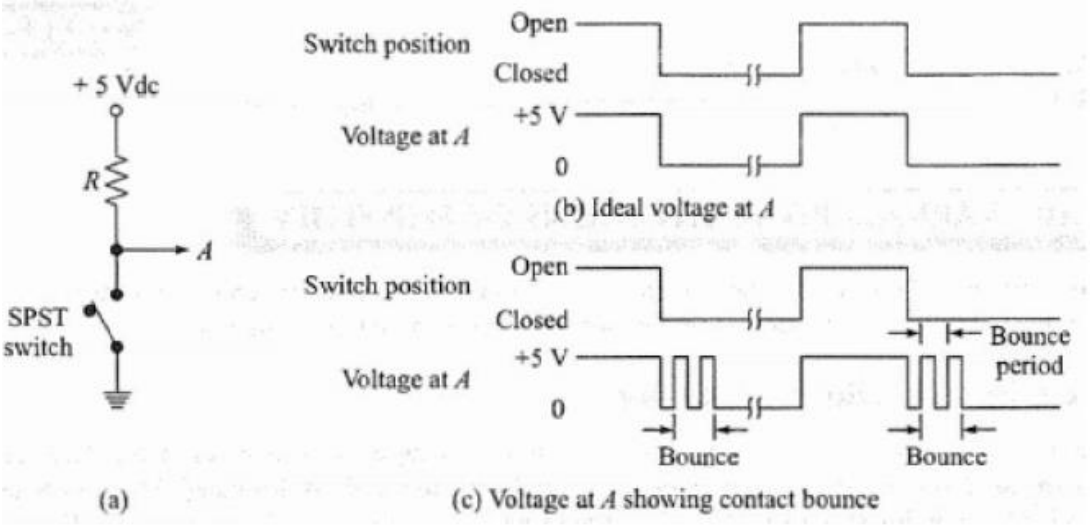
$\bar{S}$	$\bar{R}$	Q_n
0	0	Invalid
0	1	SET
1	0	RESET
1	1	No change .



IEEE Symbol

Logic Symbol .

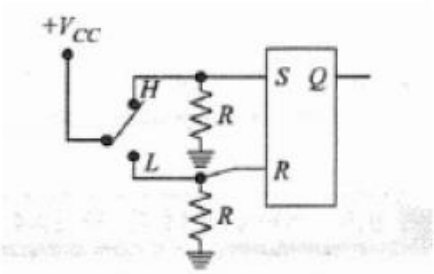
6b. Explain in detail, how an SR latch can be used to eliminate the switch contact bounce.



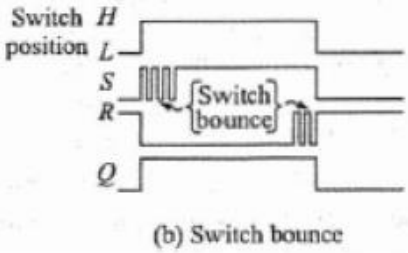
In actuality, the waveform at point A will appear more or less as shown in figure (c), as the result of a phenomenon known as contact bounce. Any mechanical switching device consists of a moving contact arm restrained by some sort of a spring system. As a result, when the arm is moved from one stable position to the other, the arm bounces, much as a hard ball bounces when dropped on a hard surface. The number of bounces that occur and the period of the bounce differ for each switching device. Notice carefully that in this particular instance, even though actual physical contact bounce occurs each time the switch is opened or closed, contact bounce appears in the voltage level at point A only when the switch is closed.

If the voltage at point A is applied to the input of a TTL circuit, the circuit will respond properly when the switch is opened, since no contact bounce occurs. However, when the switch is closed, the circuit will respond as if multiple signals were applied, rather than the single-switch closure intended - the undesired result of mechanical contact bounce. There is a need here for some sort of electronic circuit to eliminate the contact bounce problem.

RS Latch Debounce Circuit



(a) Switch contact bounce eliminator



(b) Switch bounce

The RS latch in the figure above will remove any contact bounce due to the switch. The output (Q) is used to generate the desired switch signal. When the switch is moved to position H, R = 0 and S = 1. Bouncing occurs at the S input due to the switch. The flip-flop "sees" this as a series of high and low inputs, settling with a high level. The flip-flop will immediately be set with Q = 1 at the first high level on S. When the switch bounces, losing contact, the input signals are R = S = 0, therefore the flip-flop remains set (Q = 1). When the switch regains contact, R = 0 and S = 1; this causes an attempt to again set the flip-flop. But since the flip-flop is already set, no changes occur at Q. The result is that the flip-flop responds to the first, and only to the first, high level at its S input, resulting in a "clean" low-to-high signal at its output (Q).

When the switch is moved to position L, S = 0 and R = 1. Bouncing occurs at the R input due to the switch. Again, the flip-flop "sees" this as a series of high and low inputs. It simply responds to the first high level, and ignores all following transitions. The result is a "clean" high-to-low signal at the flip-flop output.