ADE IAT -2

MAX MARKS-50

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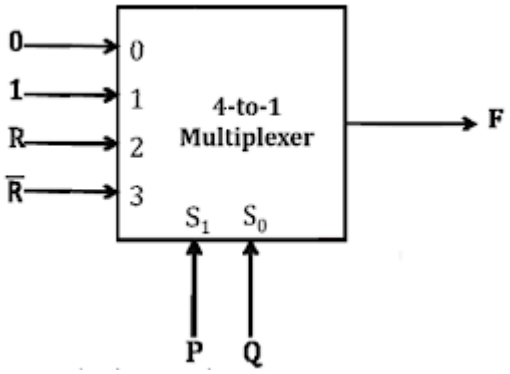
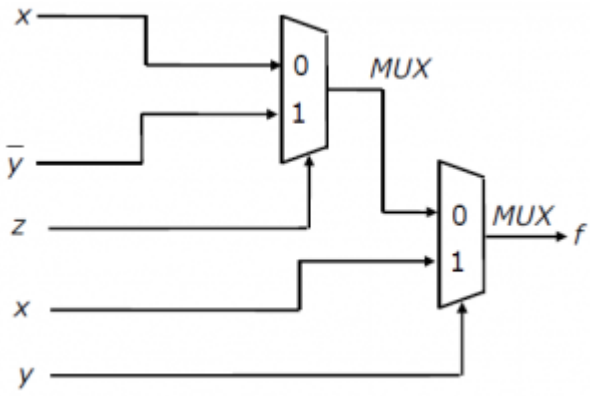
MCQ

1. Consider a 4-to-1 multiplexer with two select lines S1 and S0, given below. Determine the output F. * 2 points



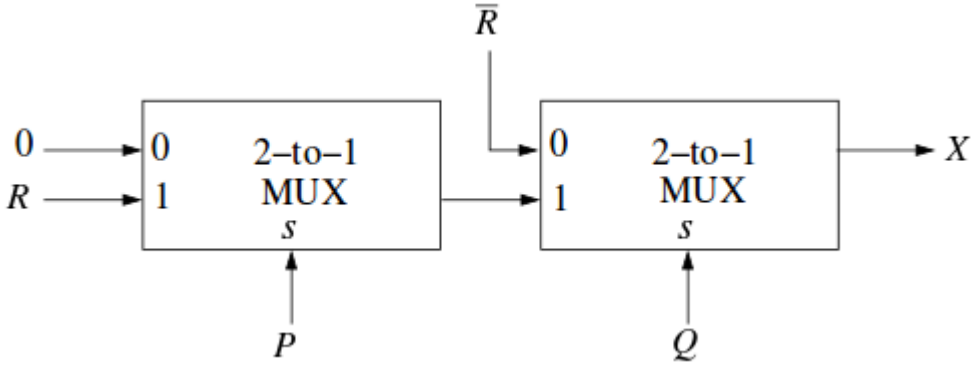
- [x] P'Q + QR' + PQ'R
- [ ] P'Q + P'QR' + PQR' + PQ'R
- [ ] P'QR + P'QR' + QR' + PQ'R
- [ ] PQR'

2. Consider the circuit above. Which one of the following options correctly represents f (x, y, z)? * 2 points



- (●) xz' + xy + y'z
- ( ) xz' + xy + (yz)'
- ( ) xz + xy + (yz)'
- ( ) xz + xy' + y'z

3.Consider the two cascaded 2-to-1 multiplexers as shown in the figure.The minimal sum of products form of the output X is * 2 points

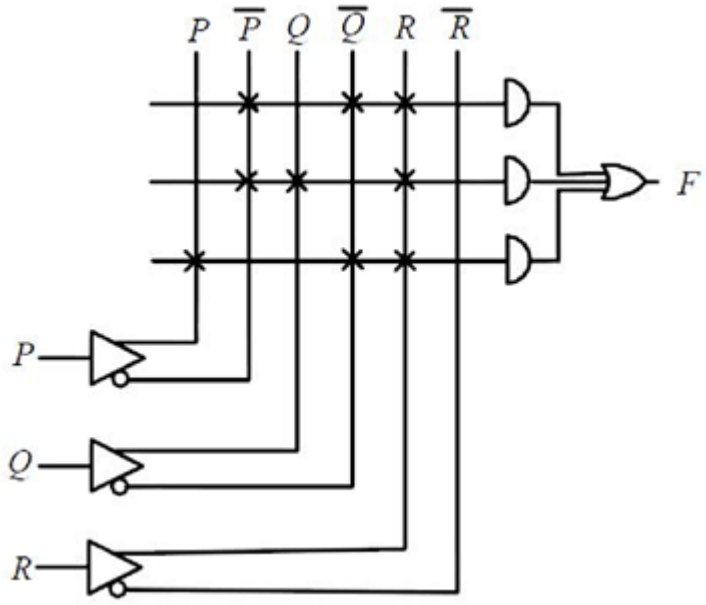


- P'Q'+PQR
- P'Q+QR
- PQ+P'Q'R
- Q'R'+PQR

4. A multiplexer with a 4-bit data select input is a * 1 point

- 4:1 multiplexor
- 2:1 multiplexor
- 16:1 multiplexor
- 8:1 multiplexor

5. A programmable logic array (PLA) is shown in the figure.The Boolean function F implements is * 2 points



- P'Q'R+P'QR+PQ'R'
- (P'+Q'+R) (P'+Q+R)+(P+Q'+R)'
- P'Q'R+P'QR+PQ'R
- NONE OF THESE

6. Logic circuits can also be designed using * 1 point

- PLD
- PLA
- ROM
- RAM

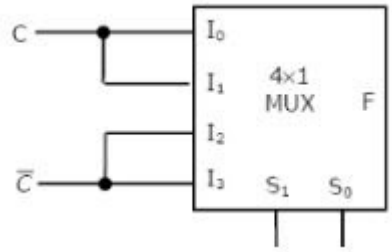
7. PLA refers to * 1 point

- ○ Programmable array logic
- ◉ Programmable logic array
- ○ Programmable loaded array
- ○ None of the above

8.Clock signals are used in the digital Sequential Logic Circuits to * 1 point

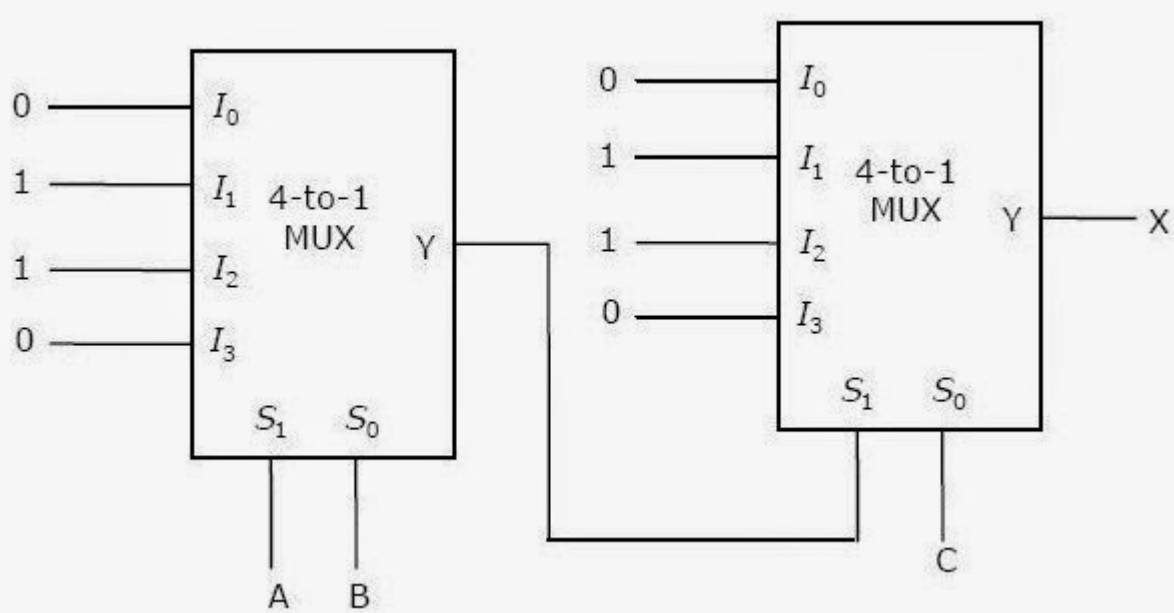
- ○ Tell the time of the day
- ○ Tell how much time has elapsed since the system was turned on
- ○ Carry parllel data signals
- ◉ Synchronize events in various parts of system

9. A 4: 1 Mux is as given in the fig. Find the Boolean Expression of the circuit * 2 points



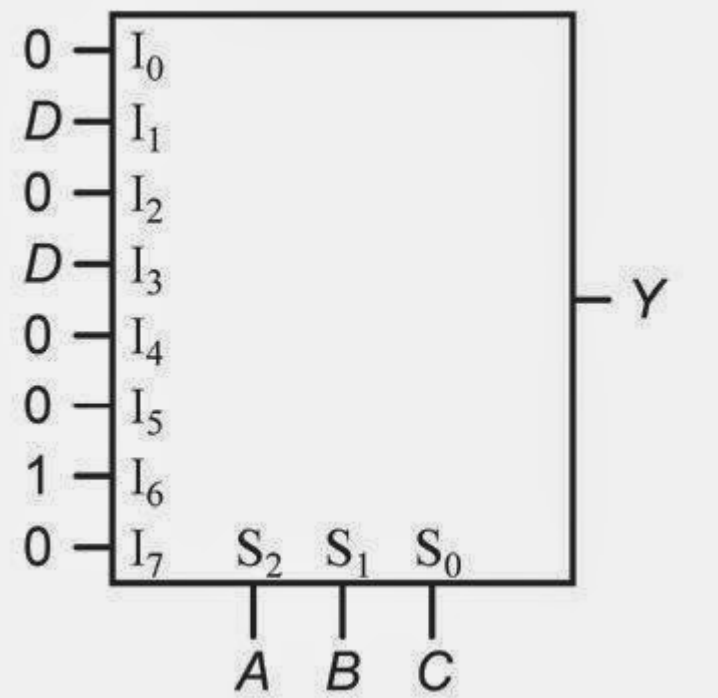
- F = A.C
- F = A+C
- F = B.C
- F = B+C

The Boolean function X will be * 2 points



- (●) X = AB'C' + A'BC' + A'B'C + ABC
- ( ) X = A'BC + AB'C + ABC' + A'B'C'
- ( ) X = AB + BC + AC
- ( ) X = A'B' + B'C' + A'C'

11. An 8:1 Mux is used to used to implement a logic function Y, which can be represented by * 3 points



- ( ) AB'C + AC'D
- ( ) A'BC + AB'D
- (•) ABC' + A'CD
- ( ) A'B'D + AB'C
- ( ) Other: .....

12. What function does the truth table represent? * 1 point

Inputs				Outputs		
D_0	D_1	D_2	D_3	X_0	X_1	V
0	0	0	0	x	x	0
1	0	0	0	0	0	1
x	1	0	0	0	1	1
x	x	1	0	1	0	1
x	x	x	1	1	1	1

- ○ Decoder
- ○ Multiplexer
- ○ Demultiplexer
- ◉ Priority Encoder

13. In this truth table, if we make D0 = 1, D1 = 0, D2 = 1, D3 = 0 then what will be expected out levels (X0, X1) * 1 point

Inputs				Outputs		
D_0	D_1	D_2	D_3	X_0	X_1	V
0	0	0	0	x	x	0
1	0	0	0	0	0	1
x	1	0	0	0	1	1
x	x	1	0	1	0	1
x	x	x	1	1	1	1

- 00
- 01
- 10
- 11

14. A SR Latch is a * 1 point

- Combinational Circuit
- Synchronous Sequential Circuit
- One bit memory element
- One clock delay element

15. A multiplexer is also called as a * 1 point

- Coder
- parallel adder
- (selected) Data selector
- NOR gate

16.A priority encoder means that * 1 point

- the lowest priority goes first.
- (selected) the highest input has priority.
- priority is programmed into the device.
- the lowest input has priority.

17. A circuit which converts some binary code into a singular active output representing its numerical value is a 1 point

- demultiplexer.
- comparator.
- (selected) decoder.
- multiplexer

18.How many possible combinations can a 5-bit Gray Code have? * 1 point

- (●) A) 32
- ( ) B) 20
- ( ) C) 5
- ( ) D) 16

19) In order to select data input I1 of a 74151 eight- line multiplexer, the select inputs must be * 1 point

- ( ) A) E = 1, S0 = 0, S1 = 0, S2 = 1
- ( ) B) E = 0, S0 = 1, S1 = 0, S2 = 1
- ( ) C) E = 0, S0 = 1,S1 = 1,S2 = 0
- (●) D) E = 1, S0 = 1, S1 = 0, S2 = 0

20)Which device is used in computer hardware to interpret the binary code of the computer instruction? * 1 point

- (●) A) Decoder
- ( ) B) Multiplexer
- ( ) C) Encoder
- ( ) D) Demultiplexer

21) A 1- of- 8 octal decoder has eight outputs and decodes an input of _____ bits. * 1 point

- A) four
- B) one
- C) three
- D) two

22) A flip-flop has _____. * 1 point

- A.one stable state
- B.no stable states
- C.two stable states
- D.none of the above

23) Which statement BEST describes the operation of a negative-edge-triggered D flip-flop? * 1 point

- A.The logic level at the D input is transferred to Q on NGT of CLK.
- B.The Q output is ALWAYS identical to the CLK input if the D input is HIGH.
- C.The Q output is ALWAYS identical to the D input when CLK = PGT.
- D.The Q output is ALWAYS identical to the D input.

24) What will be the state of Q and Q' after a flip-flop has been reset? * 1 point

- (●) A. Q = 0, Q' = 1
- ( ) B. Q = 1, Q' = 0
- ( ) C. Q = 0, Q' = 0
- ( ) D. Q = 1, Q' = 1

25)Circuits made up of combinations of logic gates, with no feedback from outputs to inputs. * 1 point

- ( ) A. Latch
- ( ) B. Sequential logic circuit
- (●) C. Combinational logic circuit
- ( ) D. Memory

26) A multiplexer is described by its size through _____, where n = number of bits. * 1 point

- ( ) A. n x 2^n
- ( ) B. 1 x 2^n
- (●) C. 2^n x 1
- ( ) D. 2^n x m

27) _____ refers to the class of logic circuit containing flip-flops. * 0 points

- A. Combinational
- B. Sequential
- C. Linear
- D. Feedback

28) The number of logic gates of the same family that can be connected to the input of a particular gate without degrading the circuit performance. * 1 point

- A. Fan-in
- B. Fan-out
- C. Input-drive
- D. Input noise immunity

29) An IC that contains a large number of interconnected logic functions wherein the user can program the IC for a specific function by selectively breaking the appropriate interconnections. * 1 point

- A. RAM
- B. ROM
- C. PLD
- D. PLC

30) One example of the use of an S-R flip-flop is as _____ * 1 point

- a) Transition pulse generator
- b) Racer
- c) Switch debouncer
- d) Astable oscillator

31)Which of the following is correct for a gated D flip-flop? * 1 point

- A. The output toggles if one of the inputs is held HIGH.
- B. Only one of the inputs can be HIGH at a time.
- C. The output complement follows the input when enabled.
- D. Q output follows the input D when the enable is HIGH.

32) Which of the following describes the operation of a positive edge-triggered D flip-flop? * 1 point

- A. If both inputs are HIGH, the output will toggle.
- B. The output will follow the input on the leading edge of the clock.
- C. When both inputs are LOW, an invalid state exists.
- D. The input is toggled into the flip-flop on the leading edge of the clock and is passed to the output on the trailing edge of the clock.

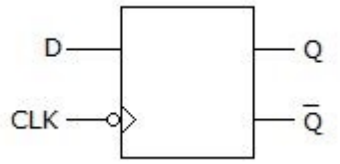
33) On a positive edge-triggered S-R flip-flop, the outputs reflect the input condition when _____. * 1 point

- A. the clock pulse is LOW
- B. the clock pulse is HIGH
- C. the clock pulse transitions from LOW to HIGH
- D. the clock pulse transitions from HIGH to LOW

34)If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____. * 1 point

- A. SET
- B. RESET
- C. clear
- D. invalid

35) The symbols on this flip-flop device indicate _____. * 1 point



- (●) A. triggering takes place on the negative-going edge of the CLK pulse
- ( ) B. triggering takes place on the positive-going edge of the CLK pulse
- ( ) C. triggering can take place anytime during the HIGH level of the CLK waveform
- ( ) D. triggering can take place anytime during the LOW level of the CLK waveform

36) Latches constructed with NOR and NAND gates tend to remain in the latched condition due to which configuration feature? * 1 point

- (●) A. cross coupling
- ( ) B. gate impedance
- ( ) C. low input voltages
- ( ) D. asynchronous operation

37) The basic latch consists of _____ * 1 point

- [x] a) Two inverters
- [ ] b) Two comparators
- [ ] c) Two amplifiers
- [ ] d) Two adders

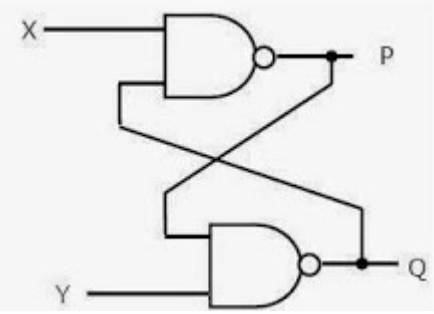
38) The output of latches will remain in set/reset until _____ * 1 point

- [x] a) until the trigger pulse is given to change the state
- [ ] b) Any pulse given to go into previous state
- [ ] c) They don't get any pulse more
- [ ] d) The pulse is edge-triggered

39)The characteristic equation of SR flipflop is _____ * 2 points

- [ ] A) Q(n+1) = (S + Q(n))R'
- [ ] B) Q(n+1) = SR + Q(n)R
- [ ] C) Q(n+1) = S'R + Q(n)R
- [x] D) Q(n+1)= S+ Q(n)R'

40) In the following circuit, binary values were applied to the inputs X and Y. Inputs of the NAND latch shown in the figure in the sequences indicated below. X=0,Y=1; X=0,Y=0; X=1, Y=1; What will P,Q outputs be? * 3 points



- (●) A) P=1, Q=0; P=1,Q=0; P=1,Q=0 OR P=0,Q=1
- ( ) B) P=1, Q=0; P=0, Q=1 or P=0, Q=1; P=0, Q=1
- ( ) C) P=1, Q=0; P=1, Q=1; P=1, Q=0 or P=0, Q=1
- ( ) D) P=1, Q=0; P=1, Q=1; P=1, Q=1