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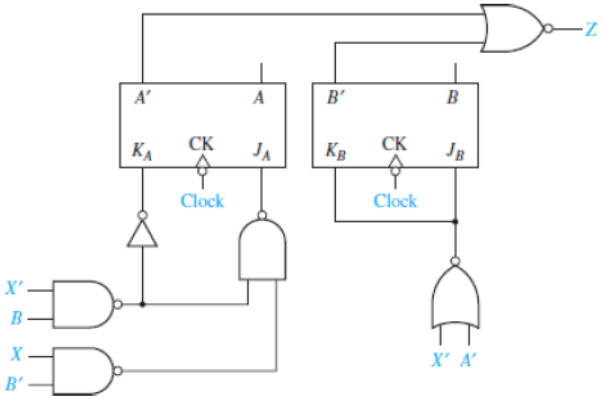
Internal Assessment Test 3 – December 2020

Sub:	Analog and Digital Electronics					Sub Code:	18CS33	Branch:	ISE		
Date:	14.12.2020	Duration:	90 mins	Max Marks:	50	Sem/Sec:	3 – A, B, C		OBE		

Answer **any FIVE FULL** Questions

		MARKS	CO	RBT
1	(a) A 4-bit PIPO shift register using D flip-flops is designed such that it should load if Sh = 0 and Ld = 1, hold its state if Sh = Ld = 0, shift left if Sh = 1 and Ld = 0 and shift right if Sh = 1 and Ld = 1. Draw the circuit of this shift register using four D flip-flops and four 4-to-1 MUXes. (b) Design a counter using T flip-flops which counts in the following sequence (circuit diagram not required): 0 → 4 → 7 → 2 → 3 → 0…	[5+5]	CO5	L3
2	(a) Analyze and identify the type of circuit (Moore or Mealy) given below. Obtain the next state equations, transition table, state table and state graph for the circuit.  (b) A U-V flip-flop behaves as follows: If UV = 00, the flip-flop does not change state. If UV = 10, the flip-flop is set to Q = 0. If UV = 11, the flip-flop changes state. The input combination UV = 01 is not allowed. Complete the following table, using don't-cares where possible. Q Q^+ | U V 0 0 0 1 1 0 1 1	[8+2]	CO5	L4

3	Using dataflow modeling, write the VHDL code for the following: (a) A 2:1 multiplexer without using conditional signal assignment statement. (b) An 8:1 multiplexer using conditional signal assignment statement.	[5+5]	CO4	L3
4	Explain in detail the two types of digital to analog conversion.	[5+5]	CO1	L2
5	(a) Explain the working of a 3-bit Flash type ADC. (b) A 555 timer is configured to work in the astable mode with a frequency of 2 kHz and duty cycle of 80%. Assuming C=0.1uF, design the circuit.	[5+5]	CO1	L2, L3
6	(a) Explain the working and characteristics of photodiodes. (b) With the help of neat circuit diagrams and mathematical analysis, explain the accurate analysis technique of biasing a voltage divider circuit.	[5+5]	CO1	L2

Scheme of Evaluation

Internal Assessment Test 3 – December 2020

Sub:	Analog and Digital Electronics							**Code:**	18CS33
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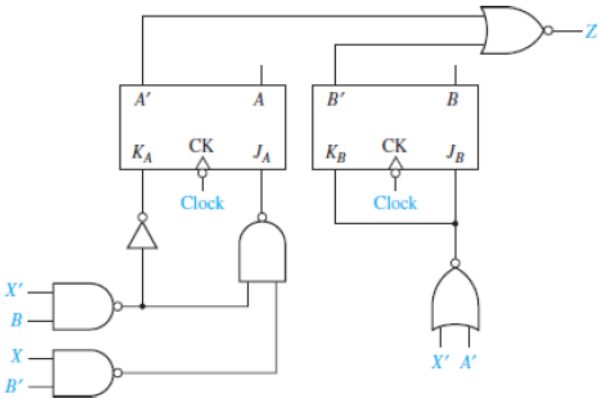
Note: Answer Any Five Questions

Question #	**Description**	**Marks Distribution**		**Max Marks**
1	(a) A 4-bit PIPO shift register using D flip-flops is designed such that it should load if Sh = 0 and Ld = 1, hold its state if Sh = Ld = 0, shift left if Sh = 1 and Ld = 0 and shift right if Sh = 1 and Ld = 1. Draw the circuit of this shift register using four D flip-flops and four 4-to-1 MUXes. • Show the next state table for this shift register. • Show the implementation of the shift register using four D flip-flops and four 4:1 MUXes.	[2+3]	[5+5]	10
	(b) Design a counter using T flip-flops which counts in the following sequence (circuit diagram not required): 0 → 4 → 7 → 2 → 3 → 0… • Show the transition table for this counter & obtain the T inputs to the 3 flip-flops. • Obtain minimized expressions for T_a, T_b & T_c.	[2.5+2.5]		

2	(a) Analyze and identify the type of circuit (Moore or Mealy) given below. Obtain the next state equations, transition table, state table and state graph for the circuit.  • (Moore circuit) - Obtain the input equations and output equation • Obtain the transition table • Obtain the state table • Illustrate using state graph.	[2+2+2+2]	[8+2]	10
	(b) A U-V flip-flop behaves as follows: If UV = 00, the flip-flop does not change state. If UV = 10, the flip-flop is set to Q = 0. If UV = 11, the flip-flop changes state. The input combination UV = 01 is not allowed. Complete the following table, using don't-cares where possible. Q Q^+ | U V 0 0 0 1 1 0 1 1 • Complete the excitation table using the state changes given in question.	[2]		

3	Using dataflow modeling, write the VHDL code for the following: (a) A 2:1 multiplexer without using conditional signal assignment statement. • Use proper syntax. • Using the correct logic, write the VHDL code for a 2:1 MUX without "when-select".	[2+3]	[5+5]	10
	(b) An 8:1 multiplexer using conditional signal assignment statement. • Use proper syntax. • Using the correct logic, write the VHDL code for an 8:1 MUX using "when-select".	[2+3]		
4	Explain in detail the two types of digital to analog conversion. • Diagram of Binary weighted resistor DAC • Expression for output voltage & its drawbacks • Diagram of R-2R ladder type DAC • Expression for output voltage & its advantages	[2+3+2+3]	[5+5]	10
5	(a) Explain the working of a 3-bit Flash type ADC. • Circuit diagram • Truth table • Explanation for working	[1.5+1.5+2]	[5+5]	10
	(b) A 555 timer is configured to work in the astable mode with a frequency of 2 kHz and duty cycle of 80%. Assuming C=0.1uF, design the circuit. • Mention the formulas to be used in this problem • Calculate R1. • Calculate R2.	[1+2+2]		
6	(a) Explain the working and characteristics of photodiodes. • Diagram of photodiode • Explanation of working • VI characteristics of photodiode with explanation	[1+2+2]	[5+5]	10

	(b) With the help of neat circuit diagrams and mathematical analysis, explain the accurate analysis technique of biasing a voltage divider circuit. • Circuit diagram for voltage divider circuit & its equivalent Thevenin's circuit • Show the mathematical analysis to obtain base current and collector voltage.	[2+3]		

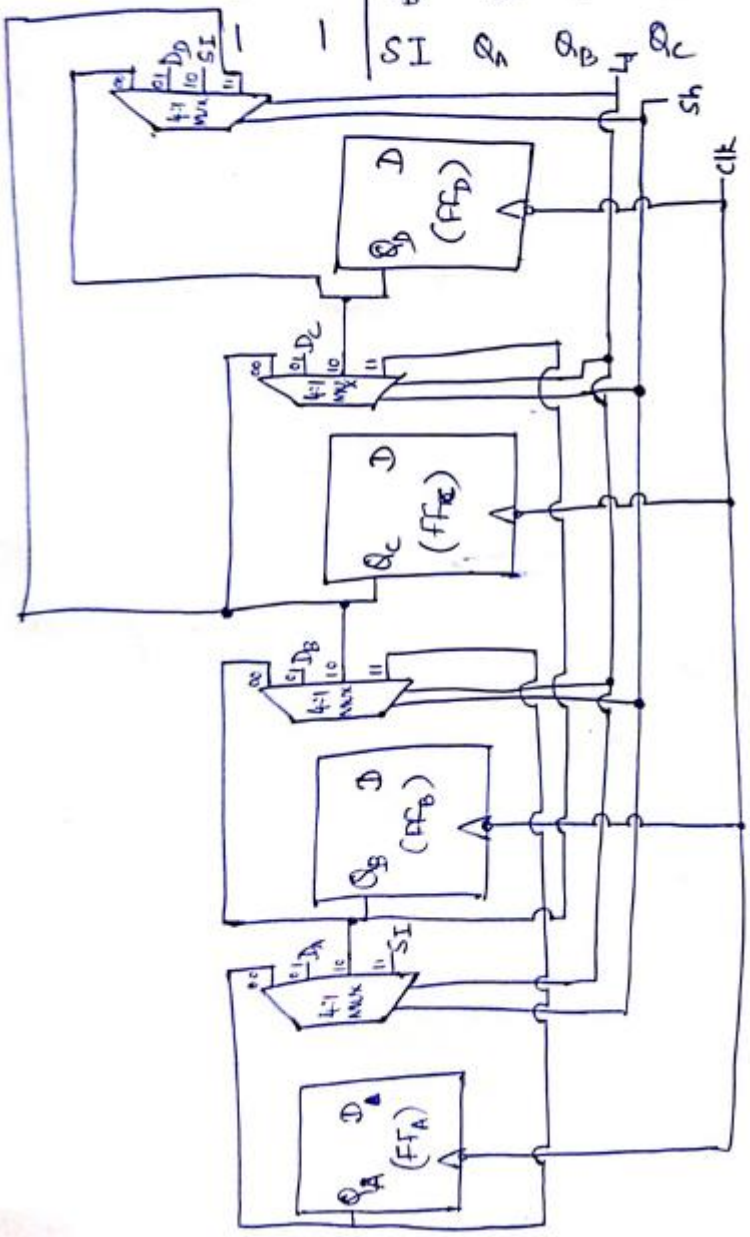
SOLUTIONS

1. (a) A 4-bit PIPO shift register using D flip-flops is designed such that it should load if Sh = 0 and Ld = 1, hold its state if Sh = Ld = 0, shift left if Sh = 1 and Ld = 0 and shift right if Sh = 1 and Ld = 1. Draw the circuit of this shift register using four D flip-flops and four 4-to-1 MUXes.

Answer:

1(a).

Sh	ld	Q_A^+	Q_B^+	Q_C^+	Q_D^+
0	0	Q_A	Q_B	Q_C	Q_D
0	1	D_A	D_B	D_C	D_D
1	0	Q_B	Q_C	Q_D	SI
1	1	SI	Q_A	Q_B	Q_C



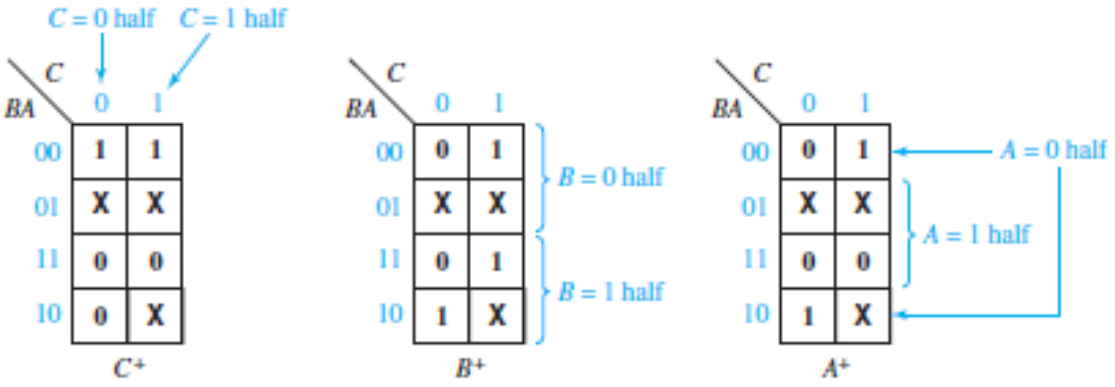
1. (b) Design a counter using T flip-flops which counts in the following sequence (circuit diagram not required):

0 → 4 → 7 → 2 → 3 → 0…

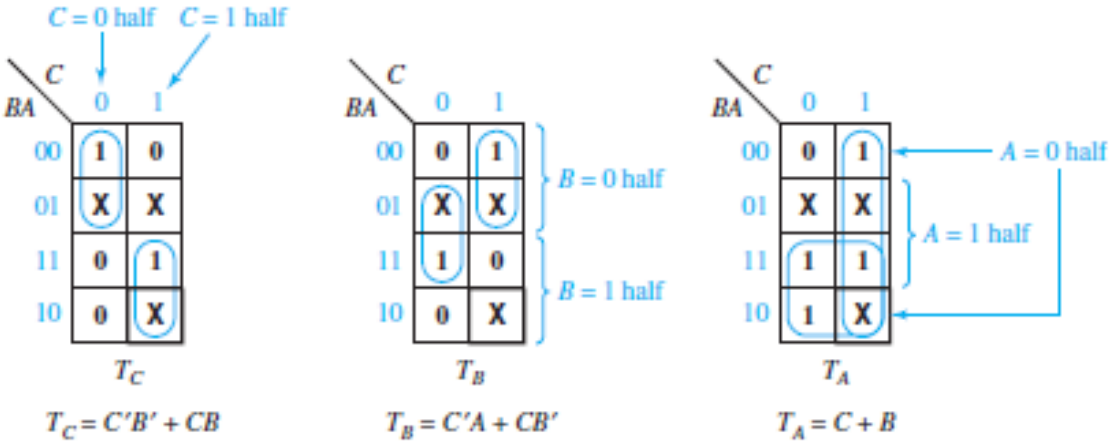
Answer:

State table:

C	B	A	C^+	B^+	A^+
0	0	0	1	0	0
0	0	1	–	–	–
0	1	0	0	1	1
0	1	1	0	0	0
1	0	0	1	1	1
1	0	1	–	–	–
1	1	0	–	–	–
1	1	1	0	1	0

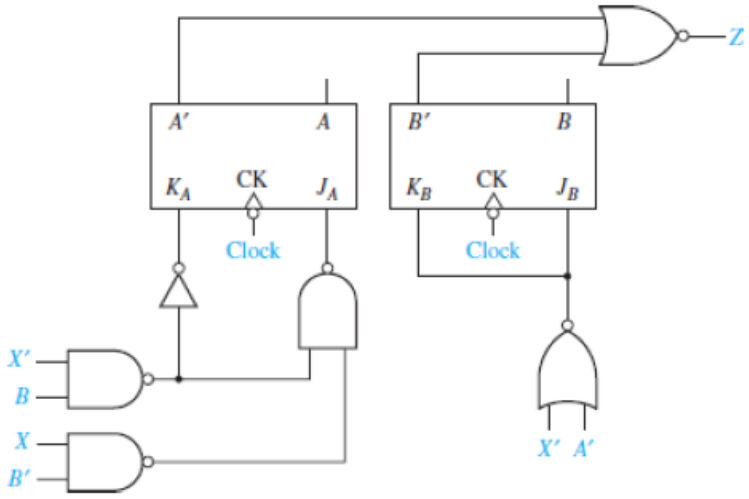


(a) Next-state maps for Table 12-3



(b) Derivation of T inputs

2. (a) Analyze and identify the type of circuit (Moore or Mealy) given below. Obtain the next state equations, transition table, state table and state graph for the circuit.



Answer:

2(a) Input Equations :

$J_A = (\overline{Bx}' \cdot \overline{B'x})$

$= \overline{\overline{Bx}} + \overline{\overline{Bx}}$

$= Bx + \bar{B}\bar{x}$

$= B \oplus x$

$K_A = \overline{\overline{Bx}} = Bx$

$\overline{Bx} = \bar{B} + x$

$\overline{\bar{B}x} = B + \bar{x}$

$K_B = J_B = \overline{A \oplus x} = \overline{A}\,\overline{\bar{x}} + A\bar{x} = \overline{A} \cdot x + A\bar{x}$

Output Equation : $Z = \overline{A + B} = \bar{A} \cdot \bar{B} = A\bar{B} \Rightarrow$ Moore ckt

for JK-FF, next state eqn is given by

$$Q^+ = J\bar{Q} + \bar{K}Q$$

∴ Here, $A^+ = J_A\bar{A} + \bar{K}_A A$

& $B^+ = J_B\bar{B} + \bar{K}_B B$

$\overline{B\bar{X}} = (\bar{B} + X)$

i.e., $A^+ = (B\bar{X} + \bar{B}X)\bar{A} + A(\overline{B\bar{X}})$

$= \bar{A}B\bar{X} + \bar{A}\bar{B}X + A\bar{B} + AX$

$\overline{A\bar{X}} = \bar{A} + X$

and $B^+ = AX\cdot\bar{B} + \overline{A\bar{X}}\cdot B$

$= A\bar{B}X + \bar{A}B + B\bar{X}$

X \ AB	00	01	11	10
0	0	1	0	1
1	1	0	1	1

A^+

X \ AB	00	01	11	10
0	0	1	1	0
1	0	1	0	1

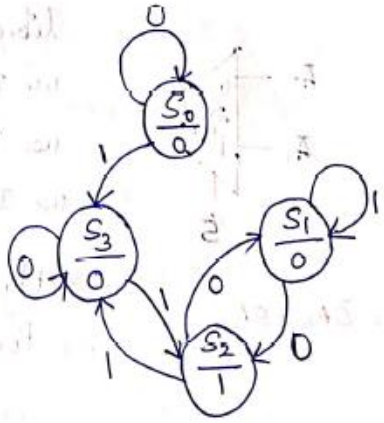
B^+

(PS) AB	(NS) A^+B^+ X=0	X=1	o/p Z
0 0	00	10	0
0 1	11	01	0
1 1	01	10	1
1 0	10	11	0

Transition table

State Table :-

PS	NS X=0	X=1	o/p Z
S_0	S_0	S_3	0
S_1	S_2	S_1	0
S_2	S_1	S_3	1
S_3	S_3	S_2	0



State graph

2. (b) A U-V flip-flop behaves as follows:

If UV = 00, the flip-flop does not change state.

If UV = 10, the flip-flop is set to Q = 0.

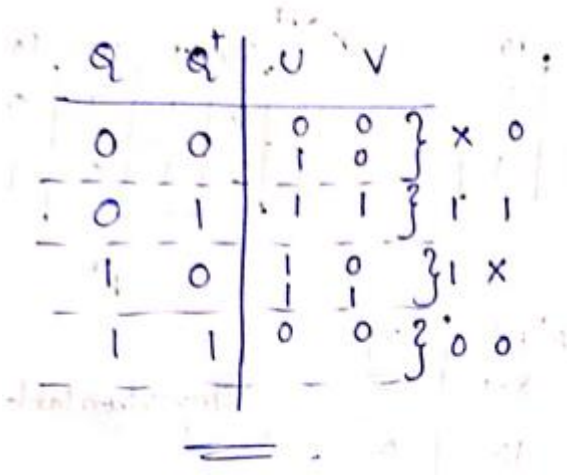
If UV = 11, the flip-flop changes state.

The input combination UV = 01 is not allowed.

Complete the following table, using don't-cares where possible.

Q	Q^+	U	V
0	0		
0	1		
1	0		
1	1		

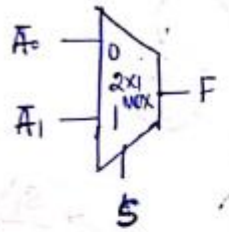
Answer:



3. Using dataflow modeling, write the VHDL code for the following:

(a) A 2:1 multiplexer without using conditional signal assignment statement.

Answer:



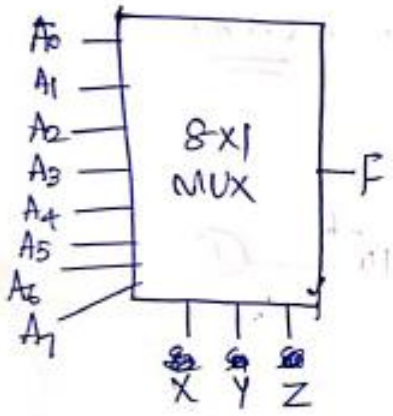
$F = \bar{S}A_0 + SA_1$

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity mux21 is
    Port (A : in STD_LOGIC_VECTOR (1 downti
          s : in STD_LOGIC;
          F : out STD_LOGIC);
end mux21;
architecture behavioral of mux21 is
begin
F<=((not s)and a(0)) or (s and a(1));
end behavioral;
```

(b) An 8:1 multiplexer using conditional signal assignment statement.

Answer:



```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity mux81 is
  Port (A0, A1, A2, A3, A4, A5, A6, A7 :
        in STD_LOGIC;
        X, Y, Z : in STD_LOGIC;
        F : out STD_LOGIC);
end mux81;
architecture behavioral of mux81 is
begin
  F <= A0 when X&Y&Z = "000"
  else A1 when X&Y&Z = "001"
  else A2 when X&Y&Z = "010"
  else A3 when X&Y&Z = "011"
  else A4 when X&Y&Z = "100"
  else A5 when X&Y&Z = "101"
  else A6 when X&Y&Z = "110"
  else A7;
end behavioral;
```

4. Explain in detail the two types of digital to analog conversion.

Answer:

1. Binary weighted Resistor DAC

This DAC is one of the simplest circuit of n-bit DAC shown in Figure 9-3. Here op-amp is used to sum n-binary weighted currents derived from a reference voltage V_R via current scaling resistors.

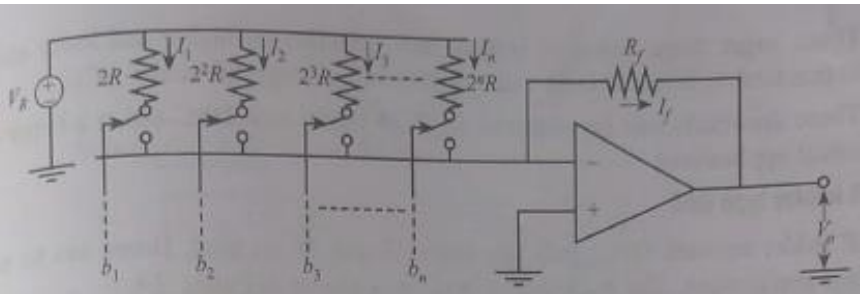


FIGURE 9-3: Binary weighted resistor DAC

Figure 9-3 shows Binary weighted resistor DAC circuit uses n-electronic switches controlled by the binary inputs $b_1, b_2, \ldots, b_n$. If the binary input is high (logic 1), then switch connects the resistance to reference voltage V_R.

When digital input bit is low (logic 0), it disconnects the resistor from V_R and no current flows through corresponding circuit.

i.e., mathematically

for ON switch current $I = \dfrac{V_R}{R}$

for OFF switch current $I = 0$.

Due to high input impedance of op-amp summing current will flow through R_f

$\therefore$ The total current through R_f is written as

$$I_f = I_1 + I_2 + I_3 + \cdots + I_n \tag{9-5}$$

$$= \frac{V_R}{2^1 R} b_1 + \frac{V_R}{2^2 R} b_2 + \frac{V_R}{2^3 R} b_3 + \cdots + \frac{V_R}{2^n R} b_n$$

$$= \frac{V_R}{R}\left[b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots + b_n 2^{-n} \right]$$

The output voltage across R_f is

$$V_o = -I_f R_f$$

Substituting for $I_f, V_o = \dfrac{-V_R}{R} R_f \left[b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots + b_n 2^{-n} \right]$ (9-6)

If $\boxed{R_f = R}$,

$$V_o = -V_R \left[b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots + b_n 2^{-n} \right] \tag{9-7}$$

equation(9-7) indicates analog output which is proportional to the digital input words.

Drawbacks

i) Large range of resistor values are required. Example for 8 bit DAC. we require 2^1R, 2^2R, 2^3R, ..., 2^nR. Therefore, the largest resistor is 128 times the smallest one.

ii) These larger range values of resistor has restriction on higher and lower end. It is impractical to fabricate large value of resistor on integrated circuit (IC).

These drawbacks can be overcome by *R*-2*R* ladder type DAC and is a better choice for practical applications.

2. R-2R ladder type DAC

In *R*-2*R* ladder network DAC, only two values *R* and 2*R* are used. Hence can be used in IC- based applications. The *R*-2R ladder DAC is as shown in Figure 9-4.

Here also, DAC uses shunt resistors for generating n–binary weighted currents. It uses voltage scaling and identical resistors.

Each binary bit connects switch either to ground or to the inverting terminal of the op-amp. Due to virtual ground concept, both the positions of switches are at ground potential and currents through resistances are constant and independent of switch position.

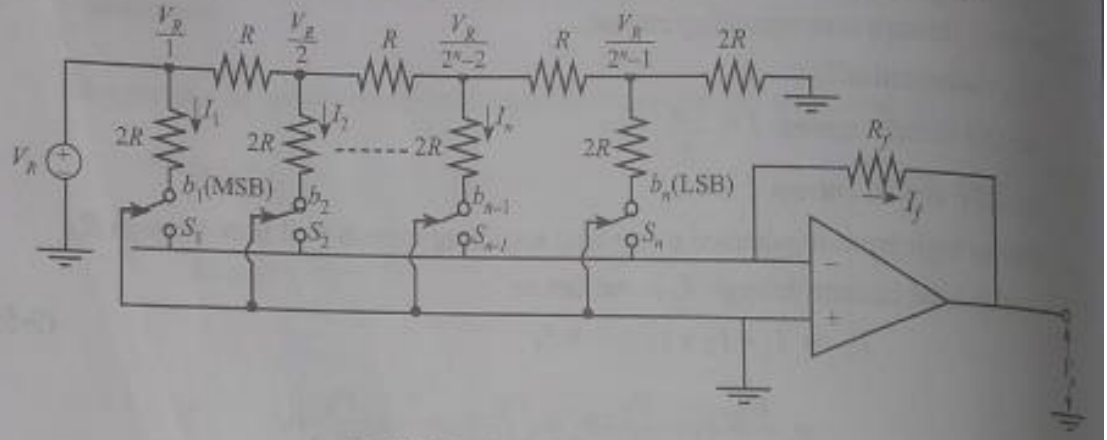


FIGURE 9-4: R-2R ladder type DAC

Now let us write currents flowing through each of these 2*R* resistances

$$I_1 = V_R / 2R$$

$$I_2 = \frac{V_R / 2}{2R} = \frac{V_R}{4R}$$

$$\text{also } I_3 = \frac{V_R / 4}{2R} = \frac{V_R}{8R}$$

$$\text{and } I_n = \frac{V_R / 2^n - 1}{2R}$$

But WKT

$$V_o = -I_f R_f$$

$$V_o = -R_f \left(I_1 + I_2 + \cdots + I_n\right)$$

$$= -R_f \left[\frac{V_R}{2R} b_1 + \frac{V_R}{4R} b_2 + \cdots + \frac{V_R}{2^n R} b_n\right]$$

$$= \frac{-V_R}{R} R_f \left(b_1 2^{-1} + b_2 2^{-2} + \cdots + b_n 2^{-n}\right)$$

When $R_f = R$ V_o can be

$$V_o = -V_R \left(b_1 2^{-1} + b_2 2^{-2} + \cdots + b_n 2^{-n}\right) \quad (9\text{-}8)$$

This V_o expression indicates that the DAC works on the principle of summing i.e., output (V_o) of DAC is analog and is proportional to digital inputs.

Advantages of R-2R DAC

i) As it uses only two types of resistors helps in fabrication and accurate value of *R-2R* can be designed.

ii) Binary input length can be increased by adding more *R-2R* sections

iii) Node voltages remain constant with changing binary input in inverted *R-2R* DAC. This helps in avoiding slow down effect by stray capacitance.

5. (a) Explain the working of a 3-bit Flash type ADC.

Answer:

a) **Flash (Comparator) type ADC:**

This is also called parallel comparator A to D converter. It is simple, fastest and most expensive conversion technique. The Figure 9-7 shows diagram of 3 bit flash A to D converter. The circuit here consist of a resistive divider network, 8 op-amp comparators and 3 bit priority encoder [8 line to 3 line encoder]. A single comparator is shown in Figure 9-8. and truth Table 9-1 gives the logical operation of the comparator.

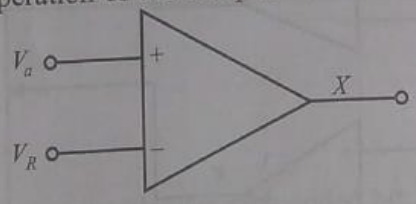


FIGURE 9-6: comparator symbol

TABLE 9-1: Truth table

Input voltage	Logic output (X)
$V_a > V_R$	X = 1
$V_a < V_R$	X = 0
$V_a = V_R$	Previous value

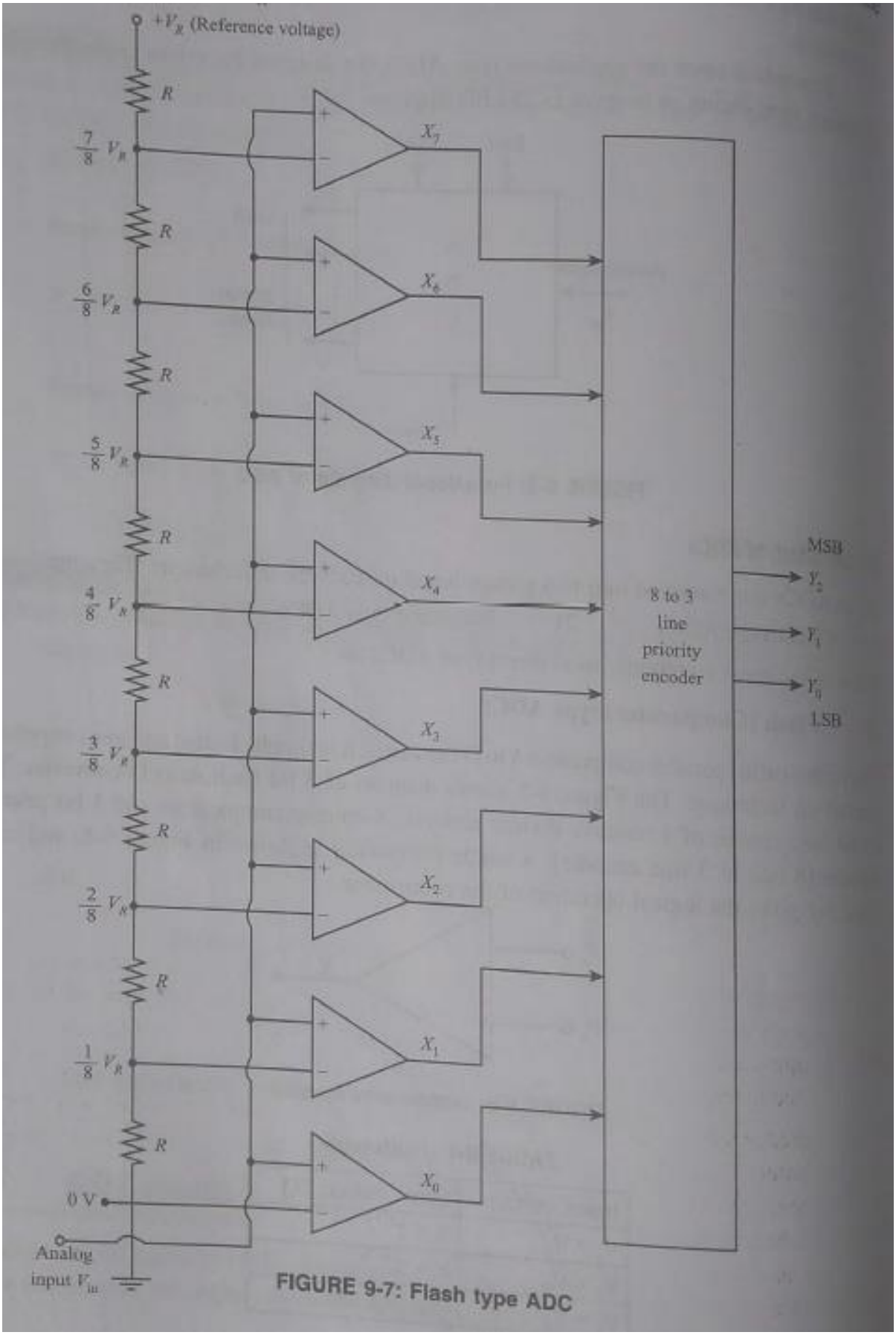


FIGURE 9-7: Flash type ADC

The resistive network is to set to equal reference voltages at each node. The comparator compares set reference value at inverting terminal of op-amp with analog output at non inverting terminal. The truth table for the flash ADC is as shown in Table 9-2.

TABLE 9-2: Truth Table for flash ADC

Input voltage (V_a)	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0 to $\frac{V_R}{8}$	0	0	0	0	0	0	0	1	0	0	0
$\frac{V_R}{8}$ to $\frac{V_R}{4}$	0	0	0	0	0	0	1	1	0	0	1
$\frac{V_R}{4}$ to $\frac{3V_R}{8}$	0	0	0	0	0	1	1	1	0	1	0
$\frac{3V_R}{8}$ to $\frac{V_R}{2}$	0	0	0	0	1	1	1	1	0	1	1
$\frac{V_R}{2}$ to $\frac{5V_R}{8}$	0	0	0	1	1	1	1	1	1	0	0
$\frac{5V_R}{8}$ to $\frac{3V_R}{4}$	0	0	1	1	1	1	1	1	1	0	1
$\frac{3V_R}{4}$ to $\frac{7V_R}{8}$	0	1	1	1	1	1	1	1	1	1	0
$\frac{7V_R}{8}$ to V_R	1	1	1	1	1	1	1	1	1	1	1

(b) A 555 timer is configured to work in the astable mode with a frequency of 2 kHz and duty cycle of 80%. Assuming C=0.1uF, design the circuit.

Answer:

5(b). $f = 2\,kHz$; $D = 80\%$; $C = 0.1\,\mu f$.

$\therefore T = \frac{1}{f} = \frac{1}{2\times10^3} = 0.5ms$

$T = T_{on} + T_{off} = T_c + T_d = 0.5\,ms$

$D = \frac{T_{on}}{T_{on}+T_{off}} = \frac{T_{on}}{T} \Rightarrow 0.8 = \frac{T_{on}}{0.5ms}$

$\Rightarrow T_{on} = 0.4ms$

$\therefore T_{off} = T - T_{on} = 0.5\,ms - 0.4ms = 0.1\,ms$

$T_{on} = 0.693\,(R_a + R_b).\,C$ ——①

$0.4\times10^{-3} = 0.693\,(R_a+R_b)\times0.1\times10^{-6}$ ——①

$T_{off} = 0.693\,R_b.C$

$0.1\times10^{-3} = 0.693\times R_b\times0.1\times10^{-6}$

$\Rightarrow R_b = \frac{0.1\times10^{-3}}{0.693\times0.1\times10^{-6}} = 1.44\times10^3\,\Omega = 1.44k\Omega$

Substituting R_b in eqn ①,

$R_a + R_b = \frac{0.4\times10^{-3}}{0.693\times0.1\times10^{-6}} = 5.77\,k\Omega$

$\Rightarrow R_a = (5.77 - 1.44)\,k\Omega$

$= 4.33\,k\Omega$

6. (a) Explain the working and characteristics of photodiodes.

Answer:

Working Principle:

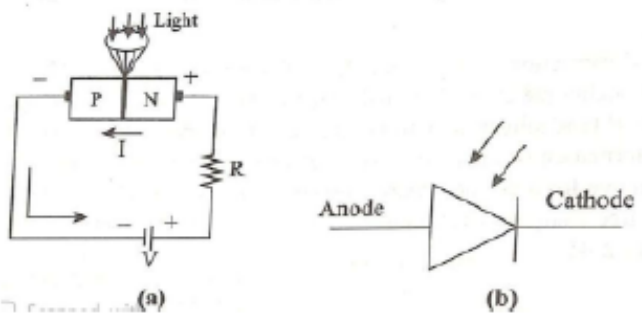
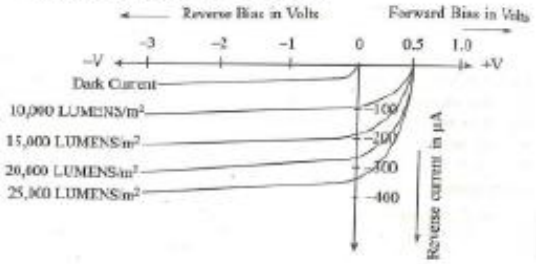


Figure (b) shows the symbol of photodiode.

The junction of photodiode is illuminated by a light source, that is, photons strike the junction surface. These photons impart their energy in the form of light to the junction. Due to this, the electrons present in the valence band get excited and move to the conduction band. This leaves positively charged holes in the valence band, thereby producing electron-hole pairs in the depletion layer. From these electron-hole pairs, electrons get attracted and move towards the positive potential on the cathode and the holes get attracted and move towards the negative potential on the anode. This constitutes a flow of current in a direction opposite to the direction of electron-flow. This current is termed as photocurrent. Thus photodiode converts light energy into electrical energy.

Characteristics of photodiode:



The characteristics are shown in the negative region because the photodiode can be operated only in reverse biased mode. When the photodiode is reverse biased, the width of the depletion layer increases which in turns increases the light gathering ability and thereby the photocurrent.

The current under large reverse bias is given by

$$I = I_{sc} + I_0 (1 - e^{V/\Delta Vt})$$

Where

I_{sc} is the short circuit current,

I_0 is the reverse saturation current in the photodiode,

V is the applied voltage (positive for forward bias and negative for reverse bias),

Vt is the volt equivalent for temperature and

$\Delta = 1$ for Germanium and $\Delta = 2$ for Silicon.

(b) With the help of neat circuit diagrams and mathematical analysis, explain the accurate analysis technique of biasing a voltage divider circuit.

Answer:

ii) Voltage divider bias by accurate analysis:

In accurate analysis, the base current I_B is considered in the analysis of the circuit. The resistor R_1 and R_2 act as a potential divider giving a fixed voltage to the base.

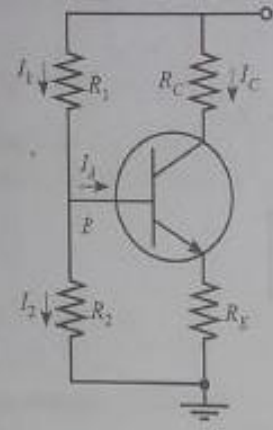


FIGURE 4-9 Voltage divider bias circuit

If I_C increases due to change in temperature change in β, the emitter current I_E also increases and the voltage drop across R_E increases, reducing the voltage difference between base and emitter (V_{BE}). Due to reduction in V_{BE}, I_B and I_C also reduces. Therefore, we can say that negative feedback exists. This reduction in I_B compensates for the original change in I_C. Figure 4-10 shows simplified circuit of voltage divider bias. Here R_1, R_2 are replaced by R_B and V_T, where R_B is the parallel combination of R_1 and R_2 and V_T is the Thevenins voltage.

Thevenins voltage is given by,

$$V_T = \frac{V_{CC} R_2}{R_1 + R_2} \qquad (4\text{-}10)$$

The equivalent resistance of parallel combination of resistors R_1 and R_2 are given by

$$R_T = \frac{R_1 R_2}{R_1 + R_2} \qquad (4\text{-}11)$$

Applying KVL to the base circuit we get,

$$V_T = I_B R_T + V_{BE} + I_E R_E$$

$$= I_B R_T + V_{BE} + (1+\beta) I_B R_E$$

$$I_B = \frac{V_T - V_{BE}}{R_T + (1+\beta) R_E} \qquad (4\text{-}12)$$

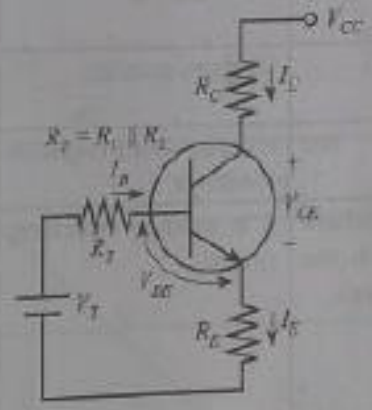


FIGURE 4-10: Thevenins equivalent circuit for voltage divider bias

Equation (4-12) gives the basic current of Thevinines equivalent circuit for voltage divider bias.

Applying KVL to the collector circuit we get,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$\boxed{V_{CE} = V_{CC} - I_C R_C - I_E R_E} \qquad (4\text{-}13)$$

Equation (4-13) gives the collector to emitter voltage of voltage divider bias using accurate analysis.