IAT -3 (ADE)

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SECTION *

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In an SR latch made by cross-coupling two NAND gates, if both S and R inputs are set to 0, then it will result in * 1 point

- ( ) MEMORY State
- ( ) RESET State
- ( ) SET State
- (•) FORBIDDEN State
- ( ) Other:

How is a J-K flip-flop made to toggle? * 1 point

- ○ J = 1, K = 0
- ○ J = 0, K = 0
- ◉ J = 1, K = 1
- ○ J = 0, K = 1

Which statement BEST describes the operation of a negative-edge-triggered D flip-flop? * 2 points

- ◉ The logic level at the D input is transferred to Q on NGT of CLK.
- ○ The Q output is ALWAYS identical to the CLK input if the D input is HIGH.
- ○ The Q output is ALWAYS identical to the D input when CLK = PGT.
- ○ The Q output is ALWAYS identical to the D input.

How many flip-flops are required to produce a divide-by-128 device? * 1 point

- ○ 128
- ○ 64
- ◉ 7
- ○ None of These

On a master-slave flip-flop, when is the master enabled? * 1 point

- (●) When clock is HIGH
- ( ) When clock is LOW
- ( ) Both of the above
- ( ) Neither of the above

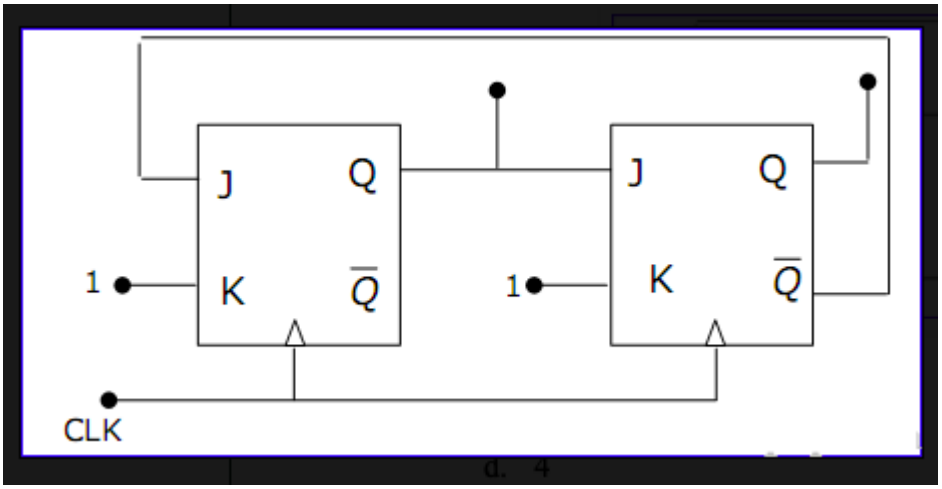
Which of the following is correct for a gated D flip-flop? * 1 point

- ( ) The output toggles if one of the inputs is held HIGH.
- ( ) Only one of the inputs can be HIGH at a time.
- ( ) The output complement follows the input when enabled.
- (●) Q output follows the input D when the enable is HIGH.

A J-K flip-flop is in a "no change" condition when * 1 point

- ( ) J = 1, K = 1
- ( ) J = 1, K = 0
- ( ) J = 0, K = 1
- (●) J = 0, K = 0

The figure shows mod-K counter, where k value is * 2 points



- 1
- 2
- 3
- 4

What is the maximum possible range of bit-count specifically in n-bit binary counter consisting of 'n' number of flip-flops? * 2 points

- 0 to 2^n
- 0 to 2^n + 1
- 0 to 2^n − 1
- 0 to 2^(n+1/2)

A counter circuit is usually constructed of * 1 point

- ○ A number of NOR gates connected in cascade form
- ○ A number of latches connected in cascade form
- ○ A number of NAND gates connected in cascade form
- ◉ A number of flip-flops connected in cascade

Three decade counter would have * 1 point

- ○ 2 BCD counters
- ◉ 3 BCD counters
- ○ 4 BCD counters
- ○ 5 BCD counters

The parallel outputs of a counter circuit represent the * 1 point

- ○ Parallel data word
- ○ Clock frequency
- ○ Counter modulus
- ◉ Clock count

How many flip-flops are required to construct a decade counter? * 1 point

- (●) 4
- ( ) 5
- ( ) 8
- ( ) 10

The terminal count of a typical modulus-10 binary counter is _____ * 2 points

- ( ) 0000
- ( ) 1010
- (●) 1001
- ( ) 1111

A 5-bit asynchronous binary counter is made up of five flip-flops, each with a 12 ns propagation delay. The total propagation delay (tp(total)) is * 2 points

- ( ) 12 ms
- ( ) 24 ns
- ( ) 48 ns
- (●) 60 ns

Three cascaded decade counters will divide the input frequency by * 1 point

- [ ] 0
- [ ] 20
- [ ] 100
- [x] 1000

A 4-bit counter has a maximum modulus of 1 point

- [ ] 3
- [ ] 6
- [ ] 8
- [x] 16

In a 3-bit asynchronous down counter, at the first negative transition of the clock, the counter content becomes * 2 points

- [ ] 000
- [x] 111
- [ ] 101
- [ ] 010

Modulus refers to _____ * 1 point

- [ ] A method used to fabricate decade counter units
- [ ] The modulus of elasticity, or the ability of a circuit to be stretched from one mode to another
- [ ] An input on a counter that is used to set the counter state, such as UP/DOWN
- [x] The maximum number of states in a counter sequence

The minimum number of flip-flops that can be used to construct a modulus-5 counter is 1 point

- [x] 3
- [ ] 8
- [ ] 5
- [ ] 10

What is state diagram? * 1 point

- [ ] It provides the graphical representation of states
- [x] It provides exactly the same information as the state table
- [ ] It is same as the truth table
- [ ] It is similar to the characteristic equation

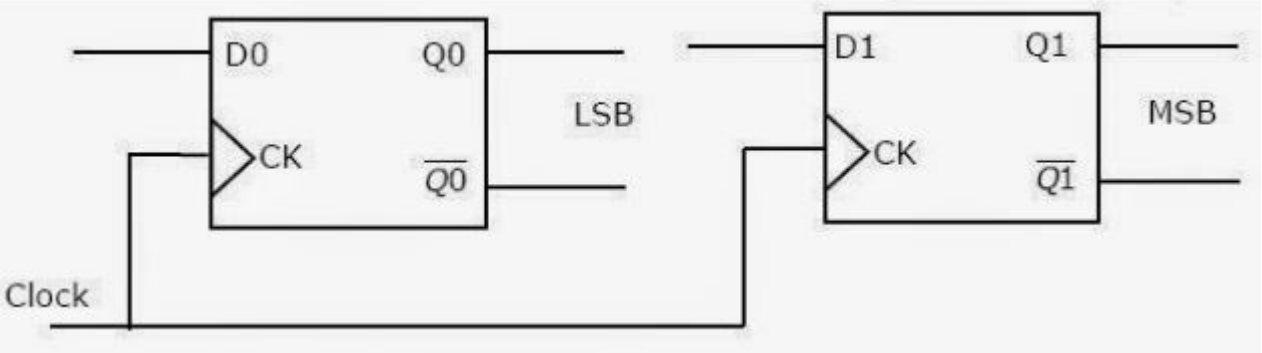
In mealy machine, the O/P depends upon? * 2 points

- ○ Present States of FlipFlops
- ○ Previous State of FlipFlops
- ◉ Present States of FlipFlops and Input Sequence
- ○ Only Input Sequence

The major difference between Mealy and Moore machine is about: * 1 point

- ◉ Output Variations
- ○ Input Variations
- ○ Both
- ○ None of the mentioned

Two D flipflops are to connected as a synchronous counter as shown below, that goes through the following Q1Q0 sequence 00->01->10->11->00->..... The inputs D0 and D1 should be connected as * 4 points

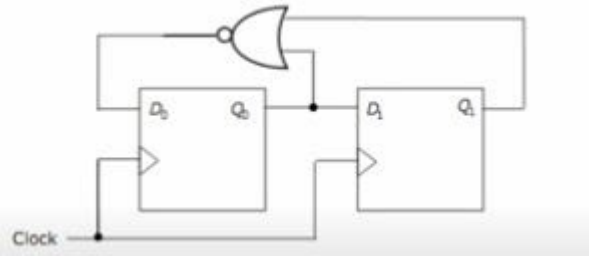


- Q1' & Q0
- Q1'Q0 & Q1Q0'
- Q1'Q0' & Q1Q0
- Q0' & Q0⊕Q1

Consider a 4 bit Johnson counter with an initial value of 0000. The counting sequence of this counter is: * 2 points

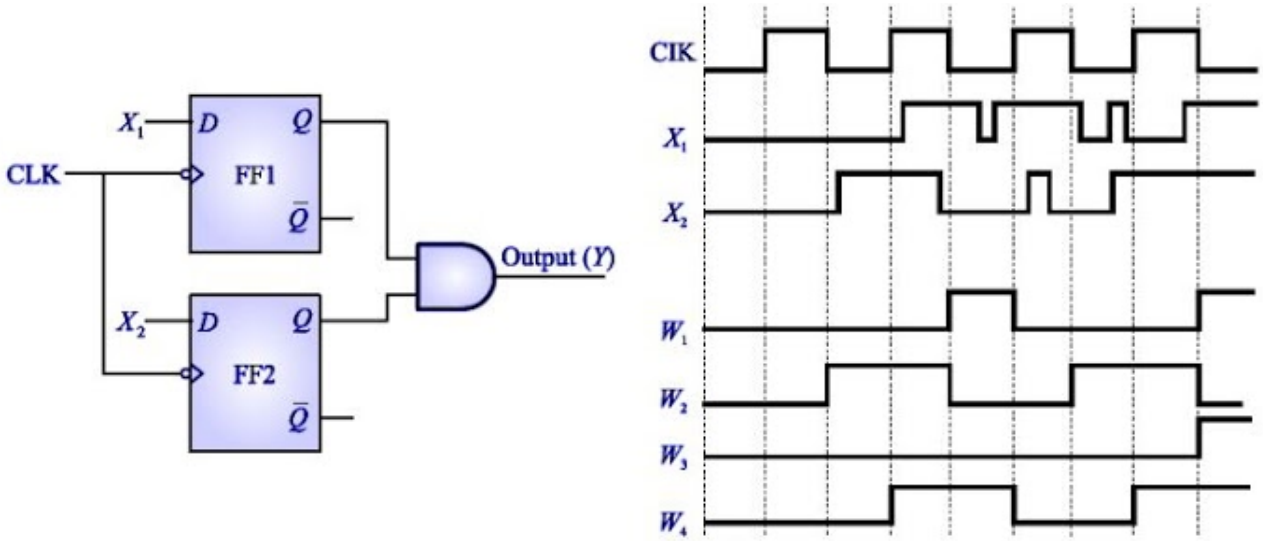
- 0, 1, 3, 7, 15, 14, 12, 8, 0
- 0, 1, 3, 5, 7, 9, 11, 13, 15, 0
- 0, 2, 4, 6, 8, 10, 12, 14, 0
- 0, 8, 12, 14, 15, 7, 3, 1, 0

For the circuit shown, the counter state (Q0Q1) follows the sequence * 3 points



- 00,01,10,11,00
- 00,01,10,00,01
- 00,01,11,00,01
- 00,10,11,00,10

The circuit shown choose the correct timing diagram for the o/p Y from the given waveforms. * 2 points

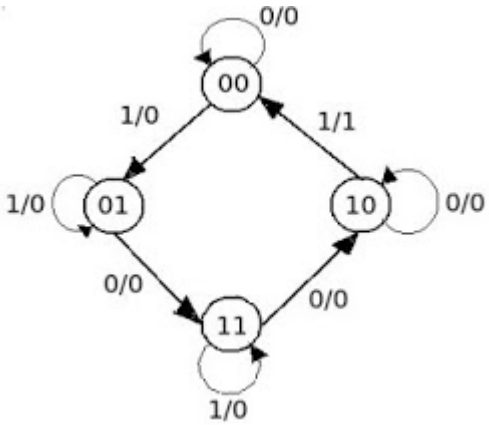


- W1
- W2
- W3
- W4

The number of flipflops required to construct a 8 bit shift register is * 1 point

- 4
- 8
- 16
- 32

In the below drawn schematic, what does an arrow between the circles indicate? * 1 point



- ( ) Present state
- ( ) Next state
- (•) State transition
- ( ) Don't care condition

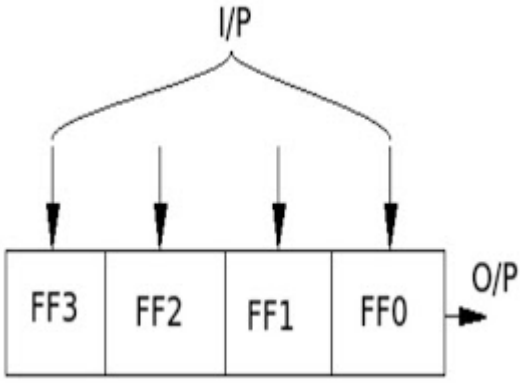
On the second falling edge of clock in ring counter, if the generated output of second clock pulse is ' 0100', what will be the output after the fourth clock pulse? * 1 point

- ( ) 1000
- (•) 0001
- ( ) 0010
- ( ) 0000

For a ring counter, the number of output states are always equal to _____ * 1 point

- ○ Number of input states
- ○ Number of clock pulses
- ○ Number of registers
- ◉ Number of flip flops

Referring to the diagram, if all inputs are loaded simultaneously and output is loaded bit by bit, then what will be the mode of operation for a shift register? * 1 point



- ○ Serial Input Serial Output (SISO)
- ○ Serial Input Parallel Output (SIPO)
- ◉ Parallel Input Serial Output (PISO)
- ○ Parallel Input Parallel Output (PIPO)

A counter is fundamentally a _____ sequential circuit that proceeds through the predetermined sequence of states only when input pulses are applied to it. * 1 point

- (●) register
- ( ) memory unit
- ( ) flipflop
- ( ) arithmatic logic unit

Match the following sequential Circuits with associated functions * 3 points

	Storage of Program & data in a digital computer	Generation of timing variables to sequence the digital system operations	Design of Sequential Circuits
Counter	( )	(●)	( )
Register	( )	( )	(●)
Memory	(●)	( )	( )

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