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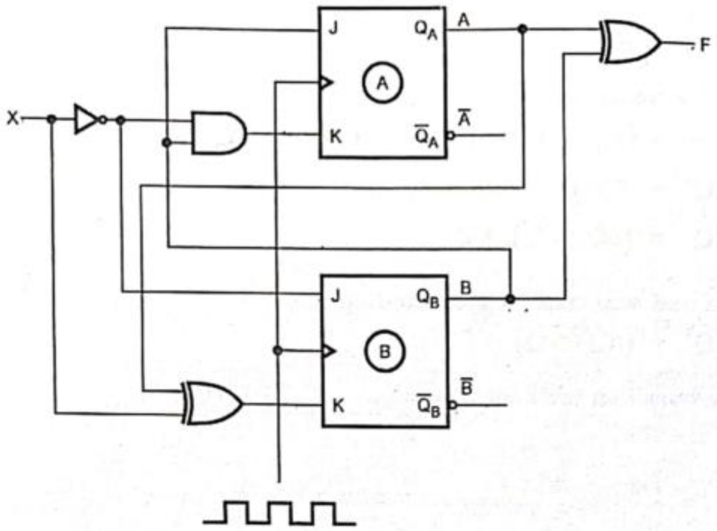
Internal Assesment Test – 3

Sub: Digital System Design				Code: 18EE35
Date: 12/12/2020	Duration: 90 mins	Max Marks: 50	Sem: 3	Sections: A&B

Answer **ANY FIVE** full questions. Explain your notations explicitly and clearly. Sketch figures wherever necessary. Good luck!

		Marks	OBE	
			CO	RBT
Q1.	With a neat logic diagram, explain the different modes of operation of universal shift register.	[10]	CO4	L3
Q2.	Design a 4-bit MOD-8 Johnson Counter. Also write the count sequence table and timing diagram.	[10]	CO4	L3
Q3.	Design and implement a divide by 10 asynchronous counter using T-FFs.	[10]	CO4	L3
Q4.	Design MOD-6 synchronous up counter using D flip-flop.	[10]	CO4	L3
Q5.	Design a synchronous counter to count the sequence 0, 1, 4, 6, 7, 5 and repeat using positive edge triggered JK flip-flops.	[10]	CO4	L3
Q6.	Construct the excitation table, transition table, state table and state diagram for the Moore sequential circuit as shown. 	[10]	CO5	L3
Q7.	With the help of block diagram explain the Mealy and Moore model in sequential circuit analysis. Give example circuits.	[10]	CO5	L2

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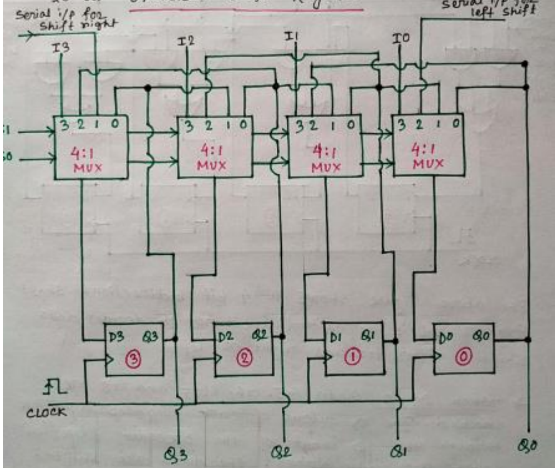
Solution

		Marks	OBE	
			CO	RBT
Q1.	With a neat logic diagram, explain the different modes of operation of universal shift register.	[10]	CO4	L3

⇒ If a Register has both left shift and right shift and also parallel load capabilities, it is referred to as Universal shift Register.



I3, I2, I1, I0 ⟶ parallel inputs
Q3, Q2, Q1, Q0 ⟶ parallel outputs

→ It consists of 4 flip flops and 4 Multiplexers. The four Multiplexers have two common select inputs S1 and S0. and they select appropriate input for D flip-flop. The below table shows the register operation depending on the select lines of multiplexer.

Mode control		Register Operation
S1	S0	
0	0	No change
0	1	Shift Right
1	0	Shift Left
1	1	parallel Load

→ When S1 S0 = 00, input 0 is selected and the present value of the register is applied to the D inputs of the flip-flops. This results no change in Register value.

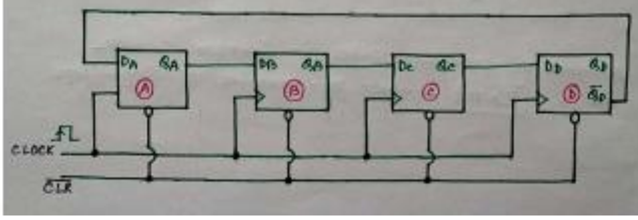
→ When S1 S0 = 01, input 1 is selected and circuit connections are such that it operates as a right shift Register.

→ When S1 S0 = 10, input 2 is selected and circuit connections are such that it operates as a left shift Register.

→ Finally when S1 S0 = 11, the binary information on the parallel input lines is transfered into the register simultaneously and it is a parallel load operation.

		Marks	CO	RBT
Q2.	Design a 4-bit MOD-8 Johnson Counter. Also write the count sequence table and timing diagram.	[10]	CO4	L3

In a Johnson Counter, the Q output of each stage is connected to the D input of the next stage. The single exception is that the complement output of the last flipflop is connected back to the D input of the first flip-flop.

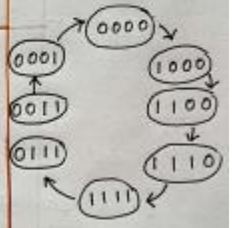


→ Let us consider, Initially all the flip flops are cleared. So, $Q_A Q_B Q_C Q_D = 0000$. The output of last stage, $Q_D = 0$. Therefore complement o/p of last stage, $\bar{Q}_D = 1$. This is connected back to the D input of first stage. So, $D_A = 1$.

→ The 1st positive edge of clock pulse produces $Q_A = 1$ and $Q_B = 0$, $Q_C = 0$, $Q_D = 0$. since D_B, D_C, D_D are zero.

→ The next clock pulse produces $Q_A = 1$, $Q_B = 1$, $Q_C = 0$ and $Q_D = 0$. The sequence of states is summarized in the below Table :-

CLOCK	Q_A	Q_B	Q_C	Q_D
—	0	0	0	0
1↑	1	0	0	0
2↑	1	1	0	0
3↑	1	1	1	0
4↑	1	1	1	1
5↑	0	1	1	1
6↑	0	0	1	1
7↑	0	0	0	1
8↑	0	0	0	0



Number of possible states in Johnson Counter is - $2 \times n$ where n = number of flip-flops.

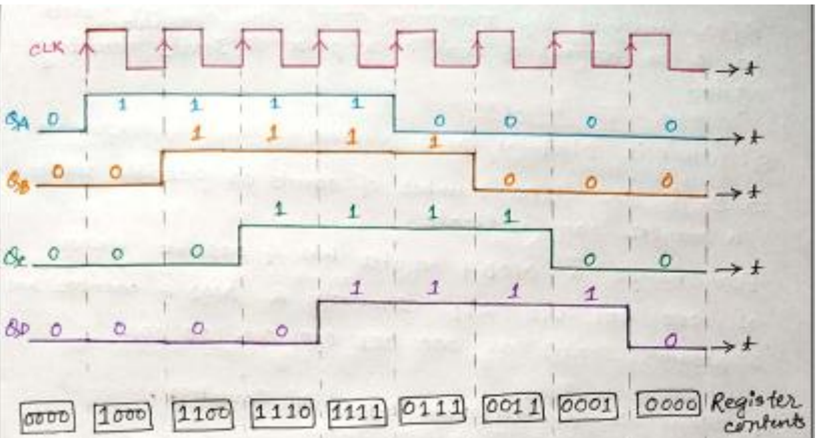


Fig:- Timing Diagram for Johnson Counter

Q3.	Design and implement a divide by 10 asynchronous counter using T-FFs.	[10]	CO4	L3

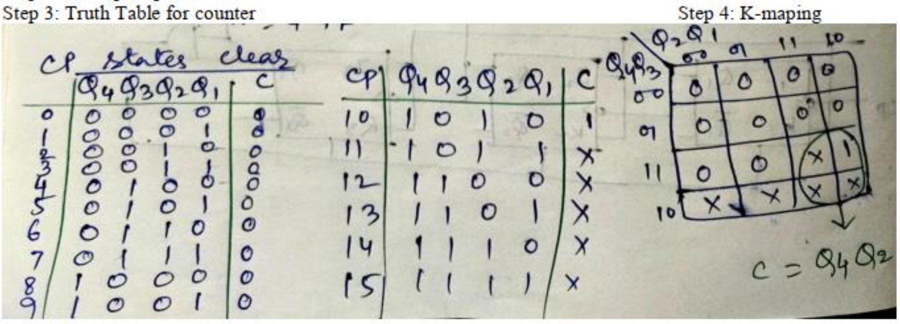
Step1:

- No. of valid states: 10 (0-9). At 10th clock pulse output will be temporarily 1010 but immediately every flip-flops will be cleared to zero and clear input will be activated (1). 11^{th} -15^{th} states will be invalid.
- No. of flip-flops: $2^n >= N$, if n=4, then the condition, 16>=10 (N=10) will be valid.
- No. of sequence states total: 16 (0-15).
- No. of clock pulse: 16.

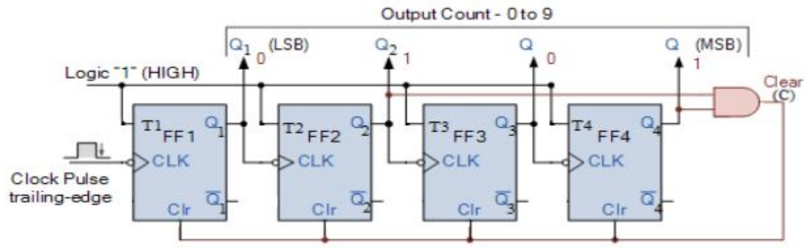
Step 2: JK Flip-flop

Step 3: Truth Table for counter

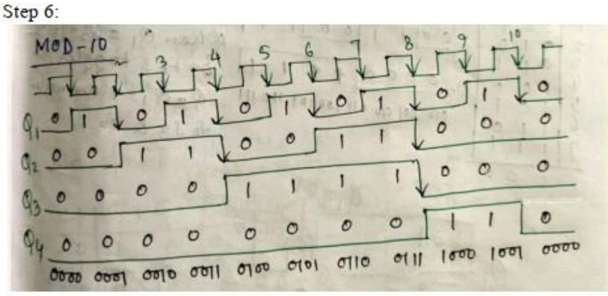
Step 4: K-maping

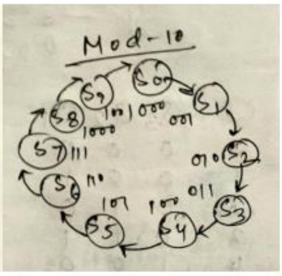


CP	Q_4	Q_3	Q_2	Q_1	C
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	0
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	0
9	1	0	0	1	0
10	1	0	1	0	1
11	1	0	1	1	X
12	1	1	0	0	X
13	1	1	0	1	X
14	1	1	1	0	X
15	1	1	1	1	X



Step 6:





Q4. Design MOD-6 synchronous up counter using D flip-flop. [10] CO4 L3

Step 1 : Find number of flip-flops required to build the counter.

Flip-flops required are : $2^n \geq N$

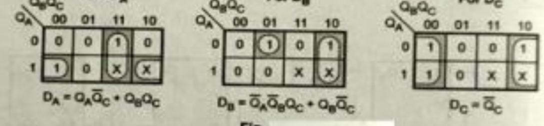
Here N = 6 ∴ n = 3

i.e. three flip-flops are required.

Step 2 : Determine the transition table.

Present state			Next state		
Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	0	0	0
1	1	0	x	x	x
1	1	1	x	x	x

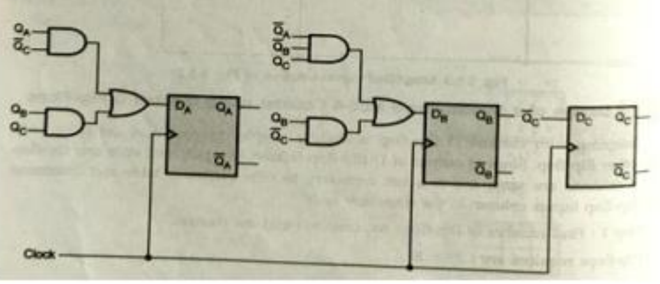
Step 3 : K-map simplification for flip-flop inputs.



$D_A = Q_A\bar{Q}_C + Q_BQ_C$ $D_B = \bar{Q}_A\bar{Q}_BQ_C + Q_B\bar{Q}_C$ $D_C = \bar{Q}_C$

Fig.

Step 4 : Implement the counter



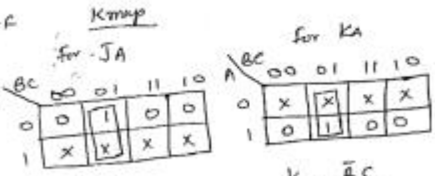
Q5. Design a synchronous counter to count the sequence 0, 1, 4, 6, 7, 5 and repeat using positive edge triggered JK flip-flops. [10] CO4 L3

Present State			Next State			Flip Flop Inputs					
A	B	C	A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	x	0	x	1	x
0	0	1	1	0	0	1	x	0	x	x	1
0	1	0	0	0	0	0	x	x	1	0	x
0	1	1	0	0	0	0	x	x	1	x	1
1	0	0	1	1	0	x	0	1	x	0	x
1	0	1	0	0	0	x	1	0	x	x	1
1	1	0	1	1	1	x	0	x	0	1	x
1	1	1	1	0	1	x	0	x	1	x	0

Excitation table for JKFF

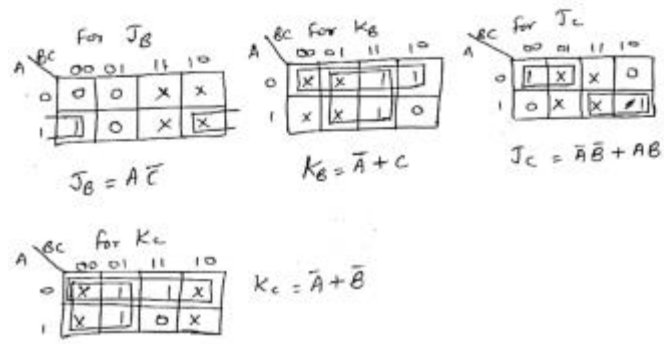
Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Kmap



$J_A = \bar{B}C$

$K_A = \bar{B}C$

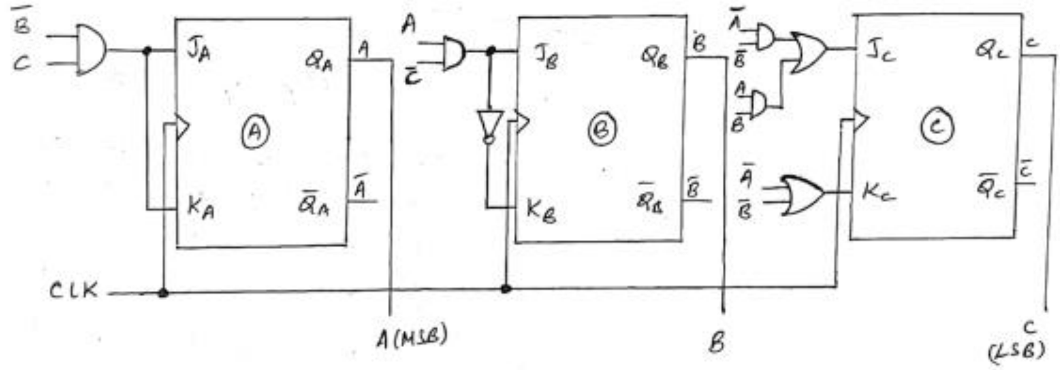


$J_B = A\bar{C}$

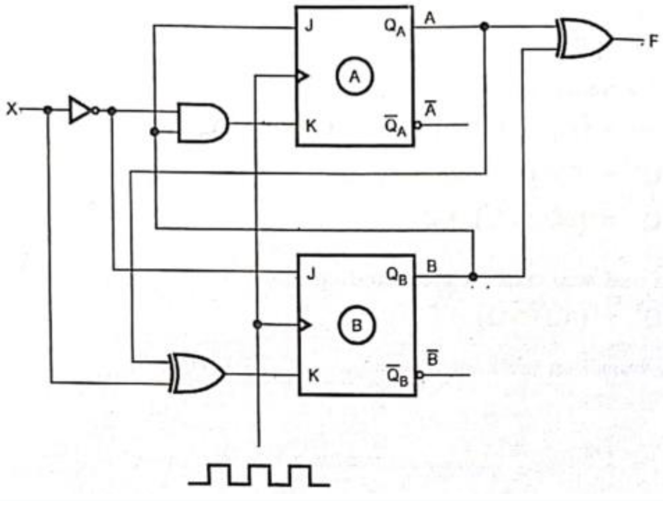
$K_B = \bar{A} + C$

$J_C = \bar{A}\bar{B} + AB$

$K_C = \bar{A} + \bar{B}$



Q6. Construct the excitation table, transition table, state table and state diagram for the Moore sequential circuit as shown. [10] CO5 L3



1. Determine the flip-flop input equations and the output equations from the sequential circuit.

$$F = A \oplus B$$

$$J_A = B \qquad K_A = \overline{X}B$$

$$J_B = \overline{X} \qquad K_B = X \oplus A$$

2. Derive the transition equations.

The transition equations for JK flip-flops can be derived from the characteristic equation of JK flip-flop as follows :

We know that for JK flop-flop

$$Q^+ = J\overline{Q} + \overline{K}Q$$

$$\therefore A^+ = Q_A^+ = J_A\overline{Q}_A + \overline{K}_A Q_A = B\overline{Q}_A + \overline{\overline{X}B}Q_A = B\overline{Q}_A + (X+\overline{B})\,Q_A$$

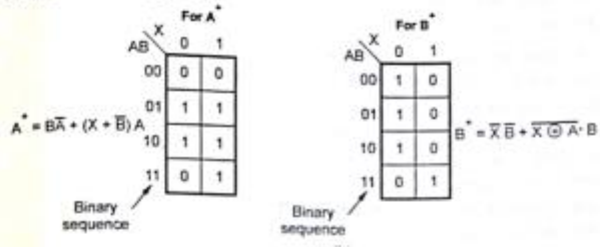
$$= B\overline{A} + (X+\overline{B})\,A$$

and $$B^+ = Q_B^+ = J_B\overline{Q}_B + \overline{K}_B Q_B = \overline{X}\,\overline{Q}_B + \overline{X \oplus A}\,Q_B$$

$$= \overline{X}\,\overline{B} + \overline{X \oplus A}\cdot B$$

3. Plot a next-state maps for each flip-flop.

The next-state maps are :



4. Plot the transition table.

The transition table can be formed by combining the above two maps. The Table 6.3.3 shows the transition table.

Present state		Next state				Output
		X = 0		X = 1		
A	B	A^+	B^+	A^+	B^+	$F = (A \oplus B)$
0	0	0	1	0	0	0
0	1	1	1	1	0	1
1	0	1	1	1	0	1
1	1	0	0	1	1	0

Note : For Moore sequential circuit output only depends on present state and not on the input.

5. Draw the state table

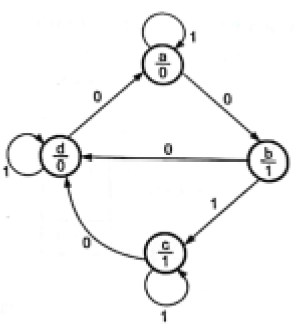
By assigning a = 0 0, b = 01, c = 10 and d = 11 we can write state table from the transition table as shown.

Present state	Next state		Output
A B	X = 0	X = 1	F
	A^+B^+	A^+B^+	
a	b	a	0
b	d	c	1
c	d	c	1
d	a	d	0

6. Draw state diagram

From the state table we can draw state diagram as shown

Note : In case of Moore model, the directed lines are labelled with only one binary number representing the state of the input that causes the state transition. The output state is indicated within the circle, below the present state because output state depends only on present state and not on the input.



Q7.	With the help of block diagram explain the Mealy and Moore model in sequential circuit analysis. Give example circuits.	[10]	CO5	L2

The synchronous or clocked sequential circuits are represented by two models.

- **Moore model :** The output depends only on the present state of the flip-flops.
- **Mealy model :** The output depends on both the present state of the flip-flop(s) and on the input (s).

Moore Model

As mentioned earlier, when the output of the sequential circuit depends only on the present state of the flip-flop, the sequential circuit is referred to as **Moore model.** Let us see one example of Moore model. Fig. shows a sequential circuit which consists of two JK flip-flops and AND gate. The circuit has one input X and one output Y.

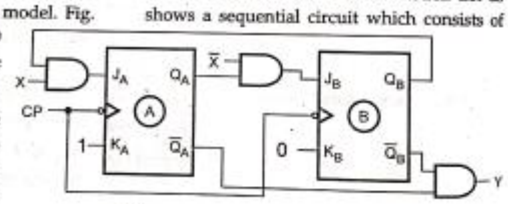
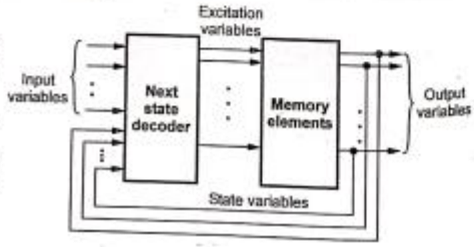


Fig.

As shown in the Fig. input is used to determine the inputs of the flip-flops. It is not used to determine the output. The output is derived using only present states of the flip-flops or combination of it (in this case $Y = Q_A Q_B$).

In general form the Moore model can be represented with its block schematic as shown



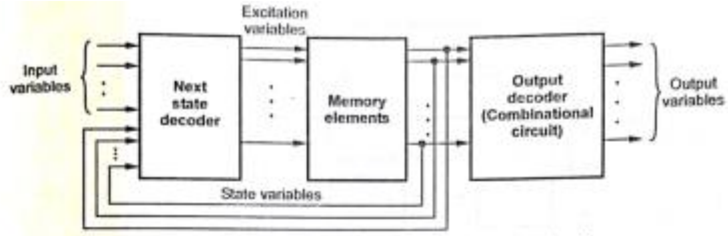


Fig. Moore circuit model with an output decoder

In the Moore model, as output depends only on present state of flip-flops, it appears only after the clock pulse is applied, i.e. it varies in synchronism with the clock input.

Mealy Model

When the output of the sequential circuit depends on both the present state of flip-flop(s) and on the input(s), the sequential circuit is referred to as **Mealy model.** Fig. shows the sample Mealy model. As shown in the Fig. the output of the circuit is derived from the combination of present state of flip-flops and input (s) of the circuit.

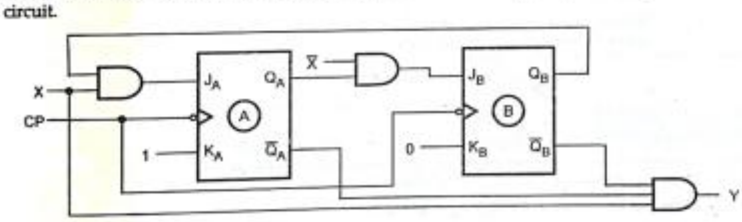


Fig. Example of Mealy model

Looking at Fig. 6.1.3, we can easily realize that, changes in the input within the clock pulses can not affect the state of the flip-flop. However, they can affect the output of the circuit. Due to this, if the input variations are not synchronized with the clock, the derived output will also not be synchronized with the clock and we get false output (as it is a synchronous sequential circuit). The false outputs can be eliminated by allowing input to change only at the active transition of the clock (in our example HIGH-to-LOW). In general form the Mealy model can be represented with its block schematic as shown