CBCS SCHEME

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18EC42

Fourth Semester B.E. Degree Examination, Jan./Feb. 2021
Analog Circuits

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. What is meant by biasing? Explain the need for biasing and the stability of Q-point with respect to BJT. **(04 Marks)**

b. Design a voltage divider bias network to operate a BJT at $V_{CE} = 6$ V and $I_C = 4$ mA. Use $V_{CC} = 12$ V, $V_E = V_{CC}/4$ and the current through the voltage-divider resistors as $I_E/10$. Assume $\beta = 100$ and $V_{BE} = 0.7$ V. **(08 Marks)**

c. For a BJT amplifier circuit, obtain the expressions for small-signal collector current, transconductance and voltage gain. **(08 Marks)**

OR

2 a. A MOSFET having $V_t = 1.5$ V, $W = 10$ μm, $L = 1$ μm, $K'_n = 200$ μA/V^2 and $\lambda = 0$ has to be biased at $I_D = 5$ mA. Design a drain-to-gate feedback bias network using $V_{DD} = 10$ V. **(08 Marks)**

b. For the circuit shown in Fig.Q2(b), determine the small-signal voltage gain, input resistance and output resistance. Assume $V_t = 1.5$ V, $K'_n W/L = 0.25$ mA/V^2 and $V_A = 50$ V.

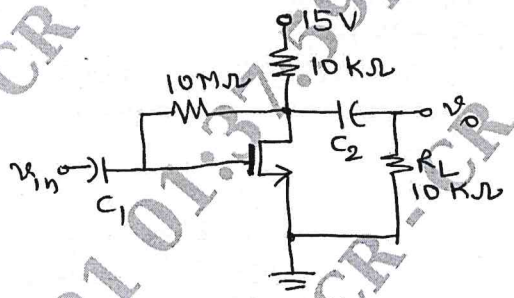

Fig.Q2(b) **(12 Marks)**

Module-2

3 a. Define the terms input resistance, output resistance, voltage gain and overall voltage gain of an amplifier. **(04 Marks)**

b. Analyze the circuit of common-drain amplifier, and derive the expressions for no-load voltage gain, overall voltage gain, input resistance and output resistance. **(10 Marks)**

c. An n-channel MOSFET has $t_{ox} = 10$ nm, $w = 10$ μm, $L = 1$ μm and $L_{ov} = 0.05$ μm. calculate the values of C_{ox}, C_{gs} and C_{gd} when the transistor is operating in its saturation region. Assume $\epsilon_{ox} = 34.53$ pF/m. **(06 Marks)**

OR

4 a. Draw the high-frequency model of MOSFET used in computer analysis, and the simplified model used in manual analysis. **(04 Marks)**

b. A common-source amplifier has signal resistance $R_{sig} = 10$ KΩ, gate resistance $R_G = 10$ MΩ, drain resistance $R_D = 15$ KΩ, load $R_L = 15$ KΩ, $r_0 = 150$ KΩ, $g_m = 10$ mA/V, $C_{gs} = 1$ pF, $C_{gd} = 0.4$ pF, coupling capacitor $C_1 = C_2 = 1$ μF and bypass capacitor $C_s = 1$ μF. Determine the maximum gain in dB and bandwidth of the amplifier. **(08 Marks)**

c. Draw the circuit of MOSFET based RC phase-shift oscillator and explain its operation. **(08 Marks)**

Module-3

5 a. List the advantages of negative feedback in amplifiers. **(04 Marks)**

b. An amplifier has open-loop gain A = 10,000. Find the feedback factor β required to get the closed-loop gain A_F = 10, Now if A decreases by 20%, determine the corresponding decrease in A_F. **(06 Marks)**

c. Draw the diagram of series-series feedback amplifier (trans-conductance amplifier) and derive the expressions for closed-loop voltage gain, input resistance and output resistance. **(10 Marks)**

OR

6 a. Define a power amplifier. Classify power amplifiers based on the location of Q-point, conduction angle, efficiency and applications. **(08 Marks)**

b. What is cross-over distortion? How can it be eliminated? **(04 Marks)**

c. A complementary symmetry push-pull amplifier is operated using V_{CC} = 10 V to deliver power to a load R_L = 5 Ω. Calculate the maximum power output and the power ratings of the transistors. **(08 Marks)**

Module-4

7 a. Draw the circuit of non-inverting amplifier and derive the expressions for exact gain, ideal gain, input resistance and output resistance. **(10 Marks)**

b. What is meant by virtual ground? Explain. **(04 Marks)**

c. An inverting amplifier with feedback resistor R_f = 4.7 KΩ and the input resistor R_1= 1 KΩ is fed with 5V peak-to-peak sinusoidal of frequency 1 kHz. Draw the input and output waveforms. **(06 Marks)**

OR

8 a. Design an op-amp circuit with three input voltage V_1, V_2 and V_3 such that to get an output of $V_0 = -(0.5V_1 + V_2 + 2V_3)$. **(08 Marks)**

b. What is meant by offset-nulling? How is it done in 741C op-amp? **(04 Marks)**

c. Determine the bandwidth of the amplifier shown in Fig.Q8(c) if the unity-gain bandwidth of the op-amp is 1 MHz.

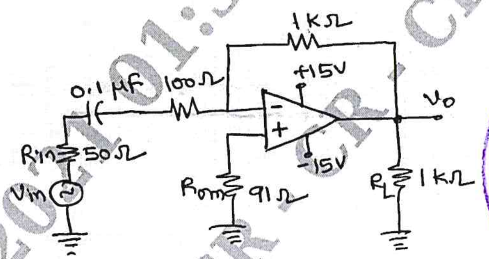

Fig.Q8(c) **(08 Marks)**

Module-5

9 a. With circuit diagram and waveform, explain the working of binary-weighted resistors 4-bit digital-to-analog converter. **(08 Marks)**

b. In a R-2R Digital-to-Analog converter, R_f= 12 KΩ, R = 5 KΩ, calculate the output voltage when only the LSB is ON, and the output voltage when all the four bits are ON. Assume reference voltage is +5V. **(04 Marks)**

c. Explain the working of positive half-wave precision rectifier using op-amp and a single diode. **(08 Marks)**

OR

10 a. A second-order low-pass filter is to be designed to have cutoff frequency 1.6 kHz and passband gain 1.586. Design and draw the circuit. **(07 Marks)**

b. Draw the circuit of first order wide band-pass filter and explain operation. **(08 Marks)**

c. Design a circuit using 555 timer to get a mono-shot pulse of width 10 ms. Choose C = 1 μF. **(05 Marks)**