CBCS SCHEME

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18EC35

Third Semester B.E. Degree Examination, Jan./Feb. 2021
Computer Organization and Architecture

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. Write neat diagrams wherever necessary.

Module-1

1 a. With a neat diagram, describe the functional units of a computer. Give few examples for I/O devices. **(06 Marks)**

b. Discuss IEEE standard for single-precision and double-precision floating point numbers, with standard notations. **(06 Marks)**

c. Develop an Assembly Language Program (ALP) for the expression $Y = Ax^2 + BCx + D$ using 3-address, 2-address and 1-address instruction formats. Assume A, B, C, D, Y as memory locations and x as immediate data. **(08 Marks)**

OR

2 a. With a neat diagram, discuss the operational concepts in a computer highlighting the role of PC, MAR, MDR and IR. **(08 Marks)**

b. Perform subtraction on the following pairs of numbers using 5-bit signed 2's-complement format. Indicate about overflow in each case:
i) +10 and -8 ii) +12 and +9 iii) -15 and -9 iv) -14 and +5 **(08 Marks)**

c. Distinguish between Big-endian and little-endian memory assignment. With a neat sketch, show how the number 26789435 is stored using these methods. **(04 Marks)**

Module-2

3 a. Define addressing mode. Explain any four basic addressing modes with syntax and examples. **(08 Marks)**

b. What is subroutine? With a pseudocode or program segment, illustrate parameter passing using registers. **(06 Marks)**

c. Consider a database of marks scored by students in 3 tests, stored in memory starting at address LIST. Each student record consists of studentID followed by marks in 3 tests. Assume each of these to be 4 bytes in size. There are 50 students in the class and this value is stored at location NUM.
i) Sketch the memory map showing all details
ii) Develop an ALP using Indexed Addressing mode, to compute the sum of scores by all the students in Test2 and store the result in location SUM. Write appropriate comments. **(06 Marks)**

OR

4 a. Discuss Auto-increment and Auto-decrement addressing modes with syntax. Consider a set of numbers (each 4 bytes in size) stored in memory starting at address TABLE. Total numbers are N and this value is stored at location LOCN.
i) Sketch the memory map showing all details
ii) Develop an ALP using Auto-increment addressing mode, to compute the sum of all numbers and store the result at memory address RESUTL. Write appropriate comments. **(08 Marks)**

b. Define stack. Explain PUSH and POP operations on stack with neat sketches and examples. **(06 Marks)**

c. Consider a register R1 to size 16-bits with initial data 5867_d. With neat sketches, depict the output in each case, after performing the following operations:
i) LshiftL #2, R1 ii) AshiftR #1, R1 iii) RotateR #1, R1
Note: For each operation, R1 value is to be taken as 5867_d and carry flag is indicated cleared. **(06 Marks)**

Module-3

5 a. Distinguish between memory mapped I/O and standard I/O. Write a program segment to read a line of text from keyboard and display it. **(08 Marks)**

b. What is interrupt priority? Why is it necessary? With relevant diagram, discuss daisy-chain method of handling multiple interrupt requests. **(06 Marks)**

c. Explain distributed arbitration mechanism in DMA with a neat diagram. **(06 Marks)**

OR

6 a. With a neat diagram, discuss implementation of interrupt priority using individual request and acknowledge lines. **(06 Marks)**

b. Briefly explain: i) Vectored interrupts and ii) Registers in a DMA interface. **(06 Marks)**

c. Explain centralized arbitration mechanism in DMA with a neat sketch and timing diagram. **(08 Marks)**

Module-4

7 a. Classify memory in a computer. With a neat diagram, describe the organization of 2M × 8 DRAM chip. **(08 Marks)**

b. What is cache memory? Explain direct mapping technique with a neat diagram. **(08 Marks)**

c. Briefly discuss the concept of virtual memory with a diagram. **(04 Marks)**

OR

8 a. Briefly explain the working of 1-bit CMOS SRAM cell with a schematic. **(06 Marks)**

b. What is mapping function? Explain set-associative cache mapping technique with a relevant diagram. **(08 Marks)**

c. With a neat diagram, explain the principle of working of magnetic disk. **(06 Marks)**

Module-5

9 a. Explain single-bus organization of data path in a processor with a neat diagram. Highlight the importance of gating signals. **(08 Marks)**

b. Develop the complete control signal sequence for the instruction Add (R1), R3 with appropriate remarks. **(06 Marks)**

c. Discuss micro programmed control unit design with relevant diagrams. **(06 Marks)**

OR

10 a. List different ways of improving CPU performance. With a neat diagram, discuss three-bus organization of CPU. Compare the performance with single-bus organization. **(08 Marks)**

b. Discuss Hardwired control unit organization with relevant diagrams and illustrate the logic to generate Z_{in} control signal. **(08 Marks)**

c. Define the following:
i) Gating signal ii) Control word iii) Microroutine iv) Control store. **(04 Marks)**

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