

CBCS SCHEME

18CS33



Third Semester B.E. Degree Examination, Jan./Feb. 2021 Analog and Digital Electronics

Time: 3 hrs

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- Explain the working principle of opto coupler with neat diagram. (06 Marks)
 - Derive an expression for collector current and collector emitter voltage of fixed bias circuit. (06 Marks)
 - For the circuit shown in Fig.Q.1(c), draw DC load line, use silicon transistor with $B = 50$, $V_{BE} = 0.7V$. (08 Marks)

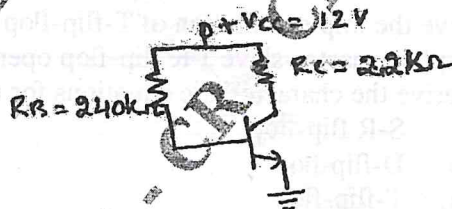


Fig.Q.1(c)

OR

- With the help of neat circuit diagram and wave form explain the working principle of relaxation oscillator. (10 Marks)
 - Explain current to voltage converter. (05 Marks)
 - Define voltage regulator. Explain adjustable voltage regulator. (05 Marks)

Module-2

- Simplify the following function using K-map and obtain simplified Boolean expressions.
 - $f_1(a, b, c, d) = \sum m(1, 3, 4, 5, 7, 10, 12)$
 - $f_2(a, b, c, d) = \sum m(5, 8, 9, 10, 11, 12, 13, 14, 15)$ (10 Marks)
 - Find all the prime implicants of function using Q-M method.
 $f(a, b, c, d) = \sum m(0, 2, 3, 4, 8, 10, 12, 13, 14)$ (10 Marks)

OR

- For the following function given use Q-M method and obtain simplified expression:
 $f(a, b, c, d) = \sum m(7, 9, 12, 13, 14, 15) + dc(4, 11)$ (08 Marks)
 - With an example explain Petrik's method. (06 Marks)
 - For the given function determine minimal sum using MEV technique. Use d as MEV variable. $f(a, b, c, d) = \sum m(3, 4, 5, 7, 8, 11, 12, 13, 15)$. (06 Marks)

Module-3

- Define static 1 – hazard. Explain how static 1-hazard can be detected and removed with an example. (08 Marks)
 - What is multiplexer and explain 8 to 1 mux with the help of logic diagram and corresponding expression. (06 Marks)
 - Explain the importance of three-state buffer. (06 Marks)

OR

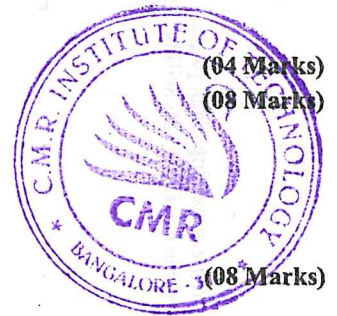
- 6 a. Implement the following functions using 3:8 decoder
 $f_1(a, b, c) = \sum m(0, 4, 6, 7)$
 $f_2(a, b, c) = \sum m(1, 4, 5)$ (06 Marks)
- b. Implement the following Boolean functions using an appropriate PLA:
 $f_1(a, b, c) = \sum m(0, 4, 7)$ (06 Marks)
 $f_2(a, b, c) = \sum m(4, 6)$ (08 Marks)
- c. Realize a full adder using PAL. (08 Marks)

Module-4

- 7 a. Explain the structure of VHDL program. Write VHDL code for 4-bit parallel adder using full adder as component. (08 Marks)
- b. With necessary diagrams, Explain switch debouncing with an S-R latch. (06 Marks)
- c. Explain D flip-flop with the help of timing diagram. (06 Marks)

OR

- 8 a. Give the implementation of T-flip-flop from D flip-flop. (04 Marks)
- b. Explain master-slave J-K flip-flop operation. (08 Marks)
- c. Derive the characteristic equations for the following flip-flops:
 i) S-R flip-flop
 ii) D-flip flop
 iii) T-flip-flop
 iv) J-K flip-flop. (08 Marks)



Module-5

- 9 a. With neat sketch, explain the working principle of Serial Input Serial Output (SISO) shift register. (06 Marks)
- b. Design 3 bit synchronous binary counter using transition table of T-flip-flop (08 Marks)
- c. Explain how 4 bit register with data, load, clear and clock input is constructed using D-flip-flops. (06 Marks)

OR

- 10 a. With the help of state graph, state and transition table and timing diagram, explain sequential parity checker. (06 Marks)
- b. With the help of block diagram, explain the working principle of n-bit parallel adder with accumulator. (08 Marks)
- c. Analyze following Moore sequential circuit for an input sequence X = 01101 and draw the timing diagram. (06 Marks)

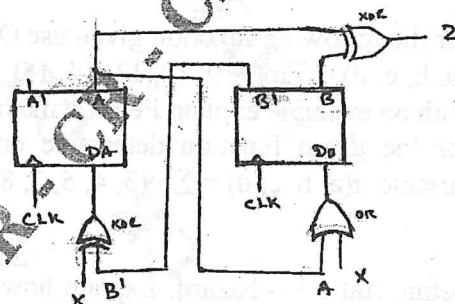


Fig.Q.10(c)
