CBCS SCHEME

USN

17CS32

Third Semester B.E. Degree Examination, Jan./Feb. 2021
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain with the constructional details and characteristics curves, the working of n-channel JFET. **(08 Marks)**

b. Define the following op-amp parameters: (i) CMRR (ii) Slew Rate **(04 Marks)**

c. With circuit diagram, explain the operation of Astable Multivibrator using IC 555. **(08 Marks)**

OR

2 a. Design a voltage divider bias network using DE-MOSFET with supply voltage V_{DD} = 16 V, I_{DSS} = 10 mA, Vp = –5V to have Quiscent drain current of 5 mA and gate voltage of 4V (assume the drain resistance R_D to be 4 times the source resistor R_S) **(08 Marks)**

b. List the Ideal characteristics of op-amp. **(04 Marks)**

c. With circuit diagram and waveforms, explain the working of Relaxation Oscillator. **(08 Marks)**

Module-2

3 a. Explain positive logic and negative logic. **(07 Marks)**

b. Use K-map to simplify the following functions:

(i) f(A, B, C, D) = Σm(0, 2, 6, 10, 11, 12, 13) + d(3, 4, 5, 14, 15)

(ii) f(A, B, C, D) = πM(1, 2, 4, 5, 6, 7, 8, 10, 11, 13, 14) **(06 Marks)**

c. Explain Static-1 Hazard and Hazard cover with an example. **(07 Marks)**

OR

4 a. Write HDL code for the Boolean expression Y = AB + CD. **(08 Marks)**

b. Get the simplified expression of, Y(A, B, C, D) = Σm(0, 1, 3, 7, 8, 9, 11, 15). Using Quine Mc Clustery method. **(12 Marks)**

Module-3

5 a. Show how two 1:16 deMUX can be connected to get 1:32 deMUX. **(10 Marks)**

b. With IEEE symbol, logic symbol, explain NAND gate SR latch. Justify the Truth Table. **(10 Marks)**

OR

6 a. Explain the positive edge triggered JK flipflop. **(10 Marks)**

b. List the differences between PAL and PLA. Explain 7-segment decoder using PLA. **(10 Marks)**

Module-4

7 a. What are the various ways of representing flip flop? Explain the various representation of JK, SR, D, T flip flop. **(10 Marks)**

b. Define Register. Explain SISO using four D- flip flops. Assume initial values of 4 flip flop QRST as 1010, write truth table and plot waveforms. **(10 Marks)**

OR

8 a. Design mod-3 counter using JK flip flop. Also draw state diagram and write the truth table. **(10 Marks)**

b. Explain Linear Feedback Shift Register [LFSR] for the polynomial $x^4 + x^3 + 1$. **(10 Marks)**

Module-5

9 a. Explain Digital Clock with block diagram. **(10 Marks)**

b. What is Binary ladder? Explain Binary ladder with digital input of 1000. **(10 Marks)**

OR

10 a. Explain Successive Approximation A/D converter. **(10 Marks)**

b. Write short note on A/D Accuracy and Resolution. **(04 Marks)**

c. Design mod-5 counter using JK flip flops. Write the truth table and draw the waveforms. **(06 Marks)**

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