Visvesvaraya Technological University, Belagavi.

PROJECT REPORT

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"Performance of LDPC encoder and decoder in 5G"

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CERTIFICATE

This is to Certify that the dissertation work **"Performance of LDPC encoder and decoder in 5G"**carried out by PARAM.JYOTHI.REDDY.GUTTI , PRAGATHI.N , PRAMODH.K.REDDY, USN:1CR16EC105, 1CR16EC110 , 1CR16EC112 bonafide students of **CMRIT** in partial fulfillment for the award of **Bachelor of Engineering** in **Electronics and Communication Engineering** of the **Visvesvaraya Technological University, Belagavi ,** during the academic year **2019-20**. It is certified that all corrections/suggestions indicated for internal assessment have been incorporated in the report deposited in the departmental library. The project report has been approved as it satisfies the academic requirements in respect of Project work prescribed for the said degree.

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CHAPTER 1

ELECTRONICS AND RADAR DEVELOPMENT AND ESTABLISHMENT (LRDE)

Historical Background

Electronics and Radar Development Establishment (LRDE) is a laboratory of the Defence Research & Development Organization (DRDO). Located in C.V. Raman Nagar, Bangalore its primary function is research and development of Radars and related technologies.

LRDE is sometimes mis-abbreviated as "ERDE". To distinguish between "Electrical" and "Electronic", the latter is abbreviated with the first letter of its Latin root (lektra). The same approach is used for the DLRL.

The LRDE is India's premier Radar design and development establishment and is deeply involved in Indian radar efforts. Its primary production partners include Bharat Electronics Ltd. and various private firms like Mistral in Bangalore, Astra micro in Hyderabad and Data patterns in Chennai.

The genealogy of LRDE originates from the Inspectorate of Scientific Stores created in 1939 at Rawalpindi. This was re-christened as TDE (Technical Development Establishment) in early 1946 and relocated in Dehradun. With electronic industrial complexes growing in the Bangalore outskirts, the Electronics part of TDE (I&E) branched off to settle in this seminal city in 1955. Coinciding with the promotion of DRDO (Defence Research and Development Organisation), then TDE (E) was divided into Inspectorate of Electronics Equipments (ILE) and LRDE(Electronics RADAR Development and Establishment) on 01 Jan 1958 to meet the aspiration of Defense Services. LRDE moved to the present location in 1986 to find place for expansion and growth.

Born in the barracks of High Grounds in Jan 1958 as Electronic Research and Development Establishment, got the present name Electronics & Radar Development Establishment in Jun 1962. With the nucleus personnel, equipment and material inherited from parental TDE (E), initial emphasis was laid to undertake such tasks as investigation of defects in equipment or necessary modifications required to improve the performance of equipment covering the entire spectrum of defence electronics.

During the initial years, the necessity of redefining the objectives of establishment was appreciated to reorient & to undertake development of modern sophisticated and complicated radio, line communication, radar,

electrical, electro-medical equipment, devices, and their accessories with maximum indigenous content. With every passing year, efforts were concentrated in recruiting committed, qualified personnel and organizing the various divisions or departments, so as to function in a well coordinated fashion for undertaking meaningful development of systems that could withstand the rigmarole of field acceptance. Early in life, LRDE visualized the scientific and logical guidelines for the systematic development of electronic equipment.

The roles of DRDO, User Agencies, the Inspection Authorities and Maintenance Authorities were orchestrated through DDPIL-64. LRDE played a major role in bringing out the modified DDPIL-69 which has withstood the test of time till date, albeit practical modifications or adaptations. Structured and partnership oriented development processes were born in late sixties. The functional based Radar Divisions, the Engineering Service Divisions, in consonance with professional project management practices, came into existence during 1967-68.

Vigorous activities were undertaken in the area of radars. Modifications to Fire Control Radar AA No 3 Mk7, development of S-1000 Mk I radar based on CSF (Compagnie de Telegraphie Sans Fil) radar ER 370 and FAX Mk I radar for locating mortars and guns for Artillery and Battle Field Surveillance Radar to detect moving men and vehicles were major innovative achievements in the radar area during that period. In the absence of open literature on modern radars, the scope in sixties was limited to learn through development of modules/components for radars in Service. The confidence building exercise won the day and firm foundation was laid for system approach of seventies and eighties.

Vision and Mission of LRDE

Vision: To create a center of excellence in design and development of radars and related technologies.

Mission: Develop Radar system and related technologies to cater to the needs of services. Enhance the infrastructure, knowledge base and technologies for achieving self-reliance.

1.1 Areas of Work

Design and Development of Radar Systems for army based, Navy based, air force based by LRDE is as given below –

Army:

a) Multifunction Phased Array Radar and 3D Surveillance Radar for Akash Missile Weapon System.

b) Low Level Light weight 2D Radar for mountainous terrain Air Defence.

c) 3D -Tactical Control Radar for Air Defence.

d) Short Range Battle Field Surveillance Radar.

e) Weapon Locating Radar.

f) Multi Mission Radar (MMR).

g) FOPEN Radar.

h) Through wall detection Radar.

i) Ground Penetration Radar.

Air Force:

a) Multifunction Phased Array Radar and 3D Surveillance Radar for Akash Missile Weapon System.

b) Active Phased Array Radar for AEW&C.

c) Low level 2D Air Defence Radar.

d) 3D Low Level Light Weight Radar.

e) 3D Medium Range Surveillance Radar for Air Defence (AD).

f) 4D Active Array Medium Power radar for AD role.

g) Airborne Electronically Scanned Array Radar for Tejas Mark II.

h) Ground Controlled interception.

i) SAR for UAVs.

Navy:

a) Maritime Patrol Radar for fixed and Rotary Wing Aircraft.

b) Maritime Patrol Radar with RS and ISAR.

c) 3D Medium Range Surveillance Radar for ASW Corvettes.

d) Multifunction Phased Array Radar for Air Defence Ship.

e) Maritime Patrol Airborne Radar for UAV.

f) Coastal Surveillance Radar (CSR).

Products and Technologies for Civil Sectors

a) Terminal-based Air Traffic Control (ATC) Radars

3D Medium Surveillance Radar (3D CAR) can be upgraded with Radar Data Processing (RDP) for improved and efficient handling of large air traffic. The Radar Networking System can be used to link various ATC radars to extend the air surveillance coverage to regulate civil air traffic. Transfer of radar air pictures through digital data link of limited bandwidth (possible at output of RDP) will enable netting shore-based as well as offshore radar installations for coastal air defence.

b) Industrial Perimeter Surveillance Radar

Light Weight Battery Powered Radar (BFSR - SR) for Surveillance of large industrial, defence and other installations to detect intruders up to the distance of 2 kms. The Radar can detect even a crawling man. Classification of targets such as Crawling man, Walking man, Group of men walking, moving light vehicles is possible with Doppler Tone.

c) Antennas

Slotted Waveguide Array Solutions are available in X and Ku band for airborne and land based radars. The antennas are rugged, compact and offer high radiation efficiency with high power handling capability. Microstrip Patch Array Antenna Solutions are available in X band for airborne and ground based radar. It is light-weight, low power and cost effective.

d) Radar Data Processing (RDP) Technology

RDP technology, using state-of-the-art processors (like Power PC) and very efficient algorithms, is established and available. The technology offers efficient solutions in automatic tracking of multiple targets, False alarm and clutter suppression, multi sensor data fusion, target classifications etc.

e) Avalanche Victim Detector (AVD)

AVD can be used by high altitude trekkers and mountaineers as life saving device in case of burial under avalanche or any other debris. The device can be used in the mining sector for limited burial depth.

f) Infrastructure facilities

Environmental, EMI/EMC and Antenna measurement facilities are available to private and public sector undertakings.

CORE COMPETENCIES

LRDE is committed to the indigenous development of modern radar systems through an effective Quality Management System. Some of its core competency areas are

1. Radar System Engineering

2. Develop critical radar technologies like TR Modules, Antenna arrays, Transmitters, Digital Receivers, DDS programmable signal and data processors

3. Design and Development of major sub-systems –

   a. Mechanical and Electronic Scanning Antennas

   b. High Performance Exciters and Receivers , High Power Transmitters , Digital signal & Data

   c. Processors, Consoles, Mechanical Engineering, Digital Beam Forming (DBF)

   d. Array Group Receiver (AGR), Central Unit.

4. System Integration and Evaluation

5. Radar System Integration with other entities

6. Environmental engineering including EMI/EMC.

CHAPTER 2

INTRODUCTION

Generally, communication means conveying or exchanging the information from one end to another through a communication channel. A communication is said to be perfect only if the receiver receives the data that is transmitted without any error. But whenever we are transmitting data over a communication channel an error may occur due to the presence of noise in the channel. The main challenge in the communication system is to achieve a reliable and error free transmission of data from source to destination. So to increase the reliability of data transmission too basic control stratergies like Automatic Repeat Request (ARQ) and Forward Error Correction (FEC) is used.

In the ARQ scheme receiver requests retransmission of unreliable data frames. The data frame declared as unreliable when the error is detected in the frame. But the FEC scheme can be used for both error detection and correction. In FEC error detection and correction uses the added redundant bits called parity bits on the transmission side. So FEC is usually preferred over ARQ schemes since ARQ schemes result in unnecessary wastage of the channel bandwidth due to retransmission. Nowadays there is a great demand for video streaming services which make us to analyse and design algorithms to provide good error correcting probability. LDPC codes have been selected for the Enhanced Mobile Broadband (eMBB) data channels for 5G New Radio, while Polar codes have been chosen for the corresponding control channel. Beyond any doubt, LDPC codes and their variants will find more deployment in many other applications and will be included in other new standards in the future.

In this work we have implemented coding and decoding of low density parity check (LDPC) codes and compared the results with the turbo codes. This uses iterative decoding.

2.1 MOTIVATION

An LDPC code is a linear block code defined by a very sparse parity check matrix, which is populated primarily with zeros and sparsely with ones. The LDPC code gives better performance when extended to non-

binary code as well as binary code to define code words and it yields a ratio of signal to noise, which approaches Shannon channel capacity limit.

Even before the usage of LDPC, Turbo Codes were used which is a capacity approaching coding scheme. These are high performance forward error correction (FEC) codes which are closely related to the channel capacity. Turbo codes are nowadays competing with LDPC codes which provide similar performance. But turbo codes are suitable only at lower code rates and also performance is less compared to low density parity check codes. LDPC overcomes these issues easily. The performance of LDPC is evaluated in terms of bit error rate (BER) for a given value of Eb/No. Simulation results demonstrate that the bit error rate (BER) performance of the LDPC system is better than Turbo codes and close to that of coherent detection by extending the iterative decoding. In addition, the simulation results show that the LDPC system, which can exploit the receive diversity benefit, has much better performance over additive white Gaussian channels. So this motivated us to implement the LDPC codes to achieve better performance and reliable communication.

Compared to other classes of codes , LDPC codes are very fast (probabilistic) encoding and decoding algorithms. The question is about the design of the codes such that these algorithms can recover the original code word in the presence of large amounts of noise. There is a possibility to solve this design problem by new analytic and combinatorial tools. This makes LDPC codes not only attractive from a theoretical point of view, but also perfect for practical applications.

CHAPTER 3

LITERATURE SURVEY

A number of technical papers have dealt with encoding and decoding of LDPC codes.

Michel Zorzi [**1**] have explained that when the data is transmitted over a communication channel there are chance of error occurring due to the presence of noise in the channel. The main challenge in the communication system is to achieve a reliable and an error free transmission of data from information source to destination. To increase the reliability of data transmission two basic error control strategies are used. They are Automatic Repeat Request (ARQ) and Forward error correction (FEC).

C. E Shannon etal [**2**] have introduced a new channel parameter called channel capacity. Shannon theorem showed that "In a noisy channel with capacity „C" ,an information is transmitted at a rate R then, if R is less than C there exists a coding technique which allows the probability of error at the receiver to be made arbitrarily small". This means that it is possible to transmit information with arbitrarily zero probability of error up to nearly a limit of C bits per second, known as the Shannon limit.

R.G Gallager etal [3] , have stated that the Shannon theorem gave rise to the introduction of many error correcting codes called as the channel codes. Channel codes are divided into two, linear block codes and Convolutional codes.

Aqiel N. Almaamory etal[**4**] have stated that although an LDPC code is a block code it gives exceptional BER performance nearly close to Shannon limit when compared to other block codes. This work presents a comparison between the Convolutional Encoding CE, Parallel Turbo code and Low density Parity Check (LDPC) coding schemes with a Multi User Single Output MUSO Multi-Carrier Code Division Multiple Access (MC-CDMA) system over multipath fading channels. The decoding technique used in the simulation was iterative decoding since it gives maximum efficiency at higher iterations. This is due to the message passing decoding algorithm used in the LDPC decoder [**5**].

[5] shows that LDPC codes provide a significant system performance improvement with respect to the state-of-the-art FEC schemes .Such codes have high rates and can lend themselves to very low-complexity encoder/decoder implementations. The system performance is further improved by a code design that eliminates short cycles in a graph employed in iterative decoding

LDPC codes also provide high code gain at low BER. Turbo codes also work close to the Shannon limit. But decoding complexity is higher in turbo codes than LDPC [**6**] and [**7**].

LDPC codes were formulated by Robert Gallagher [8] and presented in his PhD thesis. But they were largely forgotten, and reinvented several times for the next 30 years. Their comeback is one of the most intriguing aspects of their history, since two different communities' reinvented codes similar to Gallagher's LDPC codes at roughly the same time, but for entirely different reasons.

M. Luby, etal [9] author has stated belief propagation can be analysed using a combination of tools from combinatorial and probability theory. The first analysis for a special type of belief propagation appeared in [9], and was applied to hard decision decoding of LDPC codes in [10]. The analysis was vastly generalized in [11] to belief propagation over a large class of channels.

[12]Turbo codes, prevalent in most modern cellular devices, are set to be replaced by LDPC codes as the code for forward error correction. This transition was ushered in mainly because of the high throughput demands for 5G New Radio (NR). The new channel coding solution also needs to support incremental-redundancy hybrid ARQ, and a wide range of blocklengths and coding rates, with stringent performance guarantees and minimal description complexity. Here[12] we briefly review the requirements of the new channel code for 5G NR. We then describe the LDPC code design philosophy and how the broad requirements of 5G NR channel coding led to the introduction of novel structural features in the code design, culminating in an LDPC code that satisfies all the demands of 5G NR.

The standard codes for 5G enhanced mobile broadband data channel is LDPC . These standard codes are designed to support multiple lifting sizes and possess rate-compatible property,which can help adapt various information lengths and coderates well.Here[13]we will first review the encoding mechanism and requirements of 5G LDPC codes, and present cycle analysis for such emerging codes.It is then applied to the proposed algorithm to construct the exponent matrices for cases of 5G LDPC codes and the standard LDPC codes of consultative committee for space data systems, respectively.

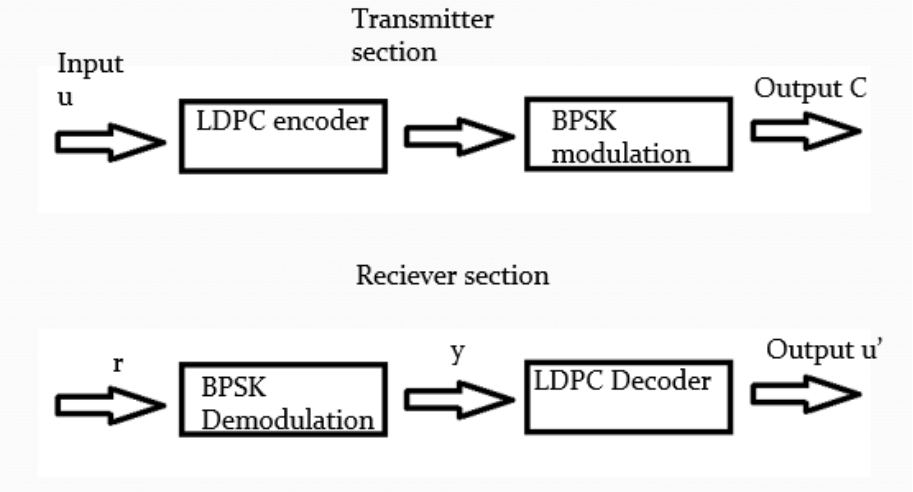
Although many coding schemes with capacity achieving performance at large block lengths are available, many of those do not show consistent good performance in a wide range of block lengths and code rates as the eMBB scenario demands. But turbo, LDPC and polar codes show promising BLER performance in a wide range of coding rates and code lengths.

OBJECTIVE

- The main objective is to achieve error free communication by using LDPC code. We achieve this by implementing the Encoding technique for the given message information.
- Implementing the modulation technique for the encoded data and analysing the performance of the proposed system by calculating Bit error rate.
- Our objective is to show that the LDPC codes are better than turbo codes by comparing their BER and SNR performances.
- And show that due to these reasons they are being used in the upcoming new radio technology 5G.
- The application we deal with is EMBB.

2.3 METHODOLOGY

Using MATLAB we intend to implement LDPC encoding and decoding for text data.
We intend to use BPSK modulation at the transmitter section and BPSK demodulation at the receiver section respectively as shown in the below figure.


Transmitter section
Input u
LDPC encoder
BPSK modulation
Output C
Reciever section
r
BPSK Demodulation
y
LDPC Decoder
Output u'

CHAPTER 4

LDPC ENCODER AND DECODER

Analog computation is more energy and area-efficient at the cost of its limited accuracy,where as digital computation is more Versatile and derives greater benefits from technology scaling. Besides, design automation tools for digital circuits are much more sophisticated than those for analog circuits. Time domain analog and digital mixed signal processing (TD-AMS) exploits both advantages, and is a solution better suited to implementing a system on chip including functions for which high computational accuracy is not required, such as error correction, image Processing, and machine learning. TD-AMS is a hybrid of analog signal processing and binary digital signal Processing that is optimized in order to enjoy their respective advantages. The efficiency of analog computation in several arithmetic functions derived from a single analog signal's capacity to convey multi-bit information is exploited, whereas the advantages of digital signal processing, such as performance improvement due to technology scaling and versatility of binary logic, are fully retained.

As an example, a low-density parity-check (LDPC) code decoder with the technique is implemented. Low Density parity check code (LDPC) is an error correcting code which reduces the error in the noisy communication channel and probability of losing the information. This probability can be reduced to a desired value so that the data rate transmission can be as close to Shannon's limit. Low-density parity-check (LDPC) codes are [1] of large block size, achieves a good performance very close to the Shannon limit [2], with low-complexity iterative decoding by Believe Propagation (BP) or the Sum-Product Algorithm (SPA) [3]. Decoding of LDPC codes can be performed efficiently as long as the parity-check matrices are sparsely populated.

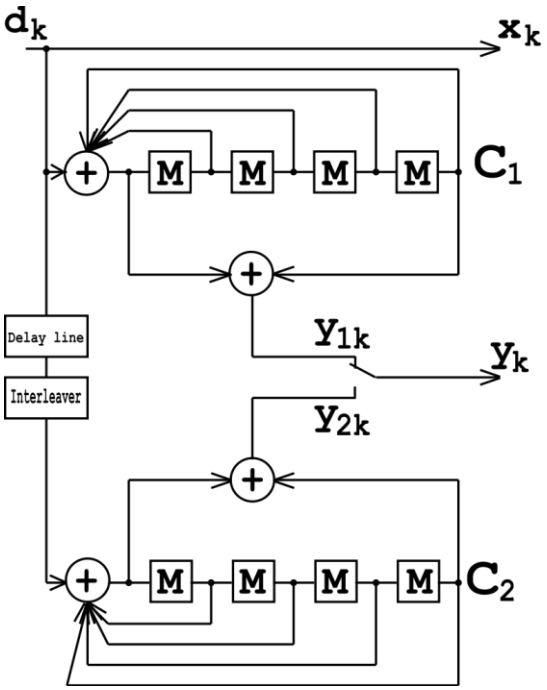
LDPC is applied to wireless, wired and optical communication system [6] and Storage application such as magnetic discs and compact discs. The main attraction for LDPC codes is less computational complexity.

EXISTING SYSTEM

In 1993 Turbo Codes are discovered which is a capacity approaching coding scheme. These are high performance forward error correction (FEC) codes which closely related to the channel capacity. Channel capacity means, with maximum code rate and the specific noise level also, reliable communication is possible. Some of the applications of turbo codes are, they used in 3G/4G mobile communications, deep space network and satellite communications as well as other applications to achieve reliable information transfer in the presence of noise. Turbo codes are nowadays competing with LDPC codes which provide similar performance.

TURBO ENCODER

The figure 3.1 Shows classic turbo encoder and explains the 4th general design of parallel turbo codes.



This encoder sends three sub-blocks of bits.

1) The first sub-block in the m-bit block of payload data.
2) The second Sub block is a n/2 parity bits for payload data, computed using a Recursive sysytematic convolution code(RSC).

3) The third sub-block is n/2 parity bits for a known permutation of the payload data, again computed using RSC code.Thus, two redundant but different sub-blocks of parity bitssent with the payload. The complete block has m + n bits of data with a code rate of m/(m+n).

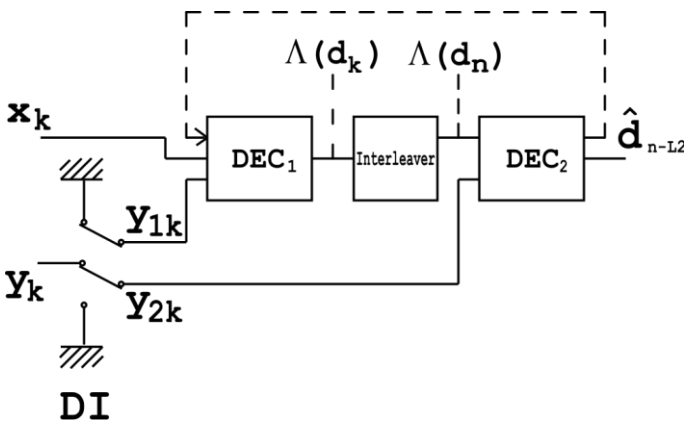
The permutation of the payload data is carried out by a device called an interleave.

Hardware-wise, this turbo-code encoder consists of two identical RSC coders, C1 and C2, as depicted in the figure, which are connected to each other using a concatenation scheme, called parallel concatenation. M is a memory register. The delay line and interleave force input bitsdk to appear in different sequences. At first iteration, the input sequence dk appears at both outputs of the encoder, xk and y1k and y2k due to the encoder's systematic nature. If the encoders C1 and C2 are used respectively in n1 and n2 iterations, their rates are respectively equal to

$$R_1 = \frac{n_1 + n_2}{2n_1 + n_2}$$
$$R_2 = \frac{n_1 + n_2}{n_1 + 2n_2}$$

TURBO DECODER

Figure 3.2. shows the Turbo code Decoder. Two elementary decoders DEC_1, and DEC_2 are interconnected to each other in serial way. The DEC_1 decoder operates on lower speed. Thus it is intended for the C_1 encoder and DEC_2 is for C_2 encoder. DEC_1 leads to L_1 delay because of soft decision. The delay line in the encoder also causes some delay. Similarly DEC_2 causes L_2 delay.



An interleaver installed between the two decoders is used here to scatter error bursts coming from output. *DI* block is a demultiplexing and insertion module. It works as a switch, redirecting input bits to DEC_1 at one moment and to DEC_2 at another. In OFF state, it feeds both y_{1k} and y_{2k} inputs with padding bits (zeros).

The decoder receives a pair of random variables:

$$x_k = (2d_k - 1) + a_k$$
$$y_k = 2(Y_k - 1) + b_k$$

PROPOSED SYSTEM

LINEAR BLOCK CODES

Linear block codes are error correction codes which attach the redundant bits to the transmitted data. These redundant bits are used for error correction. The extra bits added to the transmitted data are known as parity bits. Error occurs when the parity bit is corrupted or the number of 1s in the information bit sequence is the different from the number used to compute the parity bit [8]. A binary block code generates a block of n coded bits from k message bits. The coded bits are known as codeword symbols. If n > k then n-k bits provides the redundancy needed for error detection and correction. R = k/n is known as code rate. For k input message, 2k different input entries are possible. In linear block codes each bits or symbols expressed as the linear combination of other bits or symbols. Thus the name linear blocks code.

The encoding of linear block code is done using a matrix called as generator matrix, G at the transmitter. At the receiver decoding is done using the parity check matrix H. For a received code word C_i If $CiH^T = 0$, then the received codeword is said to be valid. That is the received code word is valid, only when the product of a valid code word and parity check matrix results in an all zero vector. Linear block codes are decoded in two ways. They are standard array method and syndrome method. The main difference between classical block codes and LDPC codes are the method used forthe decoding, In classical block codes ML like decoding algorithm is used. LDPC codes are decoded iteratively using the message passing algorithm based on the graphical representation of their parity check matrix.

LOW DENSITY PARITY CHECK CODES(LDPC)

Low Density parity check code (LDPC) is an error correcting code which reduces the error in the noisy communication channel and probability of losing the information. This probability can be reduced to a desired value so that the data rate transmission can be as close to Shannon's limit. A linear code has a parity check matrix representation and a bipartite graph but not all linear codes have a sparse representation. Low-density parity-check (LDPC) codes [1] of large block size, achieves a good performance very close to the Shannon limit [2], with low-complexity iterative decoding by Believe Propagation (BP) or the Sum-Product Algorithm (SPA)[3]. Decoding of LDPC codes can be performed efficiently as long as the parity-check matricesare sparsely populated. The length of the shortest cycle in the Tanner graph [4] of the codedetermines the performance under BP decoding. The sparseness of the parity-check matrix (PCM) allows for decoding with low complexity based on a graph based decoder.

Some ideas for lower-complexity LDPC encoding have been presented recent years which exploits the sparseness of PCM are: the graph-based message-passing encoder [5],[6] is a technique which uses the decoder for encoding with an assumption that the unknown parity bits have been erased by the channel. Hence, the encoding process is exactly the same as decoding after transmission over a binary erasure channel (BEC). The same idea is applied for any LDPC code regular or irregular, random or structured.

As the demand for video streaming services is constantly growing day by day which has motivated us to analyse and design algorithm to provide good error probability. And also it has been selected as the coding scheme for enhance Mobile Broad Band (eMBB) data channel in the fifth generation (5G) New Radio (NR) mobile communication network. The available bandwidth on mobile is limited and expensive thus we need some technology that utilizes the available spectrum more efficiently and providing good error correction capability. The implementation presented here is based on iterative decoding using belief propagation. The eMBB provides its uses in Indoor hotspot, Dense Urban and Rural Areas.

An LDPC code is a linear block code defined by a very sparse parity check matrix, which is populated Primarily with zeros and sparsely with ones. The LDPC code also showed improved performance when extended to non-binary codes as well as binary code to define code words. The LDPC code yields a signal to noise ratio approaching a Shannon channel capacity limit, which is the theoretical maximum amount of digital data that can be transmitted in a given bandwidth in presence of certain noise interference.

For irregular low density parity check code the degree of all set of nodes are considered in accordance to some distribution. The first Step involved is describing the desired numbers of column for each weight and desired numbers of rows for each weight. Next step involves a Construction method which includes an algorithm for

determining edges between the vertices in such a way that the constraints are satisfied. The edges are completely random in nature.

Here We have divided the LDPC system into two major blocks:-

1) ENCODER BLOCK
2) DECODER BLOCK

ENCODER BLOCK

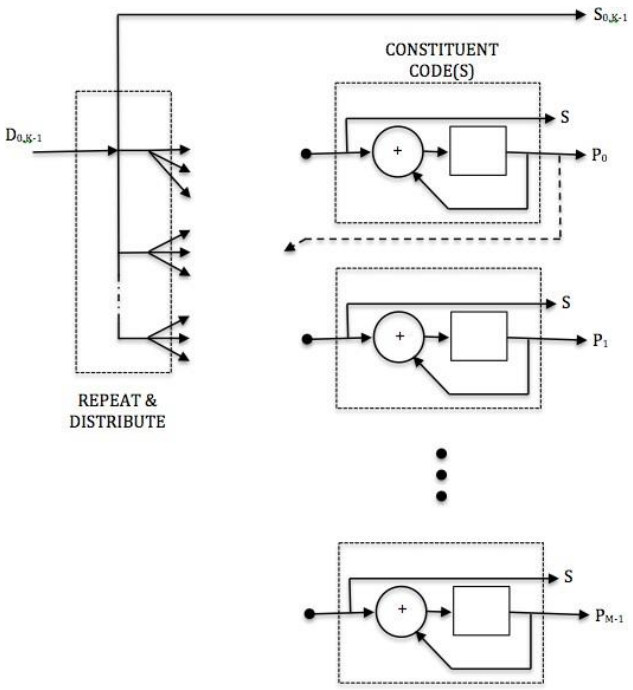


Figure 3.4 Functional components of LDPC

The above figure illustrates the functional components of LDPC encoder:

During the encoding of a frame, the input data bits (D) are repeated and distributed to a set of constituent encoders. The constituent encoders are typically accumulators and each accumulator is used to generate a parity symbol. A single copy of the original data ($S_{0,K-1}$) is transmitted with the parity bits (P) to make up the code symbols. The S bits from each constituent encoder are discarded. The parity bit may be used within another constituent code.

In an example using the DVB-S2 rate 2/3 code the encoded block size is 64800 symbols (N=64800) with 43200 data bits (K=43200) and 21600 parity bits (M=21600). Each constituent code (check node) encodes 16

data bits except for the first parity bit which encodes 8 data bits. The first 4680 data bits are repeated 13 times (used in 13 parity codes), while the remaining data bits are used in 3 parity codes (irregular LDPC code).

For comparison, classic turbo codes typically use two constituent codes configured in parallel, each of which encodes the entire input block (K) of data bits. These constituent encoders are recursive convolutional codes (RSC) of moderate depth (8 or 16 states) that are separated by a code inter leaver which interleaves one copy of the frame.

The LDPC code, in contrast, uses many low depth constituent codes (accumulators) in parallel, each of which encode only a small portion of the input frame. The many constituent codes can be viewed as many low depth (2 state) 'convolutional codes' that are connected via the repeat and distribute operations. The repeat and distribute operations perform the function of the interleaver in the turbo code.

The ability to more precisely manage the connections of the various constituent codes and the level of redundancy for each input bit give more flexibility in the design of LDPC codes, which can lead to better performance than turbo codes in some instances. Turbo codes still seem to perform better than LDPCs at low code rates, or at least the design of well performing low rate codes is easier for Turbo Codes.

As a practical matter, the hardware that forms the accumulators is reused during the encoding process. That is, once a first set of parity bits are generated and the parity bits stored, the same accumulator hardware is used to generate a next set of parity bits.

DECODER BLOCK

The ldpc decoder has 2 smaller decoders which are used repeatedly and combined in an interesting way. As with other codes, the maximum likelihood decoding of an LDPC code on the binary symmetric channel is an NP-complete problem. Performing optimal decoding for a NP-complete code of any useful size is not practical.

However, sub-optimal techniques based on iterative belief propagation decoding give excellent results and can be practically implemented. The sub-optimal decoding techniques view each parity check that makes up the LDPC as an independent single parity check (SPC) code. Each SPC code is decoded separately using soft-in-soft-out (SISO) techniques such as SOVA, BCJR, MAP, and other derivates thereof. The soft decision information from each SISO decoding is cross-checked and updated with other redundant SPC decoding of the same information bit. Each SPC code is then decoded again using the updated soft decision information.

This process is iterated until a valid code word is achieved or decoding is exhausted. This type of decoding is often referred to as sum-product decoding.

The decoding of the SPC codes is often referred to as the "check node" processing, and the cross-checking of the variables is often referred to as the "variable-node" processing.

In a practical LDPC decoder implementation, sets of SPC codes are decoded in parallel to increase throughput.

In contrast, belief propagation on the binary erasure channel is particularly simple where it consists of iterative constraint satisfaction.

ABOUT MATLAB

MATLAB is a high-performance language for technical computing. It integrates computation, visualization, and programming in an easy-to-use environment where problems and solutions are expressed in familiar mathematical notation. The name MATLAB stands for matrix laboratory. MATLAB is an interactive system whose basic data element is an array that does not require dimensioning. This allows you to solve many technical computing problems, especially those with matrix and vector formulations, in a fraction of the time it would take to write a program in a scalar noninteractive language such as C or Fortran. In university environments, it is the standard instructional tool for introductory and advanced courses in mathematics, engineering, and science. In industry, MATLAB is the tool of choice for high-productivity research, development, and analysis. The MATLAB version we use for implementing LDPC codes is MATLAB-2019b. This version of MATLAB provides a NR 5g toolbox. With the toolbox you can configure, simulate, measure, and analyze end-to-end 5G NR communications links. You can modify or customize the toolbox functions and use them as reference models for implementing 5G systems and devices.

CHAPTER 5

SYSTEM IMPLEMENTATION

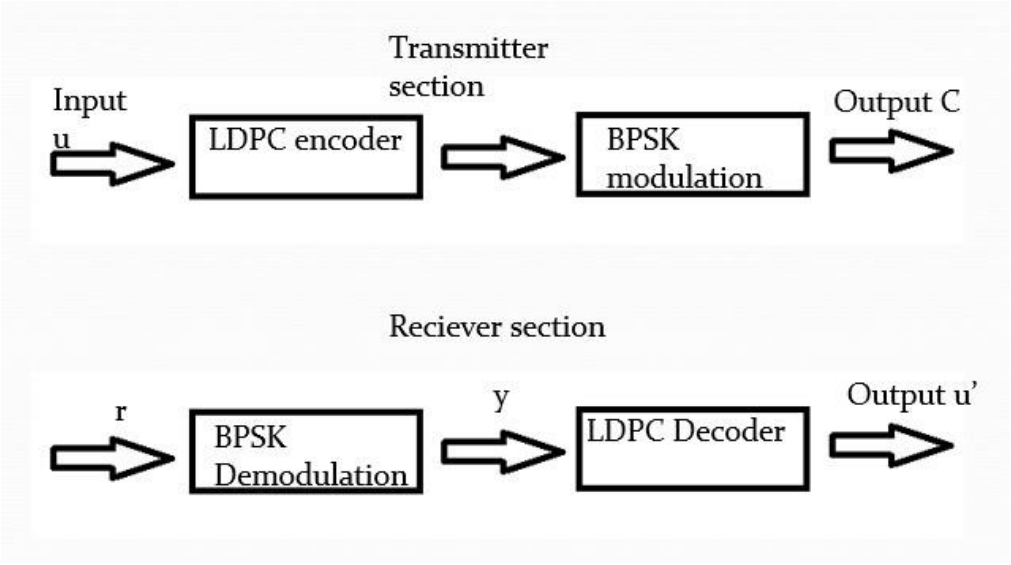


Figure 4.1 Block diagram of system model using LDPC Codes

Figure 4.1 represents the system model of a basic digital communication system which uses LDPC code as the channel code and BPSK modulation. u is the block of message bits which input to the LDPC encoder and v is the output from the LDPC encoder. After BPSK modulation the codeword C is obtained.

LDPC ENCODING

The encoding of LDPC is carried out with the help of Parity Check matrix which is similar to generator matrix except having minor changes.

Let us say we have a code with Parity check matrix H , that is

$$H = \begin{matrix} 1 & 1 & 0 & 1 & 0 & 0 \\ 0 & 1 & 1 & 0 & 1 & 0 \\ 1 & 0 & 1 & 0 & 0 & 1 \end{matrix}$$

The above Code is a (6,3) code and it is having a systematic form and now if we have the message vector m which is

m= $m1$ $m2$ $m3$

Now the code word(c) is given as

c= $m1$ $m2$ $m3$ $p1$ $p2$ $p3$

where p1,p2 and p3 are the parity bits and these parity bits can be easily computed with the help of H and m.

we know

$H.c^T=0$

$$\begin{matrix}1&1&0&1&0&0\\0&1&1&0&1&0\\1&0&1&0&0&1\end{matrix}\begin{matrix}m1\\m2\\m3\\p1\\p2\\p3\end{matrix}=\begin{matrix}0&0\\0&0\end{matrix}$$

Therefore from the above equation we can compute the parity bits whch is given as below equations

Row 1 : m1+m2=p1

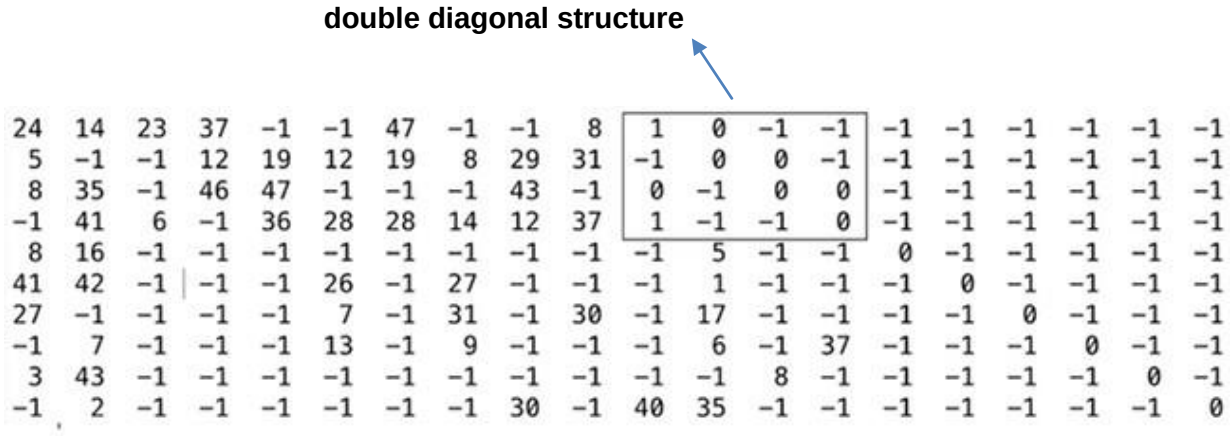
Row 2 : m2+m3=p2

Row 3 : m1+m3=p3

The above equations are nothing but the results of modulo 2 operation or simply the binary EXOR operation. The above method is the simple way to perform the encoding using Parity check matrix.

The same method is used for the encoding of LDPC codes. In the 5G standard there are two rate-compatible base graphs/Base Matrices , BG1 and BG2, for the channel coding. BG1 is targeted for larger block lengths ($500 \leq K \leq 8448$) having a size of 46x68 and higher rates ($1/3 \leq r \leq 8/9$), whereas BG2 is targeted for smaller blocklengths ($40 \leq K \leq 2560$) and lower rates ($1/5 \leq r \leq 2/3$) having a size of 42x 52.The maximum value of the expansion factor(Z) that can be used is 384.Base graphs BG1 and BG2 have similar structure. Base graph BG1 has 22 information bit columns. Using sub-column shortening, we see that any information block length in the range 21*Z to 22*Z for any of the above Z values can be supported.

Let us consider the example base matrix of BG2,since we cannot consider the whole matrix let us consider only 10 rows and 20 columns of BG2 and iLS=3, j=4,Z=48 where Z is the expansion factor.



24	14	23	37	-1	-1	47	-1	-1	8	1	0	-1	-1	-1	-1	-1	-1	-1	-1	-1
5	-1	-1	12	19	12	19	8	29	31	-1	0	0	-1	-1	-1	-1	-1	-1	-1	-1
8	35	-1	46	47	-1	-1	-1	43	-1	0	-1	0	0	-1	-1	-1	-1	-1	-1	-1
-1	41	6	-1	36	28	28	14	12	37	1	-1	-1	0	-1	-1	-1	-1	-1	-1	-1
8	16	-1	-1	-1	-1	-1	-1	-1	-1	-1	5	-1	-1	0	-1	-1	-1	-1	-1	-1
41	42	-1	-1	-1	26	-1	27	-1	-1	-1	1	-1	-1	-1	0	-1	-1	-1	-1	-1
27	-1	-1	-1	-1	7	-1	31	-1	30	-1	17	-1	-1	-1	-1	0	-1	-1	-1	-1
-1	7	-1	-1	-1	13	-1	9	-1	-1	-1	6	-1	37	-1	-1	-1	0	-1	-1	-1
3	43	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	8	-1	-1	-1	-1	-1	0	-1	-1
-1	2	-1	-1	-1	-1	-1	-1	30	-1	40	35	-1	-1	-1	-1	-1	-1	-1	0	-1

Similarly as discussed earlier the parity matrix can be computed here. Here we can see that there is the presence of a double diagonal structure that is generally necessary in the base matrices because of which the efficiency increases .The computation of double diagonal structure can be done using the below mentioned procedure.

Let us consider the below double diagonal structure for example:

$$H = \begin{bmatrix} I_1 & 0 & I_3 & I_1 & I_2 & I & 0 & 0 \\ I_2 & I & 0 & I_3 & 0 & I & I & 0 \\ 0 & I_4 & I_2 & I & I_1 & 0 & I & I \\ I_4 & I_1 & I & 0 & I_2 & 0 & 0 & I \end{bmatrix}$$

$Z = 5$

Where I_k :Identity matrix column shifted k times

Message [m1 m2 m3 m4] each of 5 bits(mxz)

Codeword c=[m1 m2 m3 m4 p1 p2 p3 p4] each parity bits of 5 bits

Therefor now if we compute using the formula which is

$Hc^T=0$

We will have the following equations and we can compute the parity bits,

- H [m1 m2 m3 m4 p1 p2 p3 p4]^T = 0

- 1: $I_1m1 + I_3m3 + I_4m4 + I_2p1 + I\ p2 = 0$
- $I_2m1 + I\ m2 + I_3m3 + I\ p2 + I\ p3 = 0$
- $I_4m2 + I_2m3 + I\ m4 + I_1p1 + I\ p3 + I\ p4 = 0$
- $I_4m1 + I_1m2 + I\ m3 + I_2p1 + I\ p4 = 0$

➢ Adding all 4 ,

- $I_1p1 = I_1m1 + I_3m3 + I_1m4 + I_2m1 + I\ m2 + I_3m3 + I_4m2 + I_2m3 + I\ m4 + I_4m1 + I_1m2 + Im3$

➢ Find p1 from above

- P2 : use p1 in 1 , p3: use p2 in 2 , p4: use p3 in 3

By this method the encoding is done in the LDPC codes also where all the parity bits can be computed once the double diagonal structure is computed.

Channel Design

When encoded signals are transmitted through channel, coded signal may get corrupted by noise in the channel and other interferers. To model this effect here we are adding AWGN noise to the coded signal.

Additive white Gaussian noise (AWGN) is a basic noise model used in information Theory to mimic the effect of many random process that occur in nature. The modifiers denote specific characteristics

- „Additive" because it is added to any noise that might be intrinsic to the information system.
- „White" refers to idea that it has uniform power across the frequency band for the information system. It is an analogy to the color white which has uniform emissions at all frequencies in the visible spectrum.
- „Gaussian" because it has a normal distribution in the time domain with an average time domain value of zero.

LDPC DECODING

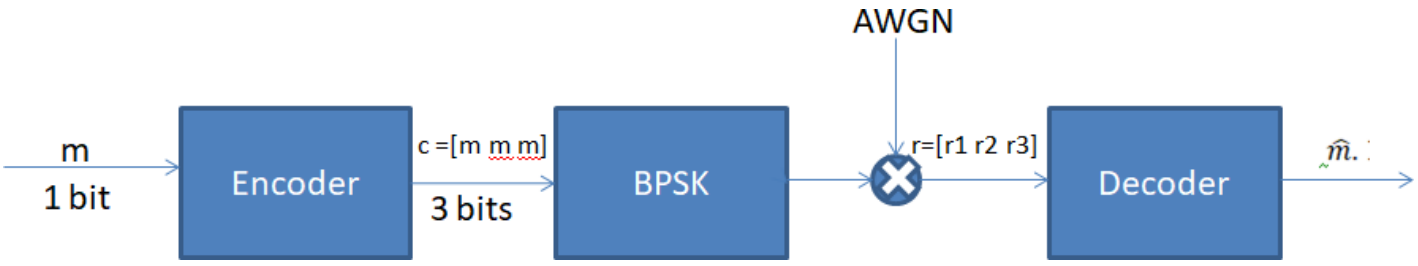
The ldpc decoder has 2 smaller decoders that are used repeatedly and combined in an interesting manner. The basic decoders that are used in the ldpc decoder is the decoder for a single parity check code and a decoder for the repetition code.

1. SINGLE PARITY CHECK CODE

2. REPETITION CODE

SISO DECODER FOR THE REPETITION CODE

Lets consider a (3,1) repetition code and look at it with BPSK modulation over a AWGN channel.



You have a message bit m which goes through the encoder that produces a codeword . then we do the BPSK modulation ie. 0 is mapped to +1 and 1 is mapped to -1 , and we get a symbol vector s. the noise is added to this and we get a received vector r.

The decoder has the task of producing m. But we will be interested in some sort of probability as the output. Not only do we want to say what the bit is but we also want to say how much do we believe in that value.that is the idea behind the decoder for the ldpc code.

Li = " belief " that bit c_i is 0.

Lets say r=[3.1 2.4 4.3] . All 3 are positive and fairly large numbers.

It is quite obvious that the transmitted symbol can be estimated or can be believed that it is +1.

On the other hand, if r= [0.01 -2.2 -0.5]

If you look at 0.01 , the confidence in saying that the transmitted symbol is was definitely +1 or -1 is very low.in that sense 0.01 also represents a belief about the 1st bit based on r1 alone. When you want to decided about the 1st bit we need to take into account r1, r2 and r3 bits. So basically looking at these examples , to compute L1 you need to consider r1,r2 and r3.

What is the probability that $P_r(C_1 = 0 \mid r) = \frac{f(r_1, C_1=0) \cdot P_r(C_1=0)}{f(r1)}$ ……(1)

$$P_r(C_1 = 1 \mid r_1) = \frac{f(r_1 \mid C_1=1) \cdot P_r(C_1=1)}{f(r1)} \quad \ldots\ldots(2)$$

$P_r(C_1 = 1)$ and $P_r(C_1 = 0)$ are the prior probability and is equal to ½ because Ci is the message itself and it could be either 1 or 0 with uniform probability.

Taking the ratio of (1) and (2),

$$\frac{P_r(C_1=0 \mid r_1)}{P_r(C_1=1 \mid r_1)} = \frac{\frac{f(r_1 \mid C_1=0) \cdot P_r(C_1=0)}{f(r1)}}{\frac{f(r_1 \mid C_1=1) \cdot P_r(C_1=1)}{f(r1)}} \quad \ldots.(3)$$

Equation (3) is called the likelihood ratio.

If c1=0, it implies the symbol is +1 and r1 = 1+ N(0 σ^2).

If c1=1 , it implies the symbol is -1 and r1= -1+ N(0 σ^2).

The likelihood ratio works out as $\frac{\frac{1}{\sqrt{2\pi}\sigma} e^{\frac{-(r1-1)^2}{2\sigma^2}}}{\frac{1}{\sqrt{2\pi}\sigma} e^{\frac{-(r1+1)^2}{2\sigma^2}}}$ .....(4)

Once you simplify this you get ,

$$\frac{P_r(C_1=0 \mid r_1)}{P_r(C_1=1 \mid r_1)} = e^{\frac{2r1}{\sigma^2}} \quad \ldots\ldots..(5)$$

$$l1 = \text{Log}\left(\frac{P_r(C_1=0 \mid r_1)}{P_r(C_1=1 \mid r_1)}\right) = \frac{2}{\sigma^2} r1 \quad \ldots\ldots(6)$$

Equation (6) gives us the intrinsic LLR.

We can see that the LLR is propotional to r1. Usually $\frac{2}{\sigma^2}$ is a positive factor and is ignored in most of the calculations.

Similarly , $l2 = \text{Log}\left(\frac{P_r(C2=0 \mid r2)}{P_r(C_2=1 \mid r_2)}\right) = \frac{2}{\sigma^2} r2$ .....(7)

We are interested in the final belief that is the combination of all the 3 recieved values ie. the output LLR which is given as

$$Li = \text{Log}\left(\frac{P_r\ C_i=0\ r_1,r_2r_3,}{P_r\ C_i=1\ r_1,r_2,r_3}\right) \quad \ldots\ldots(8)$$

By computing L1 we get,

$$L1 = \left(\frac{P_r\ C_1=0\ r_1,r_2,r_3}{P_r\ C_1=1\ r_1,r_2,r_3}\right) = \frac{\frac{f\ r_1,r_2r_3|C_1=0|\ .P_r\ C_1=0}{f(r_1,r_2r_3)}}{\frac{f\ r_1,r_2r_3|C_1=1|\ .P_r\ C_1=1}{f\ (r_1,r_2r_3)}}$$

$$= \left(\frac{P_r\ C_1=0\ r_1,r_2,r_3}{P_r\ C_1=1\ r_1,r_2,r_3}\right) = \frac{f\ r_1,r_2r_3|C_1=0\ .P_r\ C_1=0}{f\ r_1,r_2r_3\ |C_1=1|\ .P_r\ C_1=1} \quad \ldots\ldots(9)$$

For the repetition code , this conditional joint distribution/density is very easy to write down ie. c1=0 implies symbol vector is S=[+1 +1 +1] which implies r1= 1+ N1(0,σ^2) , r2= 1+ N2(0,σ^2) and r3= 1+ N3(0,σ^2), where N1,N2 and N3 are independent. Similarly when c1=1 implies symbol vector is S=[-1 -1 -1] which implies r1= -1+ N1(0,σ^2) , r2= -1+ N2(0,σ^2) and r3= -1+ N3(0,σ^2). Because the normal distributions are independent , you can simplify them as follows and get ,

$$\left(\frac{P_r\ C_1=0\ r_1,r_2,r_3}{P_r\ C_1=1\ r_1,r_2,r_3}\right) = \frac{e^{\frac{-(r1-1)^2}{2\sigma^2}}\ e^{\frac{-(r2-1)^2}{2\sigma^2}}\ e^{\frac{-(r3-1)^2}{2\sigma^2}}}{e^{\frac{-(r1+1)^2}{2\sigma^2}}\ e^{\frac{-(r2+1)^2}{2\sigma^2}}\ e^{\frac{-(r3+1)^2}{2\sigma^2}}}$$

$$\left(\frac{P_r\ C_1=0\ r_1,r_2,r_3}{P_r\ C_1=1\ r_1,r_2,r_3}\right) = e^{\frac{2}{\sigma^2}(r1+r2+r3)}$$

By taking log on both sides we get,

$$L1 = \log\left(\frac{P_r\ C_1=0\ r_1,r_2,r_3}{P_r\ C_1=1\ r_1,r_2,r_3}\right) = \frac{2}{\sigma^2}(r1 + r2 + r3), \quad \ldots\ldots(10)$$

where $\frac{2}{\sigma^2}$ *is a positive factor that can be eliminated.*

The equation (10) gives the soft output for the repetition code.

SISO DECODER FOR SINGLE PARITY CHECK CODE (SPC)

In this code, a k-bit data word is changed to an n-bit code word where n = k + 1. The extra bit, called the parity bit, is selected to make the total number of 1s in the code word even. Although some implementations specify an odd number of 1s. It is a error detecting code.

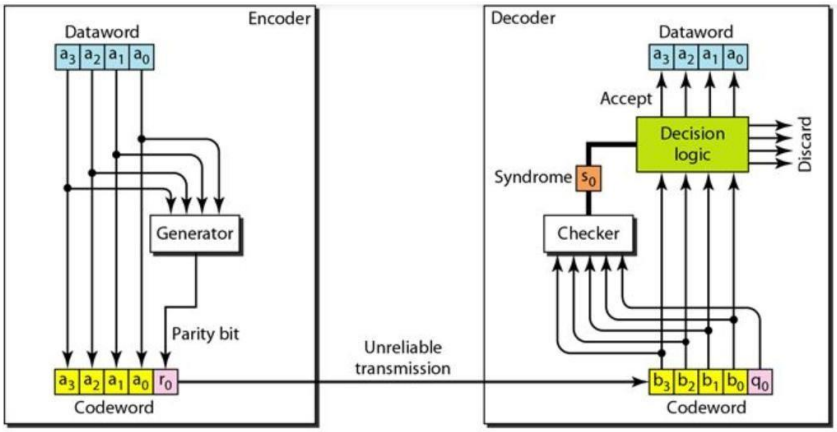
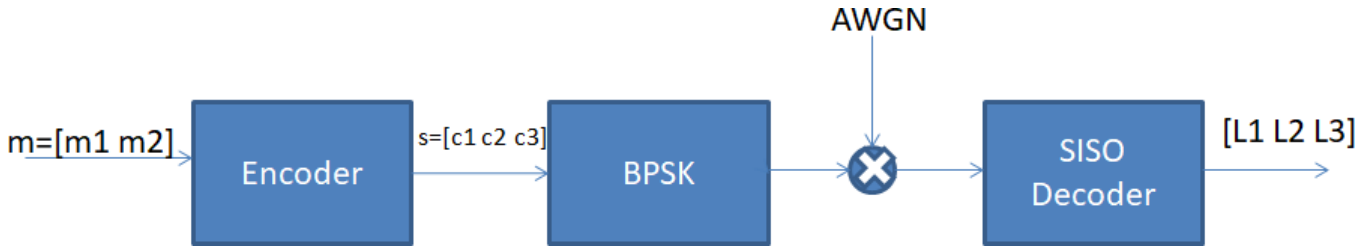


Fig SPC encoder and decoder

The encoder uses a generator that takes a copy of a 4-bit data word (a0, a1, a2 and a3) and generates a parity bit r0. The data word bits and the parity bit create the 5-bit code word. The parity bit that is added makes the number of 1s in the code word even. This is normally done by adding the 4 bits of the data word (modulo-2).

r0=a3+a2+a1+a0 (modulo-2) . The result is the parity bit. In other words, If the number of 1s is even, the result is 0; if the number of 1s is odd, the result is 1.In both cases, the total number of 1s in the code word is even. The sender sends the code word which may be corrupted during transmission. The receiver receives a 5-bit word. The checker at the receiver does the same thing as the generator in the sender with one exception: The addition is done over all 5 bits. s0=b3+b2+b1+b0+ q0 (modulo-2) . The result, which is called the syndrome, is just 1 bit. The syndrome is 0 when the number of 1s in the received code word is even; otherwise, it is 1. The syndrome is passed to the decision logic analyzer. If the syndrome is 0, there is no error in the received code word, the data portion of the received code word is accepted as the data word, if the syndrome is 1, the data portion of the received code word is discarded. The data word is not created.

Let us consider a (3,2) SPC code,



From the diagram above , we have 2 message bits [m1 m2] which is encoded into a codeword s=[c1 c2 c3] where c1=m1 , c2=m2 and c3=m1⊗ m2. BPSK modulation is then performed on the codewords and transmitted over a Gaussian channel and the received vector r [r1 r2 r3] is received. These received bits are then passed through a SISO decoder which produces [L1 L2 L3] , the beliefs about the 3 bits [c1 c2 c3].

We know that L1 is proptional to r1 which gives us the intrinsic value whereas for the extrinsic value we have to ask the question about what r2 and r3 say about c1. We know r2 says something intrinsic about c2 and similarly r3 about c3. Thereferore from the parity check condition we can say that c1= $c2$ $c3$. Now, when you add the intrinsic and extrinsic values we get the total L1 value.

We have c1 = $c2$ $c3$ and we know that l2=log ($\frac{P_r\ C_2=0\ r_2}{P_r\ C_2=1\ r_2}$) and l3=log($\frac{P_r\ C_3=0\ r_3}{P_r\ C_3=1\ r_3}$. let us assume

$P_r\ C_2\ = 0\ r_2$ is p2 and $P_r\ C_2\ = 1\ r_2$ is (1-p2) , $P_r\ C_3\ = 0\ r_3$ is p3 and $P_r\ C_3\ = 1\ r_3$ is (1-p3). We

need to find out the probability of c1=0 given r2 and r3 ie. $p1 = P_r C_1 = 0\ r_2$, r3 .

If we look at the cases of c1 c2 and c3 , we can say that c1 is zero when c2 and c3 and 0"s and also when c2 and c3 are 1"s. We can also say c1 is one when c2 and c3 are 0 and 1 respectively and also when c3 and c2 are 0 and 1 respectively.

In order to compute the extrinsic LLR ie. $\frac{p1}{1-\ p1}$ we do the following,

P1-(1-p1) = p2(p3-(1-p3)) + (1-p2)((1-p3)-p3)

P1-(1-p1) = (p2-(1-p2))(p3-(1-p3))

Divide the above equation by p1+(1-p1) and it becomes,

$$\frac{\mathrm{P1}-(1-\mathrm{p1})}{p1+(1-p1)} = \frac{p2-1-p2}{p2+(1-p2)}\ \frac{p3-1\ -p3}{p3+(1-p3)}$$

$$\frac{1-(\frac{1-p\ 1}{p1})}{1+(\frac{1-p\ 1}{p\ 1})} = \frac{1-(\frac{1-p\ 2}{p2})}{1+(\frac{1-p\ 2}{p\ 2})}\ \frac{1-(\frac{1-p\ 3}{p3})}{1+(\frac{1-p\ 3}{p\ 3})}$$

Since we are interested in the extrinsic LLR about bit 1 ie $l_{ext,1}$ = log($\frac{p1}{1-p1}$), so lets write everything in terms of the extrinsic LLR , l2 and l3.

$$\frac{1-e^{-l_{ext,1}}}{1+e^{-l_{ext,1}}} = \frac{1-e^{-l2}}{1+e^{-l2}}\frac{1-e^{-l3}}{1+e^{-l3}}$$

We know that tanh = $\frac{e^{x}-e^{-x}}{e^{x}+e^{-x}} = \frac{1-e^{-2x}}{1+e^{-2x}}$

Therefore the equation becomes,

$$\tanh\left(\frac{l_{ext,1}}{2}\right) = \tanh\left(\frac{l_2}{2}\right)\tanh\left(\frac{l_3}{2}\right)$$

This is a very famous formula for the xor. So if you have c1= c2 c3 , it results in the above equation called the tanh rule. Tanh(x) is an odd function. When x is negative , then tanh(x) is less than zero. When x is positive, tanh(x) is greater than zero. So the sign of x and the sign of tanh(x) is exactly the same. So this equation can be written in two ways 1. $\mathrm{Sgn}(l_{ext,1})=\mathrm{sgn}(l2)\mathrm{sgn}(l3)$

2. Abosulte value .

$$\tanh\left(\frac{|l_{ext,1}|}{2}\right) = \tanh\left(\frac{|l2|}{2}\right)\tanh\left(\frac{|l3|}{2}\right)$$

taking log on both sides we get,

$$\log\left(\tanh\left(\frac{|l_{ext,1}|}{2}\right)\right) = \log\left(\tanh\left(\frac{|l2|}{2}\right)\right) + \log\left(\tanh\left(\frac{|l3|}{2}\right)\right)$$

$f(|l_{ext,1}|) = f(|l2|) + f(|l3|)$

$|l_{ext,1}| = f(f(|l2|) + f(|l3|))$, this is another way to write down the tanh rule.

The problem with this SPC code is that there are a lot of non-linear components like log and tanh(x). so we use the minsum approximation to simplify this ie. f(l2) + f(l3) ≈ f(min(|l2|,|l3|). Once you make this approximation the absolute value of $l_{ext,1}$ has a very simple expression ie. $|l_{ext,1}| \approx f(f(\min(|l2|,|l3|))$. since f(f(x))=x , it becomes $|l_{ext,1}| \approx \min(|l2|,|l3|)$. so this approximation is called the minsum approximation.

SOFT-INPUT-SOFT-OUTPUT ITERATIVE MESSAGE PASSING DECODER

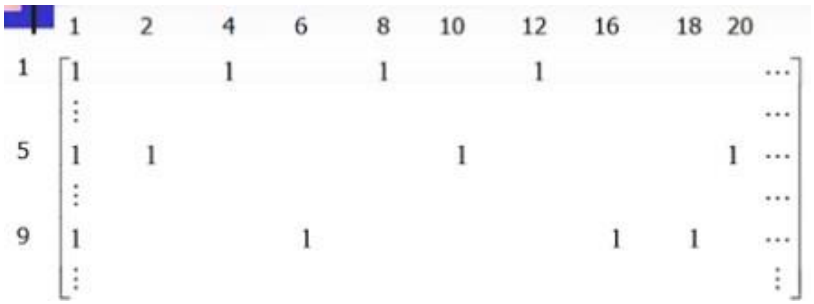
The decoder for LDPC codes is soft input soft output. It is iterative , which means it does not try to decode the entire code at once it will use some partial information from the code and do decoding and pass messages around. There is an approximation involved in this which is called the minsum approximation. What we seek from implementing the decoder is the output LLR ie. given the entire received vector what can we say about the probability of a particular bit being a zero or a one. What will happen in this decoder is we will approximately , iteratively try to improve the belief.

Sub-optimal techniques based on iterative belief propagation decoding give excellent results and can be practically implemented. The sub-optimal decoding techniques view each parity check that makes up the LDPC as an independent single parity check (SPC) code. Each SPC code is decoded separately using soft-in-soft-out (SISO) techniques such as SOVA, BCJR, MAP, and other derivates thereof. The soft decision information from each SISO decoding is cross-checked and updated with other redundant SPC decoding of the same information bit. Each SPC code is then decoded again using the updated soft decision information. This process is iterated until a valid code word is achieved or decoding is exhausted. This type of decoding is often referred to as sum-product decoding.

The decoding of the SPC codes is often referred to as the "check node" processing, and the cross-checking of the variables is often referred to as the "variable-node" processing.

In a practical LDPC decoder implementation, sets of SPC codes are decoded in parallel to increase throughput.

Let us consider the low density parity check matrix ,



PART OF A LDPC MATRIX.

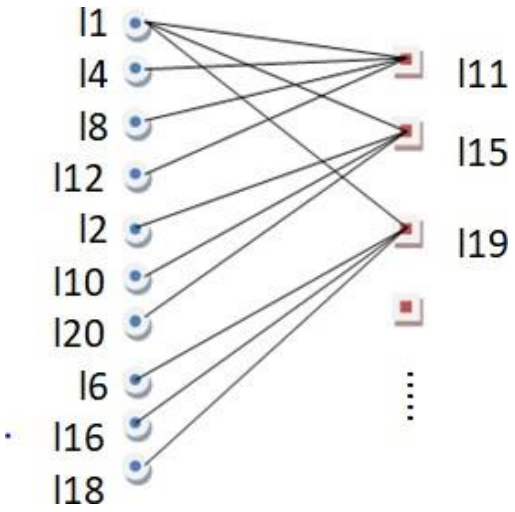
The first column has three 1"s and all zeroes. The one"s are in the 1st , 5th and 9th row. If you focus on the 1st row, it has one"s in the 1st , 4th , 8th and 12th columns. Likewise the other rows and columns also have one"s in different positions. This is the local structure.

If we are given only r1, we know what first estimate will be ie. $LLR|r1 = \frac{2}{\sigma^2} r1$. So what we do now is we try to exploit the local structure and figure out what the connections in different rows tell us. Every row of the parity check matrix actually defines a single parity check code. It gives you parity check constraint that is satisfied by one subset of the bit of codewords. From the local structure , row1 is conveys that codewords c1, c4, c8 and c12 belong to the single parity check code. So the second estimate is found by the SPC decoder. The same way row5 also defines a SPC code that involves c1 , c2 , c10 and c20. This gives you another estimate.

Similarly the other rows of the LDPC matrix give you different estimates. So every parity check in the local structure gives you more estimates for that particular bit which are calculated using the SISO decoder and compute the extrinsic information. The same can be repeated for every other bit.

But the local structure only conveys partial information because you aren‟t connected to the rest of the codeword. To make use of the codewords eddiciently we use message passing. So each code will use the local structure and then pass messages to eachother.

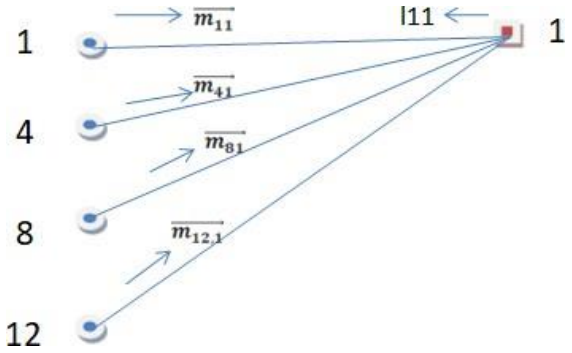
The tanner graph corresponding to the local structure is shown below.



The first iteration of the tanner graph.

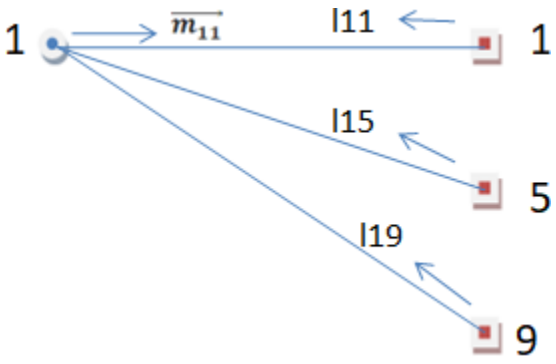
- the first estimate l1 comes from the channel.
- li passed from bit node i to all neighbouring check nodes.
- Estimates for bit 1: l_{11} , l_{15} , l_{19} are calculated at check nodes 1 , 5 and 9.
- Estimates passed from check nodes to neighbouring bit nodes.
- This is done for all the nodes in parallel.

The second iteration.



We have the check node 1 which is connected to bit node 1,4,8 and 12. The message or LLR that comes from bit node 1,4,8 and 12 is denoted as m1,1 , m4,1 ,m8,1 and m12,1 respectively. The check node one does the SPC SISO and computes l_{11}. This computation is repeated and the check node sends back l_{11} , l_4 ,l_8 and l_{12}. l_{11} uses m4,1 , m8,1 and m12,1 to compute the extrinsic LLR for bit 1 whereas l_{12} uses m1,1, m4,1, and m8,1 and computes the extrinsic LLR for bit 12. So once you have finished the SISO computation you move to the next iteration.

The third iteration.



On the bit node we have what comes from the channel ie. l1. In the first iteration we have l_{11} , l_{15} and l_{19} coming from 1st , 5th and the 9th check node respectively. What we have at the bit node is the repetition code. The same bit is repeated 4 times. Since you are getting 4 different beliefs for the same node we need to

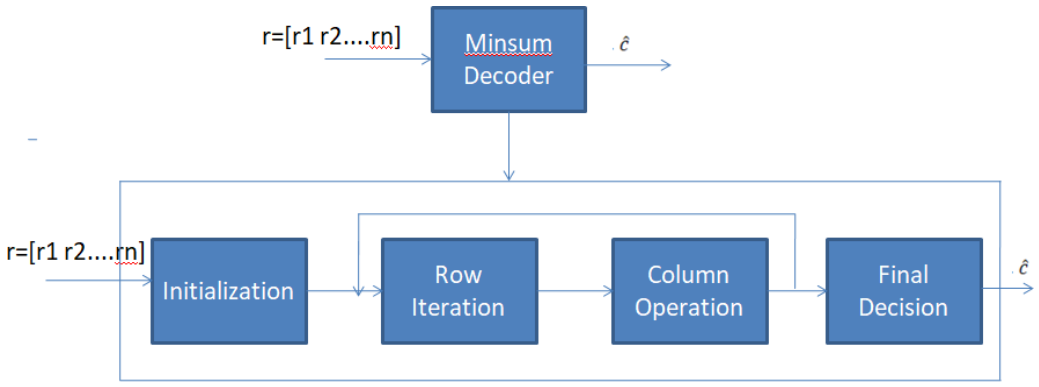
implement the SISO repetition code at the bit node. m11 = l1 + l_{15} + l_{19} ; m15 = l1 + l_{11} + l_{19} ; m19 = l1 + l_{11} + l_{15} .

The steps for the SISO iterative minsum approximation decoder is illustrated with an example.

We will consider a (4,7) parity check matrix shown below,

$$H = \begin{bmatrix} 1 & 1 & 1 & 0 & 1 & 0 & 0 \\ 0 & 1 & 1 & 1 & 0 & 1 & 0 \\ 1 & 1 & 0 & 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 & 1 & 1 & 1 \end{bmatrix}$$

We are going to focus on the minsum decoder and not the log and tanh(x) functions.



Minsun decoder

In the figure above , we have a received vector [r1,r2,……,rn] entering the minsum decoder that puts out an estimate for the codeword *c* and then we perform the initialization , row operation , column operation and then the iteration. We can perform as many iterations as we want. As the number of iterations is increased , the error rates gets improved. Once we finish the iterations we can then make a final decision. All these messages that will be getting exchanged need to stored in a storage matrix.

STORAGE MATRIX (L)

The storage matrix will be a sparse matrix with the same dimensions as a parity check matrix. For example if we consider the new radio or the 5G standard with rate ½ , the storage matrix will be (22 x 46)*48 sparse matrix. In the example shown above ie. (4,7) Parity check matrix , the storage matrix would be 4x7 sparse matrix. Just like how the L matrix has the same dimensions as parity check matrix , it also has the same

sparsity structure as the parity check matrix . Whenever the parity check matrix is zero the L will also be 0 and it can be a non-zero value only when the parity check matrix has a 1.

$$H = \begin{bmatrix} 1 & 1 & 1 & 0 & 1 & 0 & 0 \\ 0 & 1 & 1 & 1 & 0 & 1 & 0 \\ 1 & 1 & 0 & 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 & 1 & 1 & 1 \end{bmatrix}$$

$$L = \begin{bmatrix} x & x & x & 0 & x & 0 & 0 \\ 0 & x & x & x & 0 & x & 0 \\ x & x & 0 & x & 0 & 0 & x \\ x & 0 & x & 0 & x & x & x \end{bmatrix}$$

The storage matrix L will have possible non-zero values wherever is a one in the parity check matrix. If there is a zero in the parity check matrix , then the L will also be zero. There are 17 non-zero values in the storage matrix L as shown above.

INITIALIZATION STEP:

$$r = [0.2 \quad -0.3 \quad 1.2 \quad -0.5 \quad 0.8 \quad 0.6 \quad -1.1]$$

$$L = \begin{bmatrix} 0.2 & -0.3 & 1.2 & 0 & 0.8 & 0 & 0 \\ 0 & -0.3 & 1.2 & -0.5 & 0 & 0.6 & 0 \\ 0.2 & -0.3 & 0 & -0.5 & 0 & 0 & -1.1 \\ 0.2 & 0 & 1.2 & 0 & 0.8 & 0.6 & -1.1 \end{bmatrix}$$

We have a received vector from the channel r = [0.2 -0.3 1.2 -0.5 0.8 0.6 -1.1]. The next step is to place r1 in all the non zero positions of the 1st column. Similarly , all non-zero positions in the 2nd column will have r2 and so on.

ROW OPERATION:

The row operation is an inplace computation using L. For each row we need to perform the minsum SPC SISO decoder. It involves finding the 2 minimum values and the sign. Min1 = minimum absolute value of all non-zero entries in the row , Min2 = the next higher absolute value . For the sign , you first find the product of

all signs of entries in the row which will be the parity . Depending on the parity sign we either flip or not flip all the signs in that particular row.

$$L = \begin{bmatrix} 0.2 & -0.3 & 1.2 & 0 & 0.8 & 0 & 0 \\ 0 & -0.3 & 1.2 & -0.5 & 0 & 0.6 & 0 \\ 0.2 & -0.3 & 0 & -0.5 & 0 & 0 & -1.1 \\ 0.2 & 0 & 1.2 & 0 & 0.8 & 0.6 & -1.1 \end{bmatrix}$$

ROW OPERATION ON ROW 1

$$L = \begin{bmatrix} -0.3 & 0.2 & -0.2 & 0 & -0.2 & 0 & 0 \\ 0 & -0.3 & 1.2 & -0.5 & 0 & 0.6 & 0 \\ 0.2 & -0.3 & 0 & -0.5 & 0 & 0 & -1.1 \\ 0.2 & 0 & 1.2 & 0 & 0.8 & 0.6 & -1.1 \end{bmatrix}$$

If we look at the first row in L , we have absolute values 0.2 , 0.3 , 1.2 and 0.8 . so the min1 is considered as and min2 is considered to be -0.3. the overall parity is -1 by taking the product of all the signs of the entries in the row1 , which means you need to flip the signs of the entries. So in the least position ie. Min1 you replace it with the min2 value and reverse the sign. And all the other non-zero entries will be replaced with the min1 value with the signs reversed. If we look at the 2nd row in L , min1 is -0.3 and min2 is -0.5 and the overall parity is +1. So the min1 is replaced with min2 value and all other non-zero entries are replaced with min1 value ,but no signs are reversed because the parity was +1. This process is repeated for the all the rows and you get the following matrix .

$$L = \begin{bmatrix} 0.2 & -0.3 & 1.2 & 0 & 0.8 & 0 & 0 \\ 0 & -0.3 & 1.2 & -0.5 & 0 & 0.6 & 0 \\ 0.2 & -0.3 & 0 & -0.5 & 0 & 0 & -1.1 \\ 0.2 & 0 & 1.2 & 0 & 0.8 & 0.6 & -1.1 \end{bmatrix}$$

AFTER ROW OPERATION

$$L = \begin{bmatrix} -0.3 & 0.2 & -0.2 & 0 & -0.2 & 0 & 0 \\ 0 & -0.5 & 0.3 & -0.3 & 0 & 0.3 & 0 \\ -0.3 & 0.2 & 0 & 0.2 & 0 & 0 & 0.2 \\ -0.6 & 0 & -0.2 & 0 & -0.2 & -0.2 & 0.2 \end{bmatrix}$$

COLUMN OPERATION:

For the column operation we will again do the inplace computation using L. For each column , we will find the sum of all the entries in the column as well as the received value .Then the new entry will be the new sum subtracted with the old entry.

1. $Sum_j = r_j$ + sum of all entries in column j.
2. New entry = sum – (old entry).

COLUMN OPERATION ON COLUMN 1

$$r = [\,0.2 \quad -0.3 \quad 1.2 \quad -0.5 \quad 0.8 \quad 0.6 \quad -1.1]$$

$$L = \begin{bmatrix} -0.3 & 0.2 & -0.2 & 0 & -0.2 & 0 & 0 \\ 0 & -0.5 & 0.3 & -0.3 & 0 & 0.3 & 0 \\ -0.3 & 0.2 & 0 & 0.2 & 0 & 0 & 0.2 \\ -0.6 & 0 & -0.2 & 0 & -0.2 & -0.2 & 0.2 \end{bmatrix}$$

Sum = -1

$$L = \begin{bmatrix} -0.7 & 0.2 & -0.2 & 0 & -0.2 & 0 & 0 \\ 0 & -0.5 & 0.3 & -0.3 & 0 & 0.3 & 0 \\ -0.7 & 0.2 & 0 & 0.2 & 0 & 0 & 0.2 \\ -0.4 & 0 & -0.2 & 0 & -0.2 & -0.2 & 0.2 \end{bmatrix}$$

If we look at the 1st column in L , the entries are -0.3 , 0 , -0.3 and -0.6 and the value received from the channel is 0.2 . So the sum is going to be -1. Then we take the sum ie. -1 and subtract each value in the column. The same process is repeated for each column. Once we repeat the same for every column, the matrix will look as shown below.

AFTER COLUMN OPERATION

$$r = [\,0.2 \quad -0.3 \quad 1.2 \quad -0.5 \quad 0.8 \quad 0.6 \quad -1.1]$$

$$L = \begin{bmatrix} -0.3 & 0.2 & -0.2 & 0 & -0.2 & 0 & 0 \\ 0 & -0.5 & 0.3 & -0.3 & 0 & 0.3 & 0 \\ -0.3 & 0.2 & 0 & 0.2 & 0 & 0 & 0.2 \\ -0.6 & 0 & -0.2 & 0 & -0.2 & -0.2 & 0.2 \end{bmatrix}$$

$$Sum = [\,-1 \quad -0.4 \quad 1.1 \quad -0.6 \quad 0.4 \quad 0.7 \quad -0.7\,]$$

$$L = \begin{bmatrix} -0.7 & -0.6 & 1.3 & 0 & 0.6 & 0 & 0 \\ 0 & 0.1 & 0.8 & -0.3 & 0 & 0.4 & 0 \\ -0.7 & -0.6 & 0 & -0.8 & 0 & 0 & -0.9 \\ -0.4 & 0 & 1.3 & 0 & 0.6 & 0.9 & -0.9 \end{bmatrix}$$

Before we computed the 1st iteration , the received vector r was the belief for the codewords. Now , after computing the 1st iteration , the sum vector is the updated belief. The L matrix after the 1st iteration will be the message that will be passed from the bit node to the check node for the 2nd iteration. If we notice carefully ,

the 1st bit in the received vector r ie. 0.2 , we would"ve decided that the bit *c* is 0 . but , if you notice the 1st bitin the updated vector ie. -1 , we would"ve decided that bit *c* is 1. If the same process is repeated for a number of times , the belief will be improved.

DECISION MAKING

Once we have the updated vector we can make decisions as follows,

- If $Sum_j > 0$, decision on bit j is 0.
- If $Sum_j < 0$, decision on bit j is 1.
- Assuming BPSK , 0 is mapped to +1 and 1 is mapped to -1.

After first iteration,

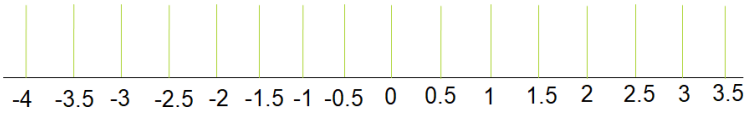
Sum = [-1 -0.4 1.1 -0.6 0.4 0.7 -0.7]

Dec = [1 1 0 1 0 0 1]

More the number of iterations , the better will be the performance .

FIXED POINT QUANTIZATION

Min-Sum decoding is a form of simplified BP decoding, with which the implementation complexity is reduced. While float-point calculation is still used in Min-Sum decoding, which makes hardware implementation a puzzle again. Consequently in term of design and implementation of LDPC decoder, fixed-point number is applied instead of float-point number in this paper. To implement high speed data transmission and achieve a higher throughout, quantization schemes are often applied for representation of information transmission and reception in decoding. The common practice is to quantify the received LLR information to an integer with uniform quantization and round the middle variables, thus the complexity is reduced with integer calculation. For the sake of reducing quantization error, a quantization scheme of joint integer value and fractional value is designed where the integer part of the received LLR information from channel is quantified with a bit and the fractional part is quantified with a single bit. In this way a (,1) a quantization may denote a uniform quantization with interval of 0.5 and quantization region of . That is, the length of the fixed-point– – – – –1 1 1 (2 ,2 2) a a number is 1+a . As 0 can be regarded as a positive integer in signed values, the region is symmetrical then. For example, if there is 3=a , the quantization region can be denoted by , which can be seen is figure below.



Region Of (3,1) Quantization

Other than whole integer quantization scheme, the integer and fractional value quantization is far more precise, thus the BER performance approaches that of float-point calculation more. Moreover a two-stage fixedpoint quantization is designed for Min-Sum decoding to achieve lower complexity. Firstly a (,1) a uniform quantization is performed with channel likehood information, then a second stage (,1) b uniform quantization is performed with information transmission between check nodes and variable nodes. For information calculation of variable nodes, information amplitude of each bit increases as the iteration decoding performs, thus the dynamic range of information increases to some extent. Consequently, when it comes to the second stage of fixedpoint quantization, the width is usually larger than that of channel receiver, say. While when the performance>b a <of the first stage of quantization is good enough, b a is a better choice for lower complexity.

CHAPTER 6

RESULTS

PEFORMANCE COMPARISON OF LDPC AND TURBO CODES

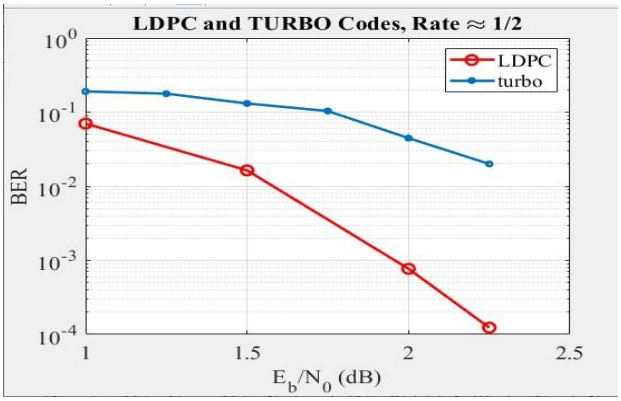
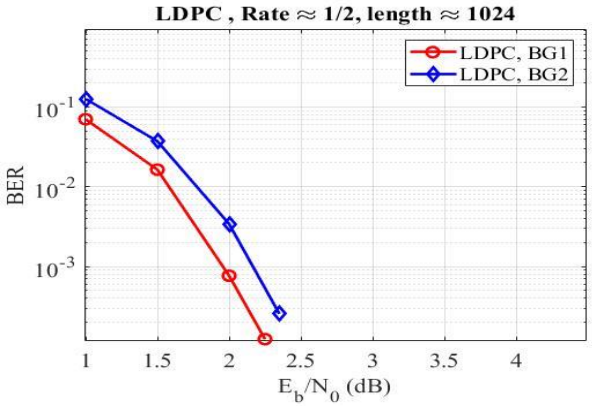


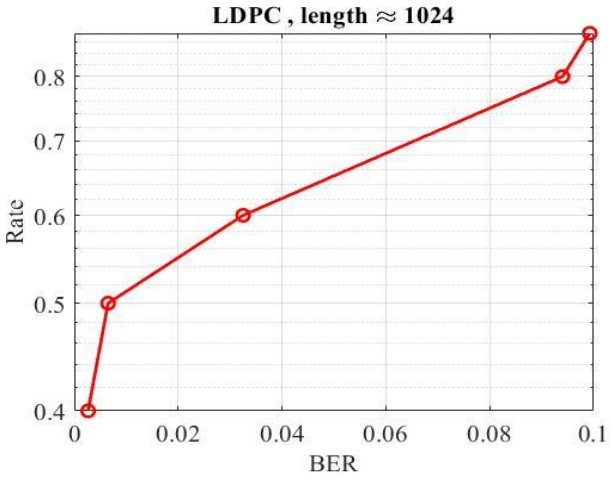
Fig.1 BER versus E_b/N_o(db)

For the performance of the LDPC and Turbo codes, a simulation is made for turbo code with rate ½ and compared with the performance of LDPC with rate ½ and the result of comparison is shown in Fig.1. It is seen that the performance of LDPC is better than the performance of turbo codes and also LDPC out performs turbo codes at higher data rates.



BER versus Eb/No for different base matrix

The iterations in the decoder of Turbo codes are fixed, which implies that the amount of time consumed in the decoding and the bit rate out of the decoder, are both constant quantities. In the LDPC decoder, when a legal codeword is found the decoder stops, denoting that there is a potential for reducing the amount of work to be done relative to Turbo codes. Higher the S/N ratio, faster the LDPC decoder. The LDPC codes may be implemented in parallel which is one of the main advantages.



Rate varsus BER

In Fig.3, we present error performance comparisons between different rates in LDPC codes. The results shown give the information bit error rate (BER) versus Rate. It is seen that the performance of LDPC is better than the performance of turbo codes and also LDPC out performs turbo codes at higher data rates. The results demonstrate that LDPC is better used for 5G codes.

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

An appropriate Forward error correction Scheme is vital for error free communication. LDPC is a powerful FEC code used for error correction. But Performance of LDPC depends on its design and selection of decoding algorithm. The BER performance obtained after decoding of LDPC was found to be good at the cost of computation .The comparison is performed between the BER obtained by turbo codes and LDPC Codes at a given code rate. The results obtained showed that the performance of LDPC codes were better than Turbo codes because of which it can be used as a channel coding code in the 5G standard .It supports the EMBB use in the case of 5G standard.

The work can be extended to check the decoder performance for different types of images for a range of code rates and comparative rates for different code rates.

CHAPTER 8

REFERENCES

[1]Michel Zorzi,Performance of FEC and ARQ Error Control IN Busty Channel Under Delay constmints, VTC'98. OTTAWA Canada May 18-21, 1998.

[2]C. E. Shannon, A Mathematical Theory of Communications, Bell Systems Technology Journal. pages 379-423, 623-657, 1948.

[3]R. Gallager, Low Density Parity Check Codes, IRE Transactions on Information Theory, vol-8. no.1, pp21-28, January 1962.

[4] Agiel N. Almaamory, Husam Abduldaem Mohammed, Performance Evaluation and Comparison Between LDPC and Turbo Coded MCCDMA. Joumal of Engineering, vol. 18. no. 8, April 20i 2.. 2nd ed., January 2002.

[5] European telecommunications standards institute, digital video broadcasting (dvb) second generation framing structure for broadband satellite applications. Pages 302-307 v1.1.I., URL: www.dvb.org.

[6]B. Vasic . Ivan B. Djordjevic, Low density parity check code and iterative decoding for long haul optical communication system. Journal of light wave technology , vol.21.no.2. February 2003.

[7] M. M Jadhav, AnkitPancholi, Dr. A. M Sapkal. Analysis and Implementation of Soft Decision Decoding Algorithm of LDPC,Intemational Journal of Engineering Trend and T Michel Zorzi, Performance of FEC and ARQ Error Control IN Bursty Channel Under Delay Constraints, VTC'98, OTTAWA Canada May 18-21, 1998.

[8] R. G. Gallager, Low Density Parity-Check Codes. MIT Press, Cambridge, MA, 1963.

[9]M.Luby, M. Mitzenmacher, and A. Shokrollahi ,\Analysis of random processes via and-or tree evaluation," in Procecdings of the 9th Annual ACM-SIAM Symposium on Discrete Algorithms,pp. 364{373, 1998.

[10] M.Luby, M. Mitzenmacher, A. Shokrollalli. and D. Spielman, \Analysis of low density codes and improved designs using irregular graphs," IEEE Trans. Inform. Theory, vol. 47, pp. 585{598,2001.

[11] T. Richardson and R. Urbanke, \The capacity of low-density parity check codes under message-passing decoding." IEEE Trans. Inform. Theory, vol. 47, pp. 599(618, 2001.

[12] HUAAN LI1 , BAOMING BAI1 , (Member, IEEE), XIJIN MU2 , JI ZHANG1 , and HENGZHOU XU3 , Algebra-Assisted Construction of Quasi-Cyclic LDPC Codes for 5G New Radio , Institute of Computing Technology, Chinese Academy of Sciences, Beijing 100190, China.

[13] Tom Richardson and Shrinivas Kudekar, Design of Low-Density Parity Check Codes for 5G New Radio, March-2018.