Visvesvaraya Technological University, Belagavi.

PROJECT REPORT

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"Neural Amplifier Design for Brain Machine Interface"

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CERTIFICATE

This is to Certify that the dissertation work **"Neural Amplifier Design for Brain Machine Interface"** carried out by Shivam Kumar(1CR16EC157), Sakshi Suman(1CR16EC145), Sagarikaa Sinha(1CR16EC143) bonafide students of **CMRIT** in partial fulfillment for the award of **Bachelor of Engineering** in **Electronics and Communication Engineering** of the **Visvesvaraya Technological University, Belagavi,** during the academic year **2019-20**. It is certified that all corrections/suggestions indicated for internal assessment have been incorporated in the report deposited in the departmental library. The project report has been approved as it satisfies the academic requirements in respect of Project work prescribed for the said degree.

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Chapter 1

INTRODUCTION

1.1 Introduction

The human brain is made up of billions of interconnected neurons; the patterns of interaction between these neurons are represented as thoughts and emotional states i.e. how we think, and feel, and act. The neuron is the basic building block of the brain and central nervous system. A neuron is an electrically excitable cell that processes and transmits information by **electrochemical signaling.** Each neuron may be connected to up to 10,000 other neurons, passing signals to each other via as many as 1,000 trillion **synaptic connections**, equivalent by some estimates to a computer with a 1 trillion bit per second process.

A typical neuron possesses a **soma** (the bulbous cell body which contains the cell nucleus), **dendrites** (long, feathery filaments attached to the cell body in a complex branching "dendritic tree", receive messages for the cell) and a single **axon** (a special, extra-long, branched cellular filament which transmits messages from the cell).

Every neuron maintains a **voltage gradient** across its membrane, due to metabolically-driven differences in **ions o**f sodium, potassium, chloride and calcium within the cell, each of which has a different charge. If the voltage changes significantly, an electrochemical pulse called an action potential (APs or nerve impulse) and Local field potential (LEP) is generated. APs have amplitudes ranging from 5 μVpp to 50 μVpp, across frequencies of 300 Hz to 7.5 kHz, whilst LFP amplitudes are around 1 mVpp to 10 mVpp, across a range of 25 mHz to 100 Hz, this electrical activity can be measured and displayed as a waveform called **brain wave** or **brain rhythm**.

This pulse travels rapidly along the cell's axon and is transferred across a specialized connection known as a **synapse** to a neighboring neuron, which receives it through its feathery dendrites. A synapse is a complex membrane junction or gap (the actual gap, also known as the **synaptic cleft**) used to transmit signals between cells, and this transfer is therefore known as a **synaptic connection**.

The interactions of neurons are not merely electrical, though, but **electro-chemical**. Each axon terminal contains thousands of membrane-bound sacs called **vesicles**, which in turn contain thousands of **neurotransmitter molecules** each. Neurotransmitters are chemical messengers which relay, amplify and modulate signals between neurons and other cells.

When stimulated by an electrical pulse, neurotransmitters of various types are released, and they cross the cell membrane into the synaptic gap between neurons. These chemicals then bind to chemical **receptors in** the dendrites of the receiving (post-synaptic) neuron. This affects the potential charge of the receiving neuron, which then starts up a new electrical signal in the receiving neuron. Each individual neuron can form thousands of links with other neurons in this way, giving a typical brain well over 100 trillion synapses.

A **brain-machine interface (BMI)** or brain-computer interface (BCI), also called mind-machine interface (MMI), and sometimes also known as neural-control interface (NCI), is a direct communication pathway between an enhanced or wired brain and an external device. BCI differs from neuromodulation in that it allows the information flow to be bidirectional. This application is often used for research purposes, augmenting, or repairing human cognitive or sensory-motor functions.

BMI uses brain activity to command, control, actuate and communicate with the world directly through brain integration with peripheral devices and systems. The field of BMI has emerged mostly towards neuroprosthetics applications that mainly concentrate on restoring damaged hearing, sight and movement. The main principle behind this interface is the bioelectrical activity of nerves and muscles.

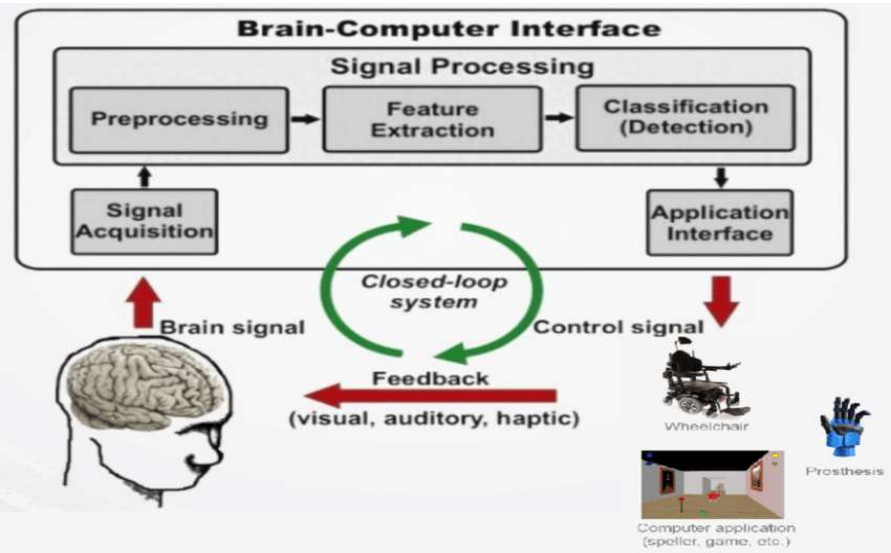

Fig 1.1.1: Block diagram of BMI

These systems are essentially composed by a set of microelectrodes to capture the neural activity, followed by a bank of low-noise amplifiers (LNAs) for signal conditioning and a mixed-signal circuitry to digitize and process the acquired data prior to wireless transmission. A key element in this architecture is the LNA which must be able to boost the weak signals detected by the microelectrodes and filter out the undesired frequency components, under severe area and power consumption constraints.

The block diagram of the Brain Machine Interface is shown in Fig.1.1.1. In the diagram shown, the circuit implemented in this project that is the low noise amplifier is a part of the signal processing block.

There is a great demand for technologies that enable neuroscientists and clinicians to observe the simultaneous activity of large numbers of neurons in the brain. Multielectrode neural recordings are becoming standard practice in basic neuroscience research, and knowledge gained from these studies is beginning to enable clinical and neuroprosthetic applications.

Ultra-low noise and ultra-low power neural amplifiers are extremely important in recording BMIs since one such amplifier is needed for each electrode. A low-noise amplifier (LNA) is an electronic amplifier that amplifies a very low-power signal without significantly degrading its signal-to-noise ratio. A typical amplifier increases the power of both the signal and the noise present at its input, whereas LNAs are designed to amplify a signal while minimizing additional noise. Designers can minimize additional noise by using low-noise components, operating points, low-power and circuit topologies. Minimizing additional noise must balance with other goals such as power gain and impedance matching.

The **operational transconductance amplifier** (**OTA**) is an amplifier whose differential input voltage produces an output current. Thus, it is a voltage controlled current source (VCCS). There is usually an additional input for a current to control the amplifier's transconductance. The OTA is similar to a standard operational amplifier in that it has a high impedance differential input stage and that it may be used with negative feedback.

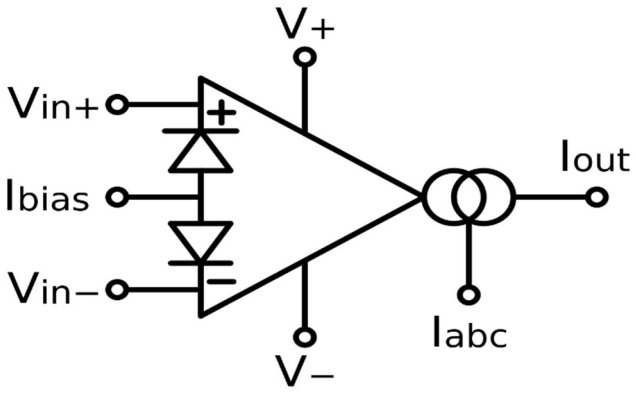

Fig 1.1.2: Schematic Symbol of OTA

In the ideal OTA, the output current is a linear function of the differential input voltage, calculated as follows:

$$I_{out} = (V_{in+} - V_{in-}) \cdot g_m \quad 1.1$$

Where,

V_{in+} is the voltage at the non-inverting input,

V_{in-} is the voltage at the inverting input and

g_m is the transconductance of the amplifier.

The amplifier's output voltage is the product of its output current and its load resistance:

$$V_{out} = I_{out} \cdot R_{load} \quad 1.2$$

The voltage gain is then the output voltage divided by the differential input voltage:

$$G_{voltage} = \frac{Vout}{Vin+ - Vin-} = R_{load} \cdot g_m \quad 1.3$$

The transconductance of the amplifier is usually controlled by an input current, denoted I_{abc} ("amplifier bias current"). The amplifier's transconductance is directly proportional to this current. This is the feature that makes it useful for electronic control of amplifier gain. The current Iabc (**a**mplifier **b**ias **c**urrent) is the quantity which directly controls the "open-loop-gain" gm. There are many applications for OTA devices, for example in filter and oscillator circuits. In most cases, OTA`s are also operated with negative feedback. Because - in contrast to voltage op amps - the "open-loop" function is finite, the value of gm appears in the formulas for the closed-loop gain - hence, the transconductance (resp. the controlling current Iabc) can be used to control/tune the gain or other filter/oscillator parameters.

1.2 Objective

Large scale chronic multi-electrode neural recording and stimulating systems have emerged as an important experimental paradigm for investigating brain function.

Low Noise Neural amplifiers are used for amplifying low amplitude neural spikes in Neural recording systems from the millihertz range to 7 kHz. The need for low noise is emphasized by the presence of background noise during recording. Additionally, the need of a greater number of recording sites and avoiding of excessive heating has given rise to low area and power requirement.

The objective of the work is to design on ultra-low-power and ultra-low noise neural amplifier for brain–machine interfaces, while rejecting large dc offsets generated at the electrode–tissue interface with applications for paralysis prosthetics, stroke, Parkinson's disease, epilepsy, prosthetics for the blind, and experimental neuroscience systems. The circuits include a micropower neural amplifier with adaptive power biasing for use in multi-electrode arrays.

Chapter 2

LITERATURE SURVEY

1. Mohseni P, Najafi K (2004) "A fully integrated neural recording amplifier with DC input stabilization**" IEEE Trans Biomed Eng (2004)**

The work proposed a low-power low-noise fully integrated bandpass operational amplifier for a variety of biomedical neural recording applications. A standard two-stage CMOS amplifier in a closed-loop resistive feedback configuration provides a stable ac gain of 39.3 dB at 1 kHz. A subthreshold PMOS input transistor is utilized to clamp the large and random dc open circuit potentials that normally exist at the electrode-electrolyte interface a neural operational amplifier. The article presents Neural Amplifier having **open loop architecture with improved dc response and sufficiently high gain.**

The tolerable dc input range is measured to be at least 0.25 V with a dc rejection factor of at least 29dB. The amplifier occupies 0.107 mm2 in die area, and dissipates 115 W from a 3 V power supply. The amplifier provides a mid-band gain of 51dB without amplifying the dc frequency components. The amplifier is shown to tolerate 400mV of dc input voltage(0-400mV) without sacrificing the ac performance.

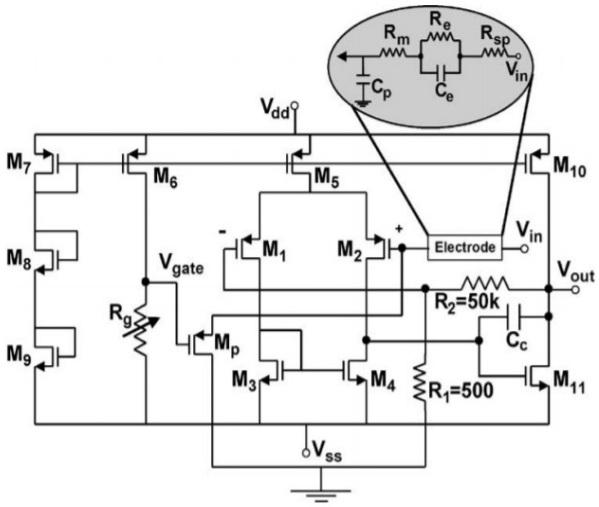

Fig 2.1 Schematic of Neural Recording Amplifier

However, the major limitations of their work include a very high-power consumption and higher noise as compared to present state of art design.

2.“An Energy-Efficient Micropower Neural Recording Amplifier**” Woradorn Wattanapanitch, Student Member, IEEE, Michale Fee, and Rahul Sarpeshkar, Senior Member, IEEE 2007**

The work describes an ultra-low-power neural recording amplifier. When configured for recording neural spikes, the amplifier yielded a midband gain of 40.8 dB and a 3-dB bandwidth from 45 Hz to 5.32 kHz; the amplifier’s input-referred noise was measured to be 3.06 Vrms while consuming 7.56 W of power from a 2.8-V supply corresponding to a noise efficiency factor (NEF) of 2.67 with the theoretical limit being 2.02.When configured for recording LFPs, the amplifier achieved a midband gain of 40.9 dB and a 3-dB bandwidth from 392 mHz to 295 Hz; the input-referred noise was 1.66 Vrms while consuming 2.08 W from a 2.8-V supply corresponding to an NEF of 3.21. The amplifier was fabricated in AMI’s 0.5- m CMOS process and occupies 0.16 mm2 of chip area.

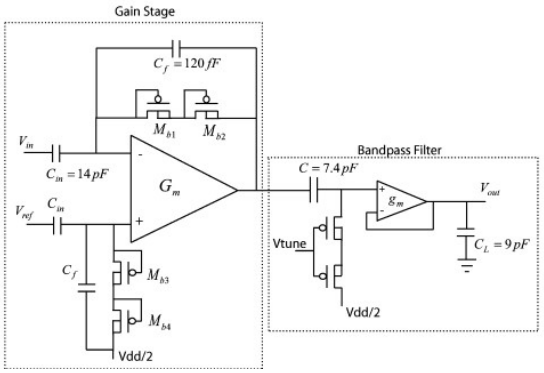

Fig.2.2: Overall system schematic of the neural amplifier.

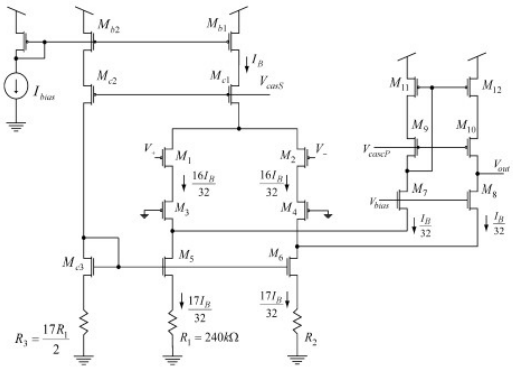

Fig.2.3: Schematic of the low-noise OTA used in this design

The design however failed to meet the very low power criteria which is essential for wearables and implantable sensors. Another limitation of this work is the use of conventional folded cascade OTA for realizing the gain stage. The conventional folded cascode OTA requires additional area for bias circuitry and also has low output swing.

3. “An Area-Efficient Noise-Adaptive Neural Amplifier in 130 nm CMOS Technology**” Vikram Chaturvedi, Student Member, IEEE, and Bharadwaj Amrutur, Member, IEEE, 2011**

The work proposed a neural amplifier in UMC 130 nm, 1P8M complementary metal–oxide semiconductor (CMOS) technology. It can be biased adaptively from 200 nA to 2 modulating input referred noise from 9.92 to 3.9. They also describe a low noise design technique with the use of current stealing technique which minimizes the noise contribution

of the load circuitry. Optimum sizing of the input transistors minimizes the accentuation of the input referred noise of the amplifier and obviates the need of large input capacitance. The amplifier achieves a noise efficiency factor of 2.58. The amplifier can pass signal from 5 Hz to 7 kHz and the bandwidth of the amplifier can be tuned for rejecting low field potentials (LFP) and power line interference. The amplifier achieves a mid-band voltage gain of 37dB.

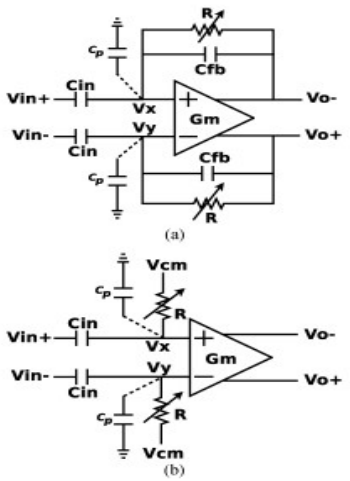

Fig.2.4 :(a) Closed loop neural low noise amplifier.
(b) Open loop neural low noise amplifier.

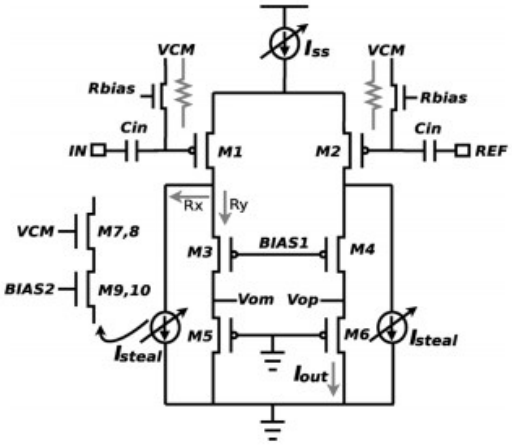

Fig.2.5: Schematic of the neural amplifier.

4. "A 0.8 V CMOS OTA and Its Application in Realizing a Neural Recording Amplifier**" Shashank Dwivedi and A. K. Gogoi, Department of Electronics and Electrical Engineering/Indian Institute of Technology Guwahati,2015**

The work presents a low-voltage, low power CMOS symmetrical operational transconductance amplifier (OTA), the linear range of OTA is increased by employing multi-tanh differential configuration and source degeneration while the common mode range is enhanced using DC-shifting scheme, but this resulted in very low mid band gain and low bandwidth. The proposed symmetrical OTA is operated with a single power supply of 0.8 V and shows an open loop gain of 31.6 dB with unit gain bandwidth of 202.3 KHz and using a 7 pF of load capacitor. A neural preamplifier was implemented in moderate inversion region using the proposed OTA. The preamplifier achieves 34.5 dB of gain consuming 77.1 μW of power and has an input referred noise of 24.18 μVrms over 8.9 KHz of bandwidth.

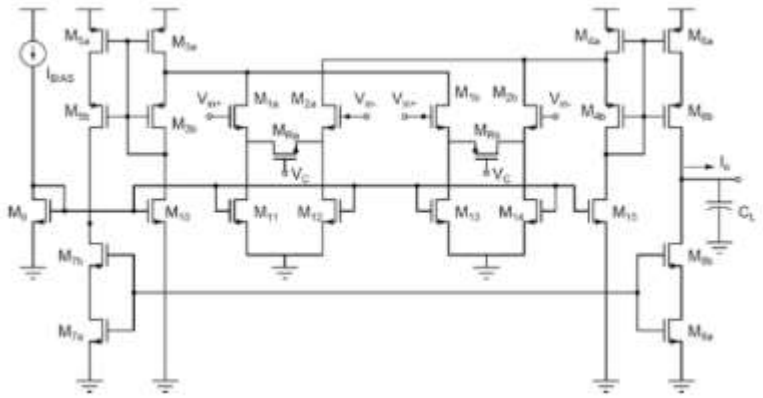

Fig.2.6: Subthreshold OTA with symmetric multi-stage balanced operation

5. Ruiz-Amaya J, Rodriguez-Perez A, Delgado-Restituto M (2015) "A low noise amplifier for neural spike recording interfaces**"**

The paper proposed a low noise neural spike recording amplifier using capacitive feedback using a two-stage OTA, efficiently solves the triple trade-off between power, area and noise. They worked with Capacitive Feedback Network (CFN), Miller Integrator Feedback Network, Capacitive Amplifier Feedback Network, Open Loop Network (OLN) and Miller Compensated Capacitive Feedback Network (MCCFN).

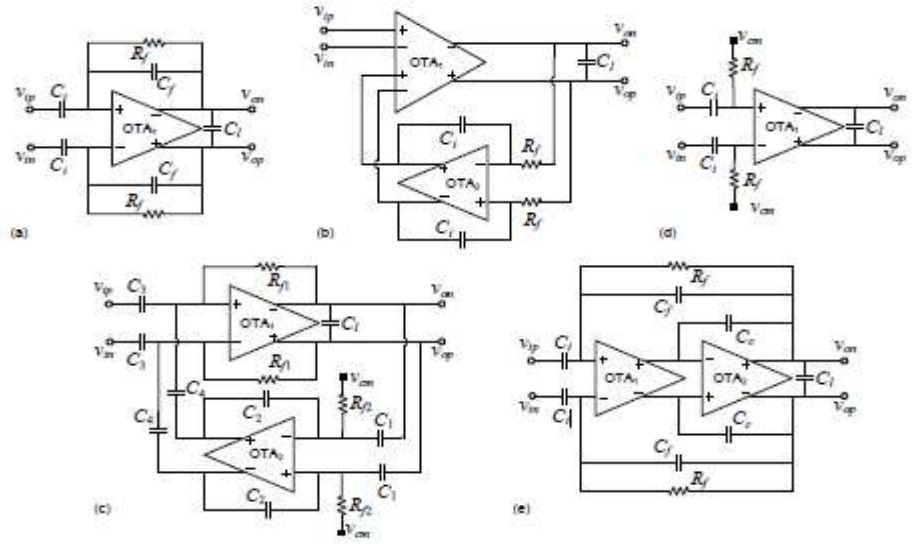

Fig 2.7: LNA architectures reviewed: (a) CFN; (b) MIFN; (c) CAFN; (d) OLN; and (e) MCCFN approaches.

- CFN Topology

In this simple architecture, the high-pass pole frequency is obtained by the feedback resistor (Rf) and capacitor (Cf), whereas the low-pass pole frequency is determined by the OTA1 response. The mid band gain is given by the capacitor ratio Ci=Cf, as long as the OTA DC gain is much higher than Mbg.

- MIFN Topology

In this approach, the high-pass roll-off of the bandpass characteristic is implemented by an active integrator placed in a feedback path around OTA1. The low-pass corner frequency is again determined by the frequency response of OTA1, and the mid band gain is directly given by the DC gain of this amplifier. This feature allows high mid band gains without resorting to large capacitor ratios, however, strong variations in Mbg can be expected due.

- CAFN Topology

In this architecture, the mid band gain is obtained by two capacitor ratios (C2=C1 and C3=C4) using a second capacitive amplifier in the feedback loop. Capacitor C3 must be large in order to reduce the input-referred noise. In practice, this translates into a highC3=C4 ratio which forces C2=C1 to take low values for a given mid band gain specification. This implies that $\beta 1 << \beta 2$, so that factor 2 can be usually neglected.

- OLN Topology

An open-loop OTA is used in this approach to directly amplify the neural signal [38]. The high-pass pole frequency is determined by an input decoupling capacitor Ci together with a resistor Rf which in turn sets the input common-mode voltage of the OTA. The low-pass corner frequency is again determined by the OTA response. In spite of its simplicity, the mid band gain is subject to large variations since it is determined by the OTA DC gain.

- MCCFN Topology

This architecture is similar to the CFN topology except that the OTA is implemented by means of two amplifier stages. In some realizations a Miller capacitor Cc is used to guarantee stability by moving non-dominant poles of the LNA to higher frequencies but, in others, no Miller compensation is employed. The MCCFN topology offers a good trade-off between output swing, DC gain, noise and power consumption

6. "A High Input Impedance Low Noise Integrated Front-End Amplifier for Neural Monitoring**" Zhijun Zhou and Paul A. Warrthe, 2016**

The work key focus is on FEA (Front End Amplifier) which ensures a high input impedance. The front-end amplifier forms the critical element for signal detection and preprocessing, which determines the fidelity of the biosignal, but also impacts power consumption and size. In this paper, a novel combined feedback loop-controlled approach is proposed to compensate for input leakage currents generated by low noise amplifiers when in integrated circuit form alongside signal leakage into the input bias network.

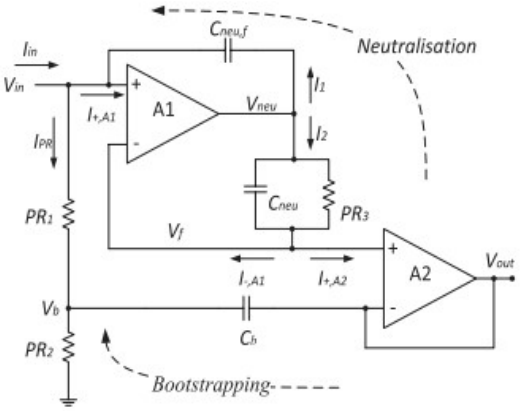

Fig.2.8: Circuit topology of proposed FEA design with bootstrapping and neutralisation loop.

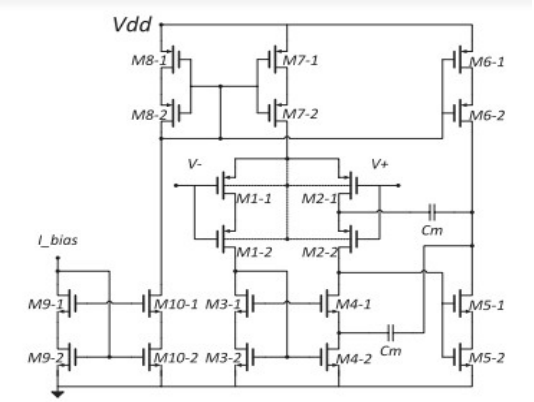

Fig.2.9: Circuit schematic of CMOS low with bootstrapping and neutralisation loop.

In Fig. 2.8, the proposed FEA includes two low-noise two- stage Complementary Metal-Oxide Semiconductor (CMOS) amplifiers (A1 and A2,) and two feedback loops, on each for neutralisation (to address the leakage current of amplifier) and bootstrapping (to address current into bias network. Pseudo Resistors (PR) are used in the design.

7. Ng KA, Xu YP (2016) "A low-power, high CMRR neural amplifier system employing CMOS inverter-based OTAs with CMFB through supply rails**" IEEE 2016**

The work proposed another neural amplifier using capacitive feedback technique. This study reports a multichannel neural amplifier system that eliminates this impedance mismatch problem by using **single-ended CMOS-inverter-based preamplifiers** for both the reference and signal inputs.

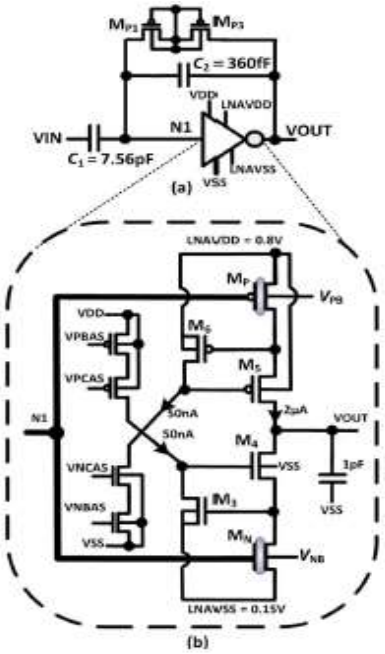

Fig.2.10: (a) CC_LNA implemented with CI_OTA. (b) Schematic of CI_OTA.

Since, inverter-based OTA design results in poor CMRR, **an additional CMFB network** was employed to improve the CMRR. However, this was achieved at the expense of higher area.

8. "Design of high gain, high bandwidth neural amplifier IC considering noise-power trade-off" N. **M. Laskar, K. Guha, S. Nath, S. Chanda, K. L. Baishnab, P. K. Paul, K. S. Rao Springer (2018)**

In this paper, the design of a neural amplifier IC consisting of two high performance neural amplifiers for recording action potentials/spikes are proposed. One amplifier is based on capacitive feedback topology and is noise efficient while the other one is based on open loop topology and is area as well as power efficient. Both amplifiers use a self-biased high swing cascode current mirror load based Folded Cascode Operational Transconductance Amplifier (OTA), which results in an efficient performance with a trade-off between noise and power. The use of such a current mirror load in the OTA helps in achieving a better output swing, improvement in gain, CMRR and bandwidth.

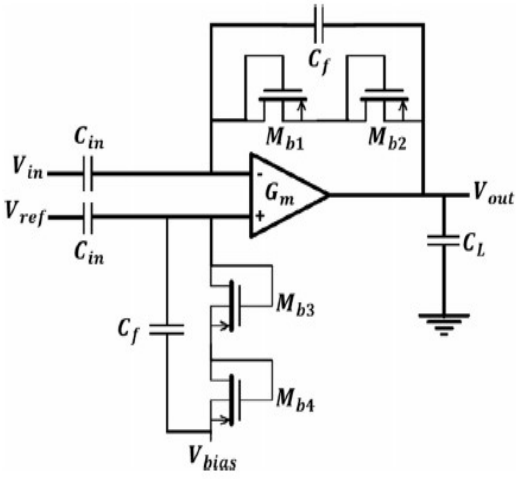

Fig.2.11: Overall schematic of closed loop neural amplifier

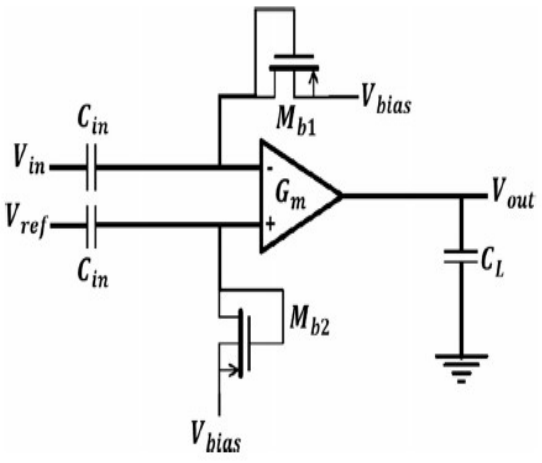

Fig.2.12: Overall schematic of open loop neural amplifier

Thus, it can be seen that the major limitations of most of these works is that they cannot meet the stringent requirement of ultra-low power as well as ultra-low noise at the same time. It has been observed that most of the reported works use the capacitive feedback topology rather than the open loop one, although open loop technique offers lower area and lower power. This is because open loop topology results in a comparatively higher input referred noise, which is a figure of merit for neural amplifiers.

Chapter 3

HARDWARE

3.1 Basics Of MOSFET

MOSFET, is a four-terminal device. The figure shown is the general representation of an N-MOS (for PMOS, simply replace N regions with P and vice-versa). MOS is a Voltage-controlled current source as the current through MOS is a function of relative voltage levels of its terminals. The relative voltages of gate, drain and source terminals (assuming bulk or substrate to be at same voltage as source) determine the magnitude of current flowing in MOS. In each of these regions, we can represent the current as a function of gate-to-source voltage (VGS) and drain-to-source voltage (VDS).

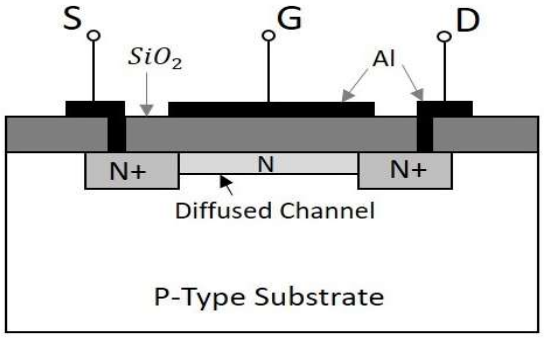

Fig. 3.1.1: Structure of N-channel MOSFET

In a MOS device, the current flows on formation of channel of carriers between source and drain terminals. For this, voltage at gate terminal needs to be such that it attracts carriers of appropriate type towards itself. When sufficient carriers are attracted towards gate, channel is said to be formed. A current, then, flows between source and drain terminals depending upon the voltage levels of these terminals. The voltage level of substrate also impacts the magnitude of current as it also determines the level of carriers in the channel.

For an N-MOS device, the channel is formed by electrons. So, to attract electrons, gate voltage must be greater than source voltage. For the formation of channel, the difference between VG and VS (VG – VS) must be greater than Vth (threshold voltage of the MOS). Threshold voltage is defined as the minimum difference in gate-to-source voltage needed for the formation of channel in a MOS device. For NMOS, Vth is positive as for channel formation gate needs to be at higher voltage as explained above. Similarly, for PMOS, Vth is negative as gate needs to be at lower voltage than source for channel to be formed.

On increasing gate voltage beyond threshold voltage, current through MOS increases with increasing gate voltage. Also, if we increase drain voltage keeping gate voltage constant, current increases till a particular drain voltage. After that, increasing drain voltage does not affect the current. Depending upon the relative voltages of its terminals, MOS is said to operate in either of the cut-off, linear or saturation region.

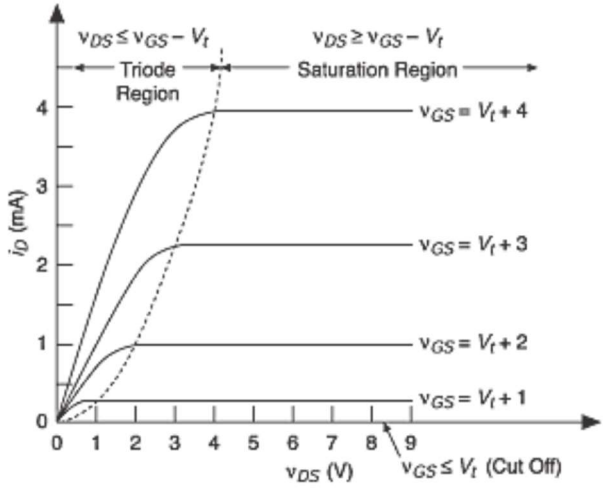

Fig.3.1.2: Output Characteristics of MOSFET

- Cut off region – A MOS device is said to be operating when the gate-to-source voltage is less than Vth. Thus, for MOS to be in cut-off region, the necessary condition is –

$$0 < V_{GS} < V_{th} \text{ - for NMOS} \quad 3.1$$

$$0 > V_{GS} > V_{th} \text{ - for PMOS (threshold voltage is negative)} \quad 3.2$$

Cut-off region is also known as sub-threshold region. In this region, the dependence of current on gate voltage is exponential. The magnitude of current flowing through MOS in cut-off region is negligible as the channel is not present. The conduction happening in this region is known as sub-threshold conduction.

- Linear or non-saturation region – For an NMOS, as gate voltage increases beyond threshold voltage, channel is formed between source and drain terminals. Now, if there is voltage difference between source and drain, current will flow. The magnitude of current increases linearly with increasing drain voltage till a particular drain voltage determined by the following relations –

$$V_{GS} \geq V_{TH} \quad 3.3$$

$$V_{DS} < V_{GS} - V_{TH} \quad 3.4$$

The current is then represented as a linear function of gate-to-source and drain-to-source voltages. That is why, MOS is said to be operating in linear region. The linear region voltage-current relation is given as follows:

$$I_D = \mu Cox\frac{W}{L}((V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2})) \quad 3.5$$

Similarly, for P-MOS transistor, condition for P-MOS to be in linear region is represented as:

$$V_{GS} < V_{TH} \text{ (OR) } V_{SG} > |V_{TH}| \quad 3.6$$

$$V_{DS} > V_{GS} + V_{TH} \text{ OR } V_{SD} < V_{SG} - |V_{TH}| \quad 3.7$$

- Saturation Region – For an NMOS, at a particular gate and source voltage, there is a particular level of voltage for drain, beyond which, increasing drain voltage seems to have no effect on current. When a MOS operates in this region, it is said to be in saturation. The condition is given as:

$$V_{GS} \geq V_{TH} \quad 3.8$$

$$V_{DS} > V_{GS} - V_{TH} \quad 3.9$$

The drain current equation is given by,

$$I_D = \mu C_{ox} \frac{W}{L}\frac{(V_{GS} - V_{TH})^2}{2} \quad 3.10$$

Body Effect:

The body effect is the change in the threshold voltage by an amount approximately equal to the change in the source-bulk voltage, VSB, because the body influences the threshold voltage (when it is not tied to the source). It can be thought of as a second gate, and is sometimes referred to as the back gate, and accordingly the body effect is sometimes called the back-gate effect.

For an enhancement-mode nMOS MOSFET, the body effect upon threshold voltage is computed according to the Shichman–Hodges model, which is accurate for older process nodes, using the following equation:

$$V_{TN} = V_{T0} + \gamma\,(\sqrt{|V_{SB} + 2\emptyset_F|} - \sqrt{|2\emptyset_F|}) \quad 3.11$$

where V_{TN} is the threshold voltage when substrate bias is present,

V_{SB} is the source-to-body substrate bias,

$2Ø_F$ is the surface potential,

V_{TO} is threshold voltage for zero substrate bias,

$\gamma = \frac{t_{ox}}{\epsilon_{ox}} \sqrt{2q\epsilon_{si}N_A}$ is the body effect parameter,

t_{ox} is oxide thickness,

$€_{ox}$ is oxide permittivity,

$€_{si}$ is the permittivity of silicon,

N_A is a doping concentration,

q is elementary charge.

Input to PMOS:

P-n-P transistors can be built in standard CMOS technology for low-frequency applications, and exhibit lower 1/f noise than NMOS transistors. PMOS has lesser flicker noise than NMOS. Flicker noise is due to the random trapping and releasing of the electrons or holes in the interface. Flicker noise is observed only when a DC current flows. Since mobility of NMOS is greater than PMOS, flicker noise is larger in NMOS (for the same W/L), as electrons have more mobility than holes, so they will have more random trappings hence more flicker noise for NMOS devices.

Noise Efficiency Factor:

Since we are interested in minimizing noise within a strict power budget, we must consider the trade-off between power and noise. The noise efficiency factor (NEF) introduced in quantifies this trade-off.

$$\text{NEF} = V_{ni,rms} \sqrt{\frac{2I_{tot}}{\Pi.U_T.4KT.BW}} \qquad 3.12$$

Where, Vni,rms is the input-referred rms noise voltage,

Itot is the total amplifier supply current

BW is the amplifier band- width in hertz.

Substituting the expression for amplifier thermal noise integrated across the bandwidth BW and assuming, g_{m3}, $g_{m7} >> g_{m1}$

We find

$$\text{NEF} = \sqrt{\frac{4I_{tot}}{3U_T g_{m1}}} = \sqrt{\frac{16\ _{D1}}{3U_T g_{m1}}} \qquad 3.13$$

where, ID1 is the drain current through M1, which is 1/4 of the total amplifier supply current. From this expression, it is clear that if we wish to minimize the NEF, we must maximize the relative transconductance of the input devices M1 and M2. In weak inversion, gm/ID reaches its maximum value of k/UT, so we make (W/L)1 very large to approach sub threshold operation with micro amp current levels. Using a more accurate model for thermal noise valid in weak inversion yields

$$\text{NEF}= \sqrt{\frac{4I_{D1}}{kU_T g_{m1}}} \qquad 3.14$$

Assuming a typical value of k=0.7. This is the theoretical NEF limit for an amplifier with this circuit topology constructed from MOS transistors, assuming current mirror ratios of unity. In practice, the NEF will be limited by stability constraints on and gm3 and gm7 and by 1/f noise.

PSRR:

The power supply rejection ratio, or PSRR, has been steadily becoming more important due to the rising demand for power efficiency in electronic designs large and small. It's a measure of how much disturbance signals have been injected at the input levels, which, in turn, can impact the regulated output. And it shows how well an op-amp carries out the power delivery while rejecting various frequency elements at the input level. An op-amp's PSRR is the ability to reject noise or ripple occurring at the input side due to the change in input offset voltage with respect to the change in power supply voltage.

The PSRR is defined as the ratio of the change in supply voltage to the equivalent (differential) output voltage it produces, often expressed in decibels. An ideal op-amp would have infinite PSRR. The output voltage will depend on the feedback circuit, as is the case of regular input offset voltages. But testing is not confined to DC, often an operational amplifier will also have its PSRR given at various frequencies (in which case the ratio is one of RMS amplitudes of sine waves present at a power supply compared with the output, with gain taken into account).

The following formula assumes it is specified in terms of output:

$$PSRR[dB]=10log10\left(\frac{\Delta V^2_{\text{supply}} \cdot A_v^2}{\Delta V^2_{out}}\right) dB \qquad 3.15$$

Total Harmonic Distortion:

Harmonics or harmonic frequencies of a periodic voltage or current are frequency components in the signal that are at integer multiples of the frequency of the main signal. This is the basic outcome that Fourier analysis of a periodic signal shows.

Harmonic distortion is the distortion of the signal due to these harmonics. A voltage or current that is purely sinusoidal has no harmonic distortion because it is a signal consisting of a single frequency. A voltage or current that is periodic but not purely sinusoidal will have higher frequency components in it contributing to the harmonic distortion of the signal. In general, the less that a periodic signal looks like a sine wave, the stronger the harmonic components are and the more harmonic distortion it will have.

So, a purely sinusoidal signal has no distortion while a square wave, which is periodic but does not look sinusoidal at all, will have lots of harmonic distortion.

THD is defined as the ratio of the equivalent root mean square (RMS) voltage of all the harmonic frequencies (from the 2nd harmonic on) over the RMS voltage of the fundamental frequency (the fundamental frequency is the main frequency of the signal, i.e., the frequency that you would identify if examining the signal with an oscilloscope)

$$THD=\frac{\sqrt{\sum_{n=2}^{\infty} V_{n_{rms}}^2}}{V_{fund\_}rms} \qquad 3.16$$

- V_{n_rms} is the RMS voltage of the nth harmonic
- V_{fund_rms} is the RMS voltage of the fundamental frequency

In practice, THD must be measured to obtain the RMS value of the fundamental frequency and all of the harmonics. This measurement can be done in a couple of ways.

In the first method, filters can be used to split the signal into two parts: a signal with all of the harmonics filtered out leaving just the fundamental frequency, and a signal with the fundamental frequency filtered out leaving all of the harmonics. Then the RMS value of each of those two parts can be measured and the THD calculated:

The upside of this method is that it is easy to perform these measurements. The downside is that noise will also be included in the measurement so you actually get a measurement of THD plus noise (although in audio systems THD and noise is actually an important measurement too).

The second method for measuring THD is to measure the amplitude of the fundamental frequency and each harmonic and then use those measurements to calculate THD using

above equations. This measurement can easily be done using a spectrum analyzer or a THD analyzer which will execute the above Equation automatically. An alternative measurement technique is to capture voltage or current data and then perform a Fourier transform on the data collected.

3.2 Methodology

The overall schematic of proposed closed loop neural amplifier is shown in Fig.3.2.1. The topology is a capacitive feedback one, consisting of a gain stage where the cut-off frequency is controlled by the MOS bipolar pseudo-resistors Mb1–Mb2, input and feedback capacitances C_1 and C_2 respectively. The pseudo-resistors are formed by diode-connected MOS transistors. The mid-band gain of the Neural Amplifier is controlled by the ratio of C_1 and C_2, given by $(-C_1/C_2)$

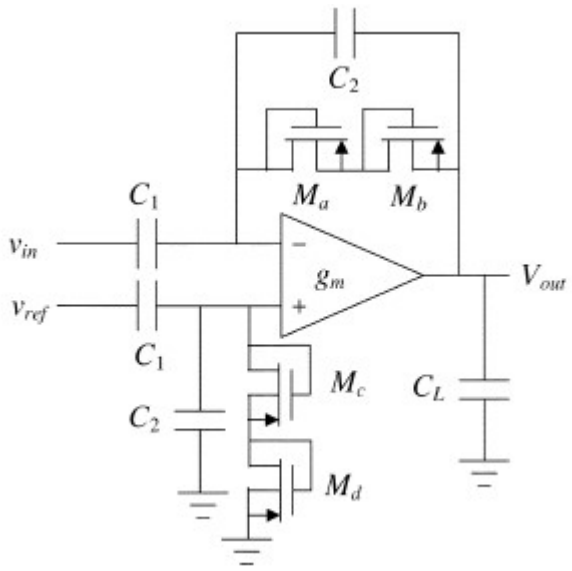

Fig. 3.2.1: Overall schematic of closed loop neural amplifier

C_1 is AC coupling capacitance for rejecting DC offsets and is generally kept large in order to compensate for the parasitic capacitances whereas C_2 is the feedback capacitance. The capacitors are realized using MIM capacitor as it has higher density, good linearity and lower parasitic/substrate capacitances. The C_2 and the MOS-bipolar pseudo-resistor generates a very low frequency pole because of a high impedance offered by the MOS-bipolar pseudo-resistor element. This sort of arrangement helps in removing the noise current and the shot noise offered by the gate leakage current of the input transistor before the pass band and it doesn't appear in the amplifier bandwidth. $C_L >> C_2$, the bandwidth is

approximately, $g_m/(A_mC_L)$ where g_m is the transconductance of the operational transconductance amplifier (OTA). Fig. 3.2.2 shows a schematic of the current-mirror OTA used in the bio-amplifier. The bias current and cascode bias voltages were generated by standard circuits, and the power consumption of these biasing circuits was not included in our power measurements since an arbitrary number of OTAs can share the generated voltages. Although the circuit topology is a standard design suitable for driving capacitive loads, the sizing of the transistors is critical for achieving low noise at low current levels. The bias current I_{bias} is set to 10 A, giving devices M1– M8 drain currents of 5 A.

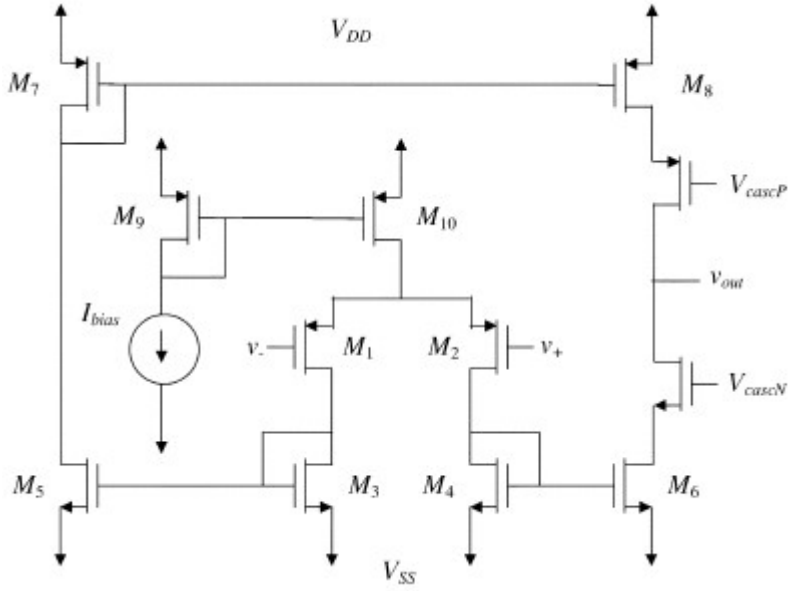

Fig.3.2.2: Schematic of OTA used in neural amplifier.

At this current level, each transistor may operate in weak, moderate, or strong inversion depending on its W/L ratio. For each device, we calculate the moderate inversion characteristic current I_s, given by

$$\text{Is} = \frac{2\mu C_{ox} U_T W}{kL} \qquad 3.17$$

where U_T is the thermal voltage kT/q, and k is the subthreshold gate coupling coefficient. Note that k has a typical value of 0.7.

The inversion coefficient (IC) for each transistor may then be calculated as the ratio of drain current to the moderate inversion characteristic current, as follows:

$$IC = I_D/I_S \qquad 3.18$$

The input devices and are drawn with identical sizes, and we denote their transconductance as and their width-to-length ratio as. Similarly, transistors – are the same size and have

transconductance. The pMOS current mirror transistors and have size and transconductance.

Analysis of this circuit reveals the input-referred thermal noise power to be

$$V^2_{ni,Thermal} = \left[\frac{16kT}{3g_m}\left(1+2\frac{g_{m_3}}{g_{m_1}}+\frac{g_{m_7}}{g_{m_1}}\right)\right] \quad 3.19$$

If we size our devices such that g_{m7}, g_{m3} << g_{m1}, we can minimize the noise contributions of devices M3–M8. This can be accomplished by making $(W/L)_3$, $(W/L)_7$ << $(W/L)_1$, thus, pushing devices M3–M8 into strong inversion where their relative transconductance (g_m/I_d) decreases as $1/\sqrt{I_d}$. By operating M1 and M2 in the subthreshold regime, we achieve a high (g_m/I_d) ratio so that g_{m1} is much greater than g_{m3} and g_{m7}. We are operating near the maximum achievable g_m/I_d ratio of kT/q (approximately $27V^{-1}$), which is reached in deep weak inversion.

If the total capacitance seen by the gate of M_3(or M_4) is denoted as C_3, then the OTA has two poles at $w_p=g_{m3}/C_3$. Similarly, there is a pole at g_{m7}/C_7 caused by the pMOS mirror. To ensure stability, these pole frequencies must be several times greater than the dominant pole, g_{m1}/C_L. This criterion becomes easier to satisfy as C_L is made larger, so it becomes necessary to consider area limitations and bandwidth requirements. In our design, we decreased $(W/L)_3$ and $(W/L)_7$ as much as possible, trading off phase margin for lower input-referred noise. Transistors M3–M8 are narrow devices that require relatively large gate overdrive voltages, so output signal swing considerations or finite power-supply voltages may also limit the designer's ability to decrease g_m.

Flicker noise, (1/f) or noise, is a major concern for a low-noise low-frequency circuit. We minimize the effects of flicker noise by using pMOS transistors as input devices and by using devices with large gate areas. Flicker noise in pMOS transistors is typically one to two orders of magnitude lower than flicker noise in nMOS transistors as long as $|V_{GS}|$ does not greatly exceed the threshold voltage, and flicker noise is inversely proportional to gate area. All transistors should be made as large as possible to minimize 1/f noise. As M_1 and M_2 are made larger, the OTA input capacitance C_{in} increases. The input-referred noise of the bio-amplifier can be related to the OTA input-referred noise by

$$V_{ni}, amp^2 = \left(\frac{C1+C2+Cin}{Cin}\right)^2 V_{ni}^2 \quad 3.20$$

where C1 and C2 are the feedback network capacitors shown in Fig. 3.2.1. Since Cin contributes to a capacitive divider that attenuates the input signal, any increase in Cin

increases the input-referred noise of the overall circuit. An optimum gate area for M1 and M2 can be found to minimize 1/f noise. Lateral p-n-p transistors can be built in standard CMOS technology for low-frequency applications, and exhibit lower 1/f noise than MOS transistors. We did not use p-n-p devices for the input transistors M1 and M2 because the base current would have to flow through the MOS-bipolar devices. This dc current would bias the pseudo-resistors toward an operating point with lower incremental resistance and raise the low-frequency cutoff. The inherently high g_m/I_c ratio of bipolar transistors makes them unsuitable for devices M3–M8 in our OTA design.

As we want the MOSFET to act as amplifier which is possible when the MOZFET is operating in saturation region.

Therefore, considering the Saturation region condition:

$$VGS \geq Vth \quad (3.21)$$

$$VDS > VGS - Vth \quad (3.22)$$

$$I_D = \frac{1}{2}\mu Cox\frac{W}{L}(VGS - Vth)^2 \quad (3.23)$$

Devices	**(W/L)**	**I_D (µA)**
M_1, M_2	100/9	5
M_3, M_4, M_5, M_6	20/9	5
M_7, M_8	20/9	5
M_9, M_{10}	200/9	10
M_{cascN}	59/450	5
M_{cascP}	20/9	5

Table 1: W/L ratio of the MOSFET.

Designed Circuit:

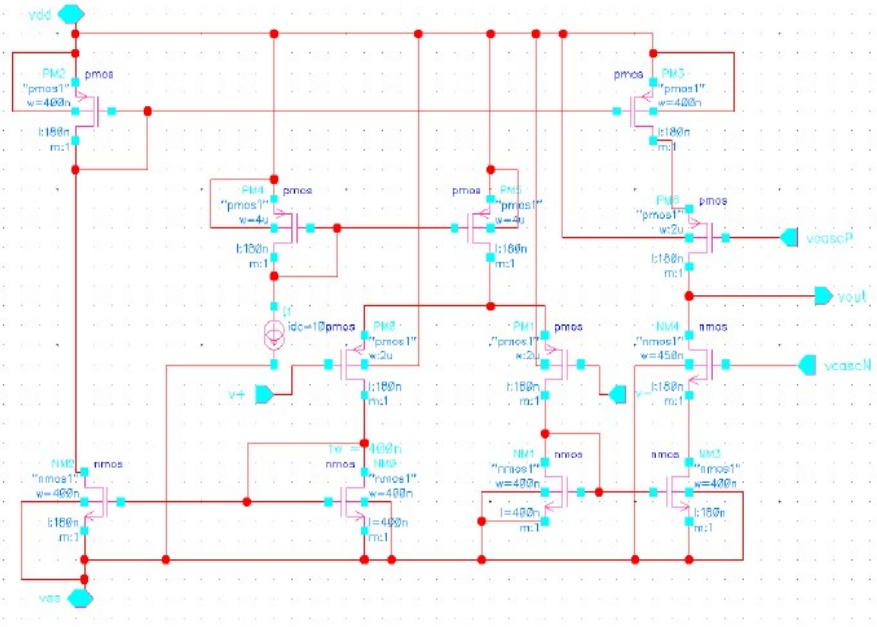

Fig. 3.2.3: Schematic Design of OTA

Test Circuit:

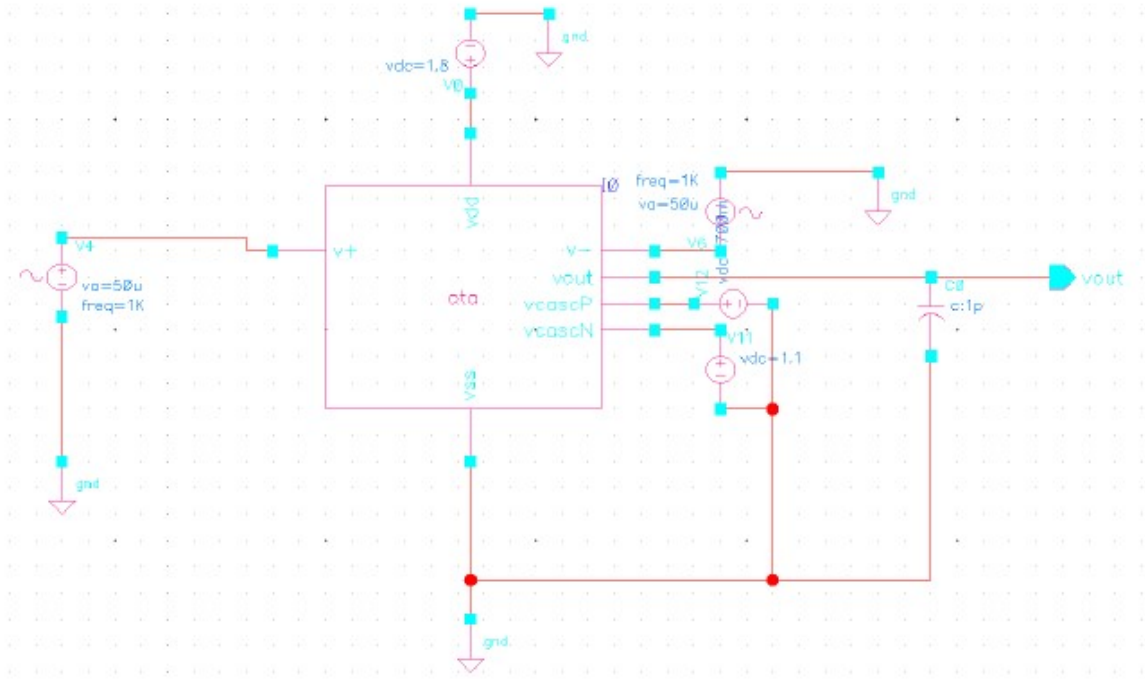

Fig. 3.2.4: Layout design of OTA

Chapter 4
SOFTWARE

The design of Neural Amplifier for Brain Machine Interface is done using 180nm CMOS technology in the software CADENCE Design System.

4.1 Introduction

This section is intended to introduce microelectronic designers to the Cadence Design Environment, and to describe all the steps necessary for running the Cadence tools during our project.

Cadence is an Electronic Design Automation (EDA) environment that allows integrating in a single framework different applications and tools (both proprietary and from other vendors), allowing to support all the stages of IC design and verification from a single environment. These tools are completely general, supporting different fabrication technologies. When a particular technology is selected, a set of configuration and technology-related files are employed for customizing the Cadence environment. This set of files is commonly referred as a design kit. The open architecture also allows for integration of tools from other vendors or of own design. The integration of all this tool is done by a program called Design Framework II (DFW).

The DFW-application is the cornerstone in the Cadence environment. It provides a common user interface and a common data base to the tools used. This makes it possible to switch between different applications without having to convert the data base.

It is not the objective of the section to provide an in-depth coverage of all the applications and tools available in Cadence. Instead, a detailed introduction to those required for an analog designer, from the conception of the circuit to its physical implementation, is provided. References to other manuals and greater understanding of Cadence, the extensive on line manual set is recommended. These are accessed from any of the tools by pressing the help button.

4.2 Cadence User Interface

In Cadence the user interface is graphic and based on windows, forms, and menus.
The main windows of DFW are:

- Command Interpreter Window (CIW) is controlling the environment. Other tools can be started from here and it also serves a log window for many applications
- Library Manager gives a view of the design libraries and the different constructions that exists therein.
- Design Window (DW) shows the current design. It is possible to have several DW opened at the same time with different, or the same, tools.
- Text Window (TW) show text. It can be a log or report that was asked for, or an editor.

The menus in Cadence are mostly pull-downs, i.e. the menu will appear when the title is clicked with the left button on the mouse. There are also pop-up menus that appear in the background of the design window on a middle button press. The forms are used for entering some specific information that is needed by the function called, the size of a transistor for instance.

4.3 Design Flow and Tool

The design tools have a common structure of the designs. It is hierarchical and consists of libraries, views, and instances.

4.3.1 Libraries and Views

All design data in Cadence are organized in libraries. There are Reference Libraries which contains basic building blocks usable in the construction and Design Libraries which embodies the current design. Every library consists of cells and their different views, as in Fig 4.1. A cell is a database object which forms a building block, an inverter for instance. A view represents some level of abstraction of the cell. It can be a schematic drawing, layout, or maybe some functional description.

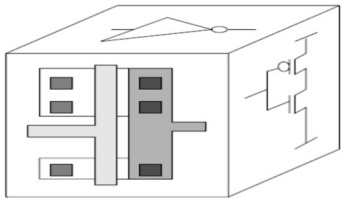

Fig. 4.1. An inverter cell with three views: layout, schematic, and symbol.

4.3.2 Instances and Hierarchy

The main reasons for using hierarchical designs is to save design time and minimize the size of the data base. Say that a design would need 500 gates of the same type. Then instead of building it 500 times, it is designed once and then used were it is needed. In this way one cell can be used (not copied) several times and each such use are called an instance of the cell. In order to be instantiated every cell needs a symbol view which acts as a handle to the cell it represents. Only the symbol is shown when a cell is instantiated.
Thus, by creating more complex structures by instantiating simple instances a hierarchical design is formed. It is possible to move up and down and work on a selected level in the hierarchy. When a design is opened, the highest level is the default one.

4.3.3 The Technology File

Since there are different semiconductor processes (with different set of rules and properties), Cadence has to know the specifications for the one that is to be used. This information is stored in a set of files called Technology Files which exists on different locations on the system.
When a library is created it is therefore connected to a specific technology.
The technology files contain information about:

• Layer definitions: Conductors, contacts, transistors ...

• Design rules: minimum size, distance to objects ...

• Display: Colours and patterns to use on the screen.

• Electrical properties: resistance, capacitance ...

The technology files are usually supplied by the silicon vendor, that is to fabricate the design, along with some libraries of standard cells and IO pads that can be used by the designer. Such a collection is called a Design Kit.

4.3.4 The SKILL Programming Language

When a command is performed, from a form or a menu, the system is executing functions written in the SKILL language. SKILL is developed by Cadence and is based on Lisp. The

Cadence tools are using SKILL for internal communication and for the tool-design communication.

SKILL is also accessible for the designers. Commands can be written in the CIW window or placed in command files for execution. it can be used for simple tasks like executing a command or building more complex functions to perform various tasks.

4.3.5 The Design Flow

The abbreviated flow in Fig 4.2 shows some of the steps in designing integrated circuits in the Cadence environment.

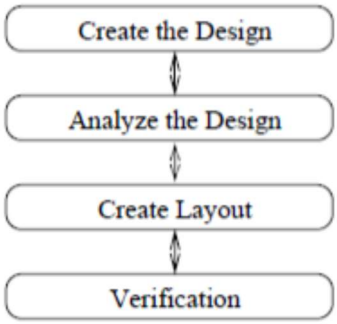

Fig. 4.2. The design flow

The step Create the Design consists of drawing schematic views of all cells and blocks. The schematic view contains transistor symbols, and maybe other components such as resistors and capacitances, and wires connecting them. From the schematic view the symbol view is created (almost automatically) so that the cell can be used on a higher level in the hierarchy.

The step Analyze the design includes functional verification (simulation) of the design on a schematic level.

The third step, Create Layout, is done in a Layout Editor. Here the final semiconductor layers are represented by different colors. All the cells and blocks used have the size they will have on the final chip.

The last step is Verification of the design. The layout is examined for violations against the geometric or electrical rules, and to verify the function of the physical implementation.

4.4 Schematic and Symbol tools

To create the schematic the tool Virtuoso Schematic Composer is used. This editor is an interactive system for building schematics by instantiating some basic components (transistors, capacitances, etc.) and to connect them to each other. The values (properties) of the components can be edited to suit the specifications. Text and comments can also be included.

The editor will also create symbols of the cells so that they can be used in other parts of the construction.

4.5 Simulation

The simulation tool is started directly from the schematic editor and all the necessary netlists describing the design will be created. A simulation is usually performed in a test bench, which is also a schematic, with the actual design included as an instance. The test bench also includes signal sources and power supply. By using parameters for the properties of the components used it is possible to quickly analyze the design for a wide range of variables.

The simulator is run from within Affirma Analog Circuit Design Environment which is a tool that handles the interface between the user and the simulator. The current version of Cadence used at the department (4.45) uses the Affirma Spectra Circuit Simulator. The simulator offers a wide range of analyses (DC, frequency sweep, transient, noise, etc.) and the results can be presented graphically and be saved.

The results (voltage levels, currents, noise, etc.) can be fed into a calculator which can present various parameters of the analyzed circuit - delay time, rise time, slew rate, phase margin, and many other interesting properties. It is also possible to set up algebraic expressions of in or output signal which can be plotted as a function of some other variable.

4.6 Layout Tool

The Virtuoso Layout Editor is used for drawing the layout. A layout consists of geometrical figures in different colors. From the size and color of this figures it is later possible to generate the final mask layers which is used in the fabrication of the design. It is possible to include other cells by instantiating their layout views.

To verify that the layout fulfills all electrical and geometric rules a Design Rule Check (DRC) program is used. This manual will describe Assura Diva verification which can be called upon directly from the layout editor. This tool will mark any error in the design and can also extract (i.e. convert to a netlist) the layout so it can be simulated.

4.7 Place and Route

The final stage of the construction of a large design is called place and route. This is the process when all the different components of the chip is placed on its locations and connected to each other. Since a design can easily consist of thousands of connection points it would be tedious and time consuming to do the connections manually. The designer might also want to try various alternatives in placing the components, output buffers, memory structures, amplifiers, etc.

The place and route tool that will be described later in this manual is named Envisia Silicon Ensemble. It is a very potent program that that can place and route a very large design while respecting some design constraints (restrictions on delay and size) at the same time.

Usually Silicon Ensemble is used for Standard Cell designs - this is when all the cells are of the same height so they can be placed in contact (abutted) with each other - but it can handle other structures.

Since not all designs that is to be routed are created in Cadence this manual will describe how to run Silicon Ensemble as a standalone tool. In some other design tools the function of a digital design is described in a functional language which is the compiled (synthesized) into a netlist that can be fed into Silicon Ensemble.

Chapter 5

RESULTS

In order to validate the performance of the proposed Neural Amplifiers, simulations have been carried out in Cadence Virtuoso using technology parameters of SCL 180 nm foundry and with the values of design parameters as shown in Table 1. The values of design parameters VDD, Ibias etc. have been chosen based on the requirement of achieving minimum specifications for a neural recording system. The capacitors are realized using MIM capacitor as it has higher density, good linearity and lower parasitic/ substrate capacitances. Another alternative was the use of MOS capacitors, which can be used for area advantage during fabrication. However, for same C_1 and C_2, a lower value of voltage gain was achieved using MOS capacitors. This could be because the capacitance imitated by the MOSCAP is not large due to some biasing problem and hence large attenuation of the signal is there from the source to the gate of the input pair. Addition of bias voltage was also done which resulted in improved Gain, but it was still poor as compared to that achieved by using MIM capacitor. The rnlpoly2T has been used to realize the current scaling resistors for better accuracy. The aspect ratio for all the MOSFETS have been chosen so as to increase Gain, CMRR etc.

We have obtained the graph of Transient response, DC response and Noise.

Transient Response:

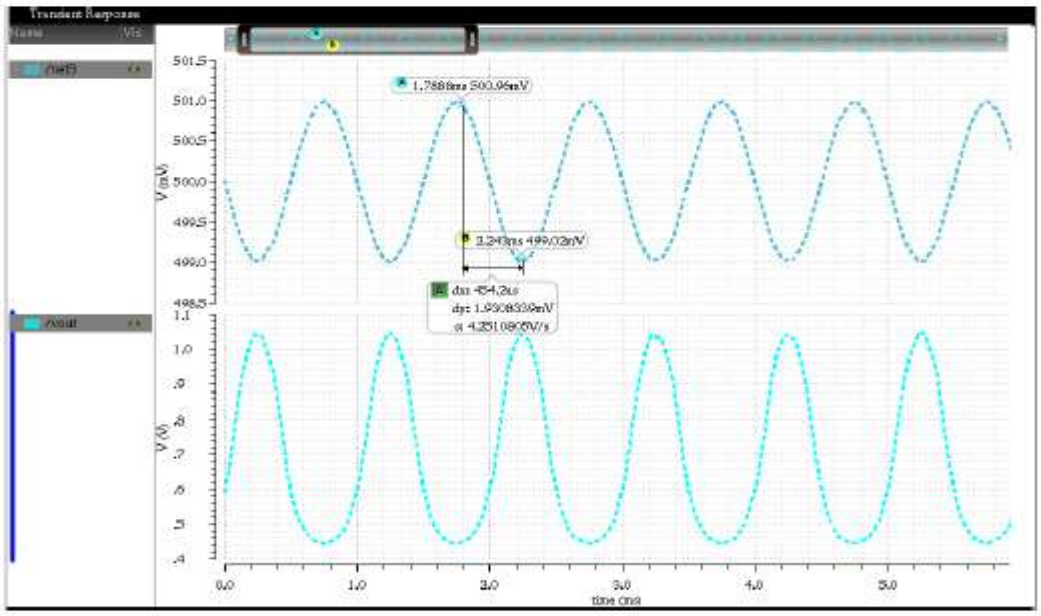

Fig. 5.1: Transient response measuring input peak of amplifier

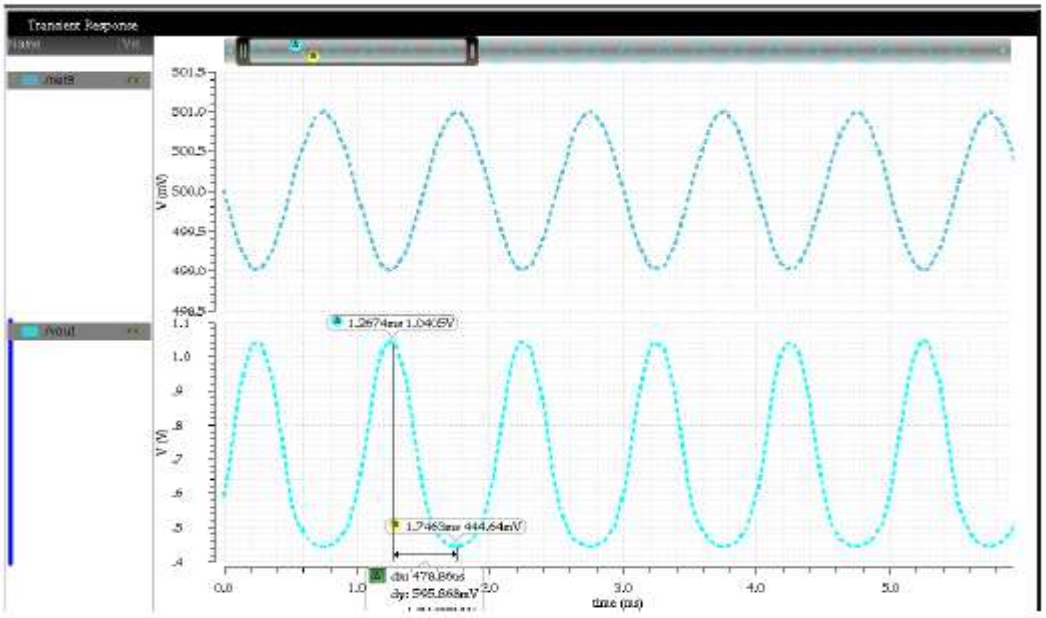

Fig. 5.2: Transient Response measuring output peak of amplifier

Transient response helps to determine the false condition in the circuit i.e. short circuit, overload, rise and fall time, slew rate and to determine the quality factor

The gain is estimated from Fig. 5.1. and Fig. 5.2. as,

$$\text{Gain } (A_v) = \frac{Vout}{Vin} = \frac{595.868mV}{1.930mV} = 308.73$$

$$\text{Gain(dB)} = 10\log_{10}(A_v) = 10\log_{10}(308.73) = 24.89\text{dB}$$

Fig. 5.1 and 5.2 shows the measured amplifier transfer function from 0.004 Hz to 50 kHz. The mid-band gain is 24.89 dB.

DC Analysis:

DC analysis of a network is important to know the required power supply and its limits, the current consumption and to be ensure that all devices in the circuit are working in the safe region without exceeding their normal ratings.

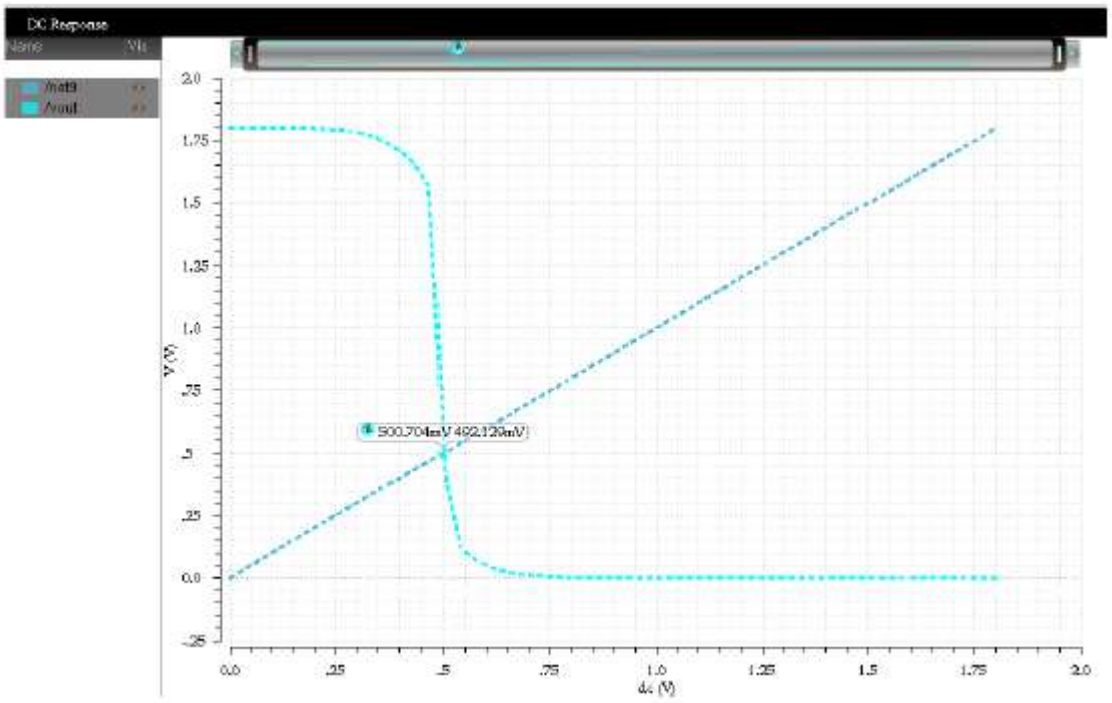

Fig. 5.3: DC response of Amplifier

The operating point of the circuit is 500.704mV.

Noise:

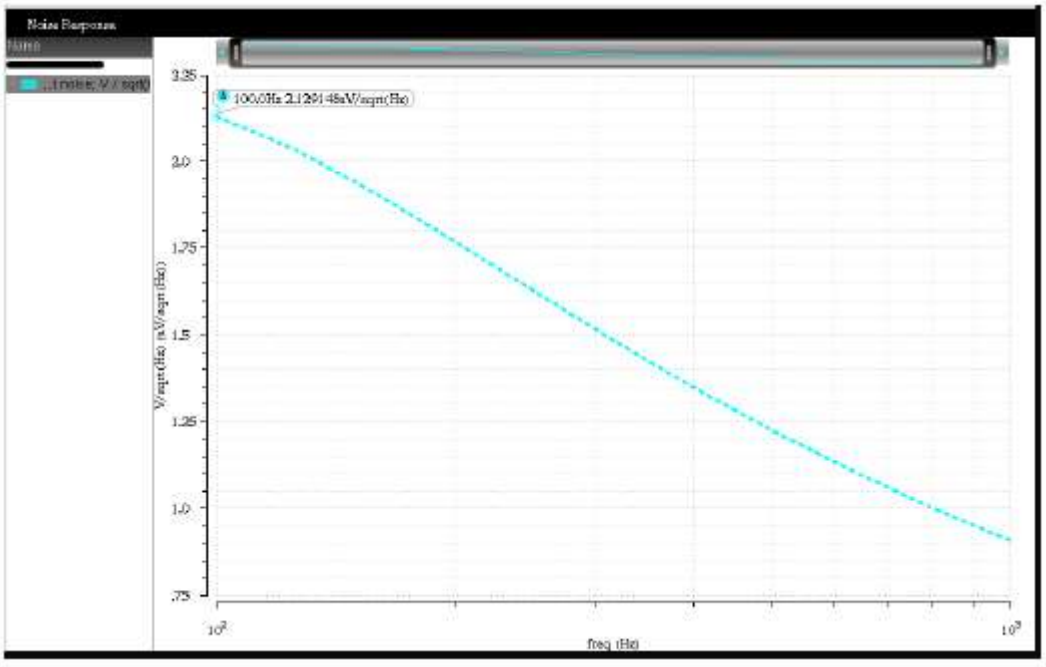

Fig. 5.4: Noise of amplifier

Using a more accurate model for thermal noise valid in weak inversion yields

$$NEF=\sqrt{\frac{4I_{D1}}{kU_T g_{m1}}}$$

Assuming a typical value of k=0.7. This is the theoretical NEF limit for an amplifier with this circuit topology constructed from MOS transistors, assuming current mirror ratios of unity.

$$NEF = \sqrt{\frac{4*27*4.74*10^{-6}}{0.7^2*7.13*10^{-6}}} = 3.832$$

$$NEF = 3.832$$

Power Consumption:

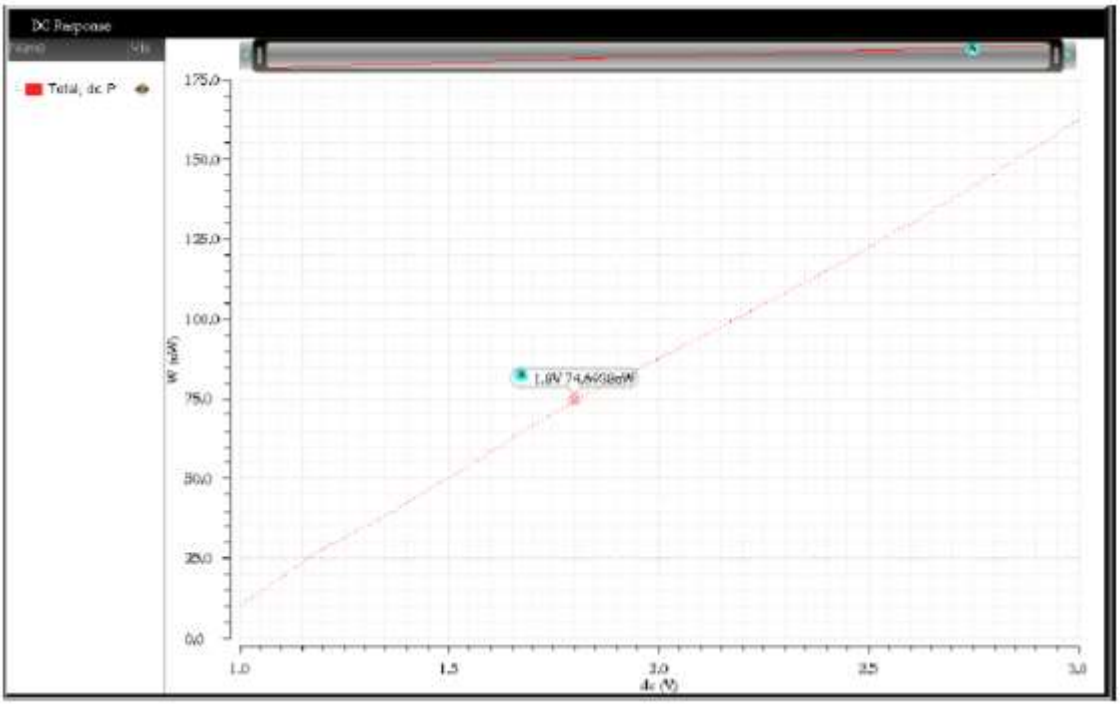

Fig.5.5: Power Consumed by circuit

The Power consumed by the designed circuit is 74.693µW for the supply voltage of 1.8V.

Chapter 6

APPLICATIONS AND ADVANTAGES

The applications of neural amplifier are as follows:

6.1 Neural amplifier for studies of central nervous system (CNS)

CNS-based IC neural amplifiers have widespread applications ranging from basic science research in animal models to translational research with human subjects. Most CNS-based neural amplifier systems have signal band-widths that are constrained to either acquire action potentials (AP), also called spikes, typically in the range of 200 Hz to 10 kHz, or to local field potential (LFPs) with a typical bandwidth of 0.1–200 Hz. By constraining the amplifiers to record only within the bandwidths of interest, the noise contribution from the amplifier is significantly reduced and therefore improves the recording quality. CNS amplifiers have also been developed that can acquire both types of signals, separately filtering, amplifying and outputting each signal type.

6.2 Neural amplifiers for Paralysis Prosthetics

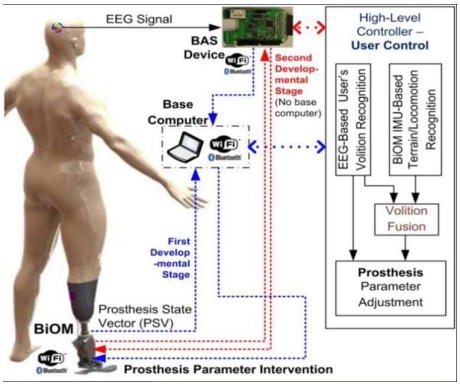

Fig.6.2: Schematic diagram of user's direct control of prosthesis using BCI.

Neural amplifier provides the ability to move an object using brainpower. Brain−machine interface (BCI) technology is employed as neural prostheses for communication and control. The technology uses brain signals from electrodes or sensors placed either outside or inside the scalp. BCI techniques are expected to improve the quality of life of paralyzed individuals, being of particular benefit to those lacking voluntary muscle control.

6.3 Neural Amplifier for Epilepsy

Neural Amplifier systems are used for epilepsy resection procedures. Epilepsy resection procedures present frequent opportunities for researchers to perform experimental studies on human subjects. Therefore, many Blackrock clinical customers are affiliated with epilepsy centers and doctors. Monitoring epileptic focus resection provides researchers with access to human subjects with a grid of electrodes positioned on their brain. This permits research studies with no added risk to the patient.

6.4 Neural amplifiers for therapeutic neuromodulation

The information gleaned from the acquisition of neural electrical activity can be used to augment therapeutic stimulation of the nervous system. Neural stimulation can be used to treat neurological diseases of the brain, restore the functions of the limbs, interface and restore functions provided by peripheral or visceral nerves, restore bladder function or relieve chronic pain. For example, deep brain stimulation (DBS) is particularly successful in treating movement disorders, such as Parkinson's Disease, dystonia and essential tremor.

6.5 Neural amplifiers for the peripheral nervous system (PNS)

Neural amplifiers are also used to acquire signals from the peripheral nervous system. Signals acquired by nerve electrodes, either extrafascicularly or intrafascicularly, generally have extremely small amplitudes. A promising use of PNS neural recording amplifiers is in neuromodulation and neuroprosthesis systems. Recently, a peripheral nerve-based neuromodulation system for bladder control was demonstrated in rats. Such a device, in human patients, could restore bladder control lost due to spinal cord injury.

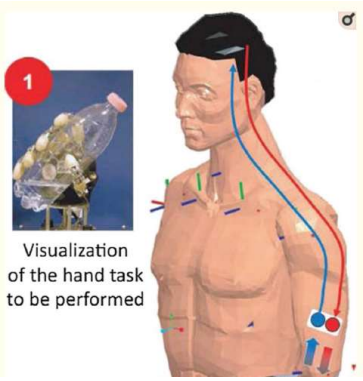

Fig.6.5: A peripheral nerve prosthesis applied to an amputee

Chapter 7

CONCLUSIONS AND SCOPE FOR FUTURE WORK

A Neural Amplifier IC with high gain and bandwidth has been designed considering noise-power trade-off. For improving the noise performance, current scaling is done by using source degenerated current sources at the sink transistors. The amplifier rejects dc offsets commonly encountered in microelectrode recording applications, but passes low-frequency signals in the millihertz range while using no off-chip components. By taking advantage of the high g_m/I_D ratio of devices operating in subthreshold, we were able to achieve the best power–noise tradeoff reported among bio-signal amplifiers.
The closed loop neural amplifier reports a very high gain and bandwidth and a comparably low noise as compared to the state of art. The design of both these amplifiers together in an IC ensures that the overall neural IC can have a low noise and low power together which is very difficult to achieve in case of neural recording systems.

Comparative analysis with other state of art design indicated that the proposed closed loop amplifier performed efficiently in terms of a higher mid- band gain, higher bandwidth and a reasonable NEF as compared to most other state of art designs, the only trade- off being a marginal increase in power dissipation with mid band gain of 24.89dB, the operating point of the circuit is 500.7mV , NEF of 3.832 and the power consumed of 74.693μW.

Our Future work can be extended to certain implementation such as
The band pass filter can be added along with the amplifier, so as to tune the bandwidth based on the requirement for recording local field as well as action potentials. The filters bandwidth is controlled by switches working on digital logic. Hence, the amplifier IC would then consist of some digital circuitry, which consume higher power, thereby increasing overall system power consumption. However, our proposed neural amplifier is designed for recording action potentials only.

For recording local field potentials, we are working on an altogether different amplifier. The restriction imposed is that the overall power consumption should be less than that consumed by a band pass filter.

A complete multichannel recording system will also require an analog multiplexer (MUX) and analog-to-digital converter (ADC) with milliwatt power dissipation. For systems with large numbers of channels, the hardware required for serialization and digitizing of neural signal data may become the dominant source of power consumption. Low-power MUX and ADC design will be essential for fully implanted neural recording systems.
The low-frequency ac coupling provided by the MOS-bipolar element may also have applications in the baseband circuitry of direct-conversion RF receivers. The direct-conversion architecture is attractive for low-power fully integrated receivers, but device mismatch and substrate coupling lead to large dc offsets that may be much larger than the received signal. The amplifier presented in this article achieves ultralow-frequency ac response while completely rejecting large dc offsets, and may be of use in integrated direct conversion systems.

The Neural Amplifier IC can be used in recording neural signals simply by connecting it with MEA and other signal conditioning circuitry, thereby interfacing the human brain. The overall system can be further used for many health monitoring applications.

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APPENDIX A