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BELAGAVI-590018, KARNATAKA

PROJECT REPORT

ON

"*Highly Linear CMOS Active Inductor for RFIC Applications*"

Submitted by

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CERTIFICATE

This is to certify that the dissertation work **"Highy linear CMOS Active Inductor for RFIC Applications"** carried out by **Sanjay N, T Prashanth, Zishani Mishra**, holding USN: **1CR16EC151, 1CR16EC177, 1CR16EC200,** bonafide students of **CMRIT** in partial fulfillment for the award of **Bachelor of Engineering** in **Electronics and Communication Engineering** of the **Visvesvaraya Technological University, Belagavi,** during the academic year **2019-20**. It is certified that all corrections/suggestions indicated for internal assessment have been incorporated in the report deposited in the departmental library. The project report has been approved as it satisfies the academic requirements in respect of Project work prescribed for the said degree.

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ABSTRACT

This project proposes a distortion reduction technique for active inductors. A bias current of a MOSFET, which acts as transconductor in an active inductor, is controlled to reduce a distortion of a active inductor. When an input voltage increases, the bias current is decreased by a control circuit. As a result of this control, transconductance of the MOSFET remains constant. The design is implemented using 180nm technology and it is based on Gyrator-C approach which consists of two transconductances. The input is given to the Nmos of the grounded cascode configuration, with a supply voltage of 1.8V. The simulation results obtained with the design are, Inductance ranging from 23.14nH to 244nH for frequency 666MHz to 2.5GHz range respectively, Noise of 921.8pV/sqrt(Hz) at 2GHz. and maximum Q factor of 337. The power consumption is 995.5uW for the supply voltage of 1.8V. An active inductor using this technique is free from distortion caused by a transconductance variation of a MOSFET. The proposed technique is applied to conventional active inductors and a more linear active inductors is derived. Computer simulations show that distortion of the proposed active inductor is very low.

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Chapter1

INTRODUCTION

An inductor is one of the basic components of electronic circuits. It is often used for filters, oscillators, low noise amplifiers, matching circuits and so on. However, using an inductor in an integrated circuit brings a significant drawback. An inductor is usually implemented as a spiral inductor in integrated circuits; however, it occupies very large chip area. Chip area required for passive elements have not decreased even in the latest CMOS process whose minimum gate width is deep sub-micron.

Recently, with scaling in CMOS technology, autonomous communicating objects operating in wide frequency band have become very popular. Many researches and studies have been performed to improve the performance of these systems. While the most specification requirements of these above systems are wide tuning range, high gain and low noise, active devices especially active inductors, have become one of the most important alternatives solution for multi-band Integrated Circuits (ICs) designing.

Furthermore, Q of an on-chip inductor is relatively low. Obtaining an on-chip inductor with high Q is very difficult. A typical value of an on-chip inductor's Q is about 10. There are a lot of literatures which deal with this problem. Using active inductors is one of the most successful approaches to overcome these problems. An active inductor is a circuit block whose input impedance is the same as that of a passive inductor. Thanks to the development of CMOS process, an active inductor can be used for RF applications nowadays.

An active inductor occupies very small chip area compared with a spiral inductor because it consists of only MOSFETs and its parasitic capacitors. Furthermore, Q of an active inductor is usually higher than that of a spiral inductor. On the other hands, disadvantages of an active inductor are non- linearity, power consumption and noise characteristics. The relation between an input voltage and input current of most active inductors is nonlinear because of non-linearity of MOSFETs. Input-signal-amplitude is limited by the linearity of active inductor. An implementation of the active inductor is a methodology called the Gyrator-C configuration. This Gyrator-C configuration exhibits much higher values of inductance and quality factor in quantitative comparison to traditional spiral inductors.

AIs are used for many applications such as variable phase shifter, wideband filter, wideband LC oscillator and wideband low noise amplifier. Various analog architectures are suggested to emulate the electrical characteristics of inductor in literature. However, the most famous topology which is used in designing AIs especially for high frequency applications is Gyrator-C (GC). Its popularity derives from the fact that gyrators transconductance can be adjusted with applied bias; thereby allowing for AIs whose value can be tuned electrically. The cascoding and RC feedback structures are used in the new design of AI. As it discussed before, input transistor is very important in term of AI performance. Cascading input transistor gives the ability to adjust first gyrators transcoductance and input parasitic capacitance independently.

Also, the inductance value can be adjusted by the input transistors transconductance. Therefore, the employed techniques not only guarantee the stability of the structure but also give the possibility to adjust specifications of AI separately. The RC feedback is utilized to cancel the parasitic resistive which it results QF enhancement. The proposed structure is robust in term of performance over variation in process, voltage and temperature.

Chapter 2

BACKGROUND THEORY

2.1 About Active Inductor

Inductors are one of the basic components used in electronics where current and voltage change with time due to the ability of inductors to delay and reshape alternating currents. The effect of an inductor in an electric circuit is to oppose changes in current through the circuit by developing a voltage across the circuit proportional to the rate of change of the current. The LC tank circuit is shown in the Figure: 2.1 The relationship between the time-varying voltage v (t) across an inductor with inductance L and the time-varying current i(t) passing through it is described by the differential equation;

$$v(t) = L * di/dt \tag{2.1}$$

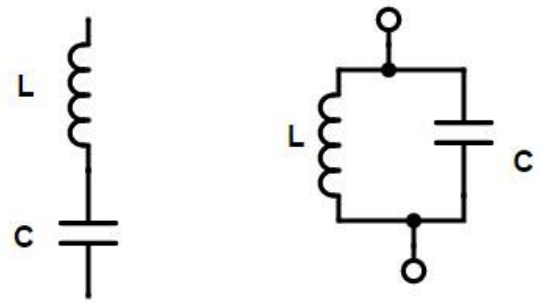


Figure: 2.1. LC Tank circuit

There are many design variations for constructing inductors. For example, an inductor may be constructed as a coil of conducting material (e.g., copper wire) wrapped around a core either of air or of ferromagnetic or ferromagnetic material as shown in the Figure 2.2.

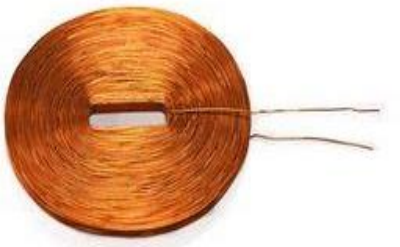


Figure: 2.2. Copper wire

Spiral inductors are used extensively in microwave circuit resonant elements and as a choke in power supplies. When used as a choke, a low Q is generally desirable obtain a broadband characteristic. To obtain a high self-resonance, the conductor width is reduced and capacitance between turns is minimized by conductor geometry. Values for chokes are usually not too critical as long as self-resonant frequency is high. Tuned circuits frequently require adjustment of the inductance value.

As another example, when incorporated as a component of an integrated circuit (IC) where it is desirable that the size of the inductor is relatively small, a gyrator-based circuit, which uses a capacitor and other active components to transpose the capacitive impedance to an inductive one, behaves similarly as an inductor. Such circuits are called "active inductors" as they use active elements to create inductive impedance in a wide frequency range.

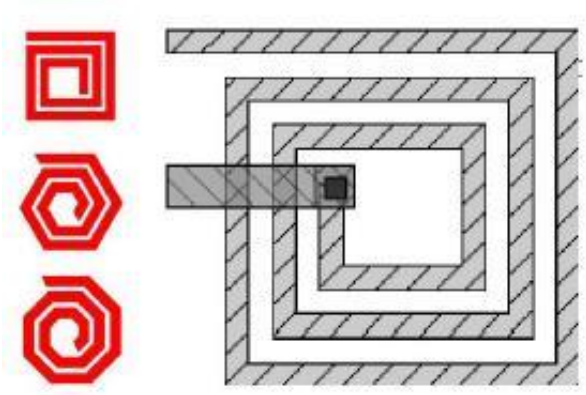


Figure: 2.3. Spiral Inductor

Inductors are prominent element in RF circuit design. "RF" refers to the use of electromagnetic radiation for transferring information between two circuits that have no direct electrical connection. Time-varying voltages and currents generate electromagnetic energy that propagates in the form of waves. The spiral inductor is shown in the Figure: 2.3 which we use for the active inductor. An inductor, in general, is a passive electrical component that can store energy in a magnetic field created by the electric current passing through it. An inductor's ability to store magnetic energy is measured by its inductance (symbol "L"), in units of "henries" (symbol "H", named after American scientist Joseph Henry).

Inductance results from the magnetic field forming around a current-carrying conductor, which tends to resist changes in the current. Electric current through the conductor creates a magnetic flux proportional to the current. A change in this current creates a corresponding change in magnetic flux which, in turn, by Faraday's Law generates an electromotive force (EMF) that opposes this change in current. Inductance is measure of the amount of electromotive force generated per unit change in current. By definition, if the rate of change of current in a circuit is one ampere per second and the resulting electromotive force is one volt, then the inductance of the circuit is one henry.

An active inductor includes an MOSFET having a gate, a drain serving as an output terminal and a grounded source, the MOSFET having a transconductance gm1, and a capacitor having opposite ends, one of which is grounded and the other of which is connected to the gate of the MOSFET and to a voltage-controlled constant current source having a transconductance gm, the capacitor having a capacitance C, the active inductor being operative with a small-signal output impedance between the output terminal and the ground expressed as :

$$Zo=j\omega\{C/(gm1\cdot gm)\} \quad \text{(wherein } \omega \text{ is an angular frequency)} \tag{2.2}$$

And inductance expressed as:

$$Leq=\{C/(gm1\cdot gm)\}. \tag{2.3}$$

2.2 Characterization of Active Inductor

In this section, we investigate the most important figure-of-merits that provide quantitative measures of the performance of active inductors. These figure-of-merits include frequency range, inductance tunability, quality factor, noise, linearity, stability, supply voltage sensitivity, parameter sensitivity, signal sensitivity, and power consumption.

2.2.1 Frequency Range

It was shown in the preceding section that a lossless gyrator-C active inductor exhibits an inductive characteristic across the entire frequency spectrum. A lossy gyratorC active

inductor, however, only exhibits an inductive characteristic over a specific frequency range. This frequency range can be obtained by examining the impedance of the RLC equivalent circuit of the lossy active inductor. The Bod'e plots of *Z* are sketched in Figure: 2.4. It is evident that the gyrator-C network is resistive when$\omega < \omega z$, inductive when $\omega z < \omega < \omega o$, and capacitive when$\omega > \omega o$.

The frequency range in which the gyrator-C network is inductive is lower-bounded by ωz and upper-bounded by ωo. Also observed is that *Rp* has no effect on the frequency range of the active inductor. *Rs*, however, affects the lower bound of the frequency range over which the gyrator-C network is inductive. The upper bound of the frequency range is set by the self resonant frequency of the active inductor, which is set by the cut-off frequency of the transconductors constituting the active inductor. For a given inductance *L*, to maximize the frequency range, both *Rs* and *Cp* should be minimized.

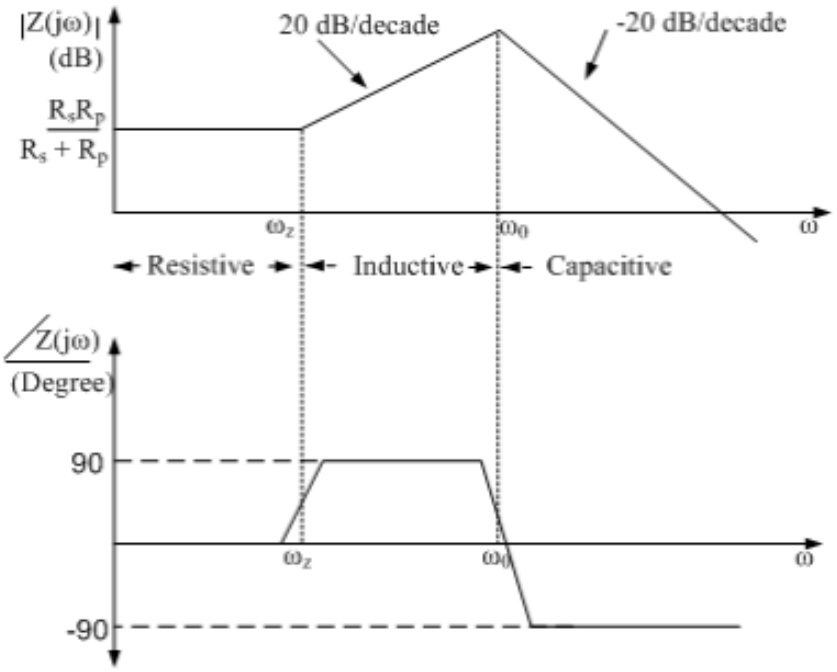


Figure: 2.4 Bod´e plots of the impedance of lossy gyrator-C active inductors.

2.2.2 Inductance Tunability

Many applications, such as filters, voltage or current controlled oscillators, and phase-locked loops, require the inductance of active inductors be tunable with a large inductance

tuning range. The inductance of gyrator-C active inductors can be tuned by either changing the load capacitance or varying the transconductances of the transconductors constituting the active inductors. Capacitance tuning in standard CMOS technologies is usually done by using varactors. Two types of varactors exist, namely pn-junction varactors and MOS varactors. Because p-substrate is connected to the ground, n+/p-well varactors are single-ended. p+/n-well varactors, on the other hand, are floating varactors. The swing of the voltages at the nodes of the varactors must ensure that the n+/p-well and p+/n well junctions be revise biased all the time such that a junction capacitance exists. The junction capacitance of an abrupt pn-junction is given by:

$$C_J = \frac{C_{Jo}}{\sqrt{1 + \frac{v_R}{\phi_o}}},$$

(2.4)

Where C_{Jo} is the junction capacitance at zero-biasing voltage, v_R is the reverse biasing voltage of the junction and φo is built-in potential of the junction. It is seen that C_J varies with v_R in a nonlinear fashion. The performance of junction varactors is affected by the following factors: Large parasitic series resistance - p+/n-well varactors suffer from a large series resistance - the resistance of the n-well. As a result, the quality factor of the varactor quantified by:

$$Q = \frac{1}{\omega R_{n-well} C},$$

(2.5)

- Large parasitic capacitance between n-well and p-substrate - The larger the capacitance of the varactors, the larger the n-well and subsequently the larger the n-well/p-substrate junction capacitance.
- Small capacitance tuning range - The nonlinear characteristics of *CJ* result in a small capacitance tuning range with a low capacitance tuning ratio.
- Stringent voltage swing requirement - As pointed out earlier that the p+/n-well and n+/p-well junctions must remain in a reverse biasing condition all the time to ensure the existence of a junction capacitance. This imposes a stringent constraint on the swing of the voltage across the terminals of the varactors.

2.2.3 Quality Factor

The quality factor *Q* of an inductor quantifies the ratio of the net magnetic energy stored in the inductor to its ohmic loss in one oscillation cycle. For spiral inductors, the quality factor of these inductors is independent of the voltage / current of the inductors. This property, however, does not hold for active inductors as the inductance of these inductors depends upon the transconductances of the transconductors constituting the active inductors and the load capacitance. When active inductors are used in applications such as LC oscillators, the inductance of the active inductors is a strong function of the swing of the voltage and current of the oscillators.

To quantify the ratio of the net magnetic energy stored in the inductor to its ohmic loss in one oscillation cycle and relate it to the performance of LC oscillators, in particular, the phase noise of the oscillators, an alternative definition of the quality factor that accounts for the swing of the voltage / current of the active inductors is needed. The quality factor *Q* of an inductor quantifies the ratio of the net magnetic energy stored in the inductor to its ohmic loss in one oscillation cycle.

$$Q = 2\pi \times \frac{\text{Net magnetic energy stored}}{\text{Energy dissipated in one oscillation cycle}}. \tag{2.6}$$

For a linear inductor, the complex power of the active inductor is obtained from:

$$P(j\omega) = I(j\omega)V^*(j\omega) = \text{Re}[Z]|I(j\omega)|2 + j\ \text{Im}[Z]|I(j\omega)|2 \tag{2.7}$$

where Re[*Z*] and Im[*Z*] are the resistance and inductive reactance of the inductor, respectively, $V(j\omega)$ and $I(j\omega)$ are the voltage across and the current through the inductor, respectively, the superscript $*$ is the complex conjugation operator, and $|.|$ is the absolute value operator. The first term in (7) quantifies the net energy loss arising from the parasitic resistances of the inductor, whereas the second term measures the magnetic energy stored in the inductor.

Active inductors are linear when the swing of the voltages / currents of the inductors are small and all transistors of the active inductors are properly biased. The quality factor of a lossy gyrator-C active inductor can be derived directly

$$Q = \left(\frac{\omega L}{R_s}\right) \frac{R_p}{R_p + R_s\left[1 + \left(\frac{\omega L}{R_s}\right)^2\right]} \left[1 - \frac{R_s^2 C_p}{L} - \omega^2 L C_p\right].$$

(2.8)

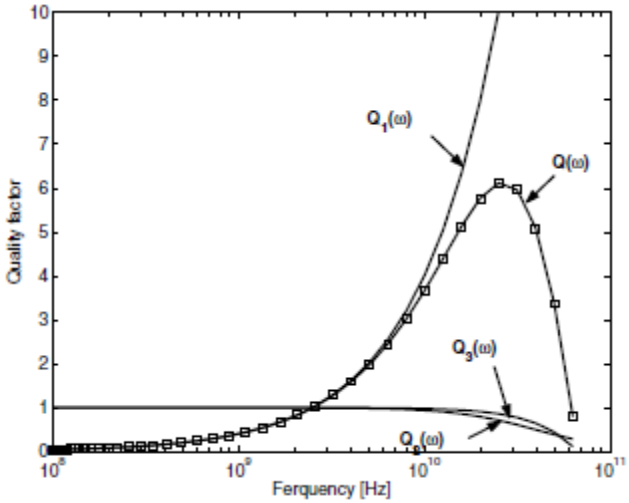


Figure: 2.5. Frequency dependence of the quality factor of active inductors.

2.2.4 Noise

Active inductors exhibit a high level of noise as compared with their spiral counterparts. To analyze the noise of a gyrator-C active inductor, the power of the inputreferred noise-voltage and that of the noise-current generators of the transconductors constituting the active inductor must be derived first. The power of the input-referred noise-voltage generator, denoted by *v*2*n* , and that of the input-referred noisecurrent generator, denoted by *i*2 *n*, of these transconductors can be derived using conventional noise analysis approaches for 2-port networks, and the results are given in Table 1.1 where

$$i2nD = 4kT\,(\gamma + Rggm)\,gm\Delta f$$

(2.9)

represents the sum of the power of the thermal noise generated in the channel of MOSFETs and the thermal noise of the gate series resistance of MOSFETs, *Rg* is the gate series resistance, γ = 2.5 for deep sub-micron devices, *T* is the temperature in degrees Kelvin, and *k* is Boltzmann constant. The effect of the flicker noise of MOSFETs, which has a typical corner frequency of a few MHz [71], is neglected. The thermal noise of other parasitics of MOSFETs, such as the thermal noise of the bulk resistance of the

source and drain diffusions, is also neglected. To illustrate how the results of Table 1.1 are derived, consider the commongate transconductor. To derive the input-referred noise-voltage generator *v*2*n* of the transconductor, we first short-circuit the input of the transconductor.

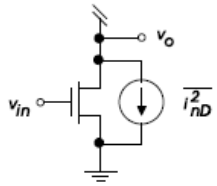
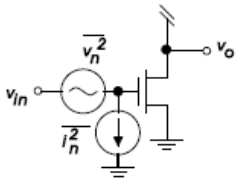
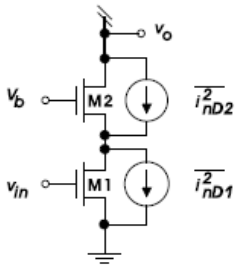
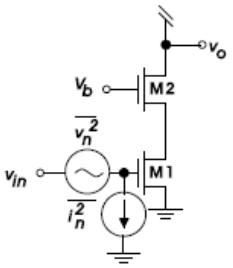
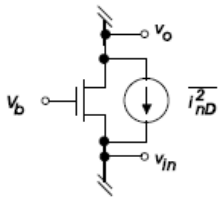
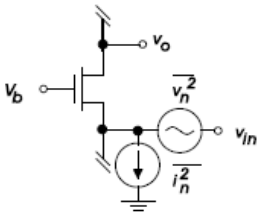
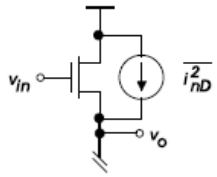
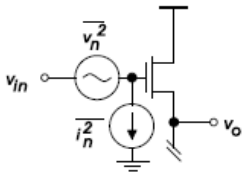
	Transconductors with noise sources	Transconductors with noise generators
Common source		
Cascode		
Common gate		
Source follower		

Table: 2.1. Input-referred noise-voltage and noise-current generators of transconductors at low frequencies.

2.2.5 Linearity

The preceding development of gyrator-C active inductors assumes that the transconductors of the active inductors are linear. This assumption is only valid if the swing of the input voltage of the transconductors is small. When the voltage swing is large, the transconductors will exhibit a nonlinear characteristic and the synthesized active inductors are no longer linear. The linearity constraint of active inductors sets the maximum swing of the voltage of the active inductors. If we assume that

thetransconductances of the transistors of gyrator-C active inductors are constant when the transistors are biased in the saturation, then the maximum swing of the voltage of the active inductors can be estimated from the pinch-off condition of the transistors.

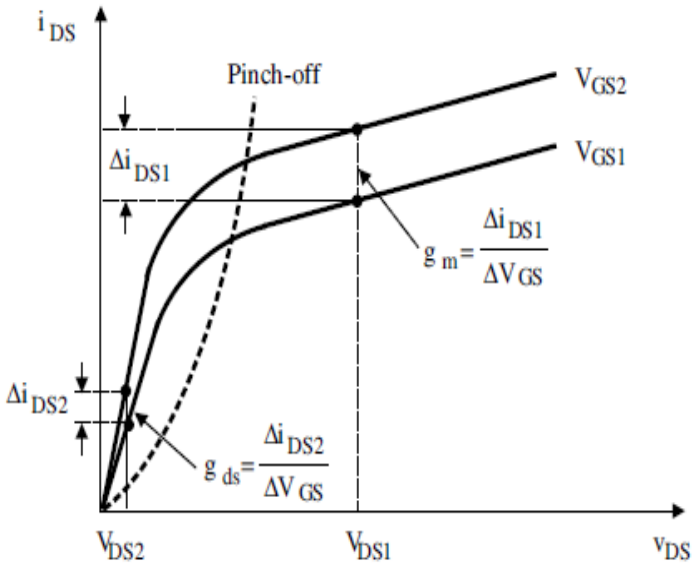


Figure: 2.6 Transconductance of MOSFETs in the saturation and triode regions. Because Δ*iDS*1 > Δ*iDS*2, *gm* > *gds* follows.

When the transistors of active inductors enter the triode region, the transconductances of the transistors decrease from g_m (saturation) to g_{ds} (triode) in a nonlinear fashion, as illustrated graphically in Figure: 2.6. It should be emphasized that although the transconductances of the transconductors of gyrator-C networks drop when the operating point of the transistors of the transconductors moves from the saturation region to the triode region, the inductive characteristics at port 2 of the gyrator-C network remain. The inductance of the gyrator-C active inductors, however, increases from $L = \frac{C}{Gm1Gm2}$ to $L = \frac{C}{Gds1Gds2}$ where Gm1,m2 are the transconductances of transconductors 1 and 2 respectively when (a) (b) in the saturation and Gds1,ds2 are the transconductances of transconductors 1 and 2 respectively when in the triode. It should also be noted that the parasitic resistances of active inductors also vary with the voltage swing of the active inductors.

2.2.6 Supply Voltage Sensitivity

The supply voltage sensitivity of the inductance of active inductors is a figure-ofmerit quantifying the effect of the variation of the supply voltage on the inductance of the active inductors. The fluctuation of the supply voltage of a mixed analog-digital system is mainly due to the switching noise of the system [10]. Assume that the supply voltage of a mixed-mode system containing an active inductor varies from V_{DD} and $V_{DD}+\Delta V_{DD}$, where ΔVDD is a random variable with $E[\Delta V_{DD}] = 0$, where E[.] denotes the mathematical mean operator. For a well designed mixed-mode system, $\Delta V_{DD}\_V_{DD}$ holds. The small-signal analysis approach can therefore be employed to analyze the effect of ΔV_{DD} on the inductance of the active inductor. Following the definition of normalized sensitivity, the normalized sensitivity of the inductance of an active inductor to the supply voltage is defined as

$$S_{V_{DD}}^{L} = \frac{V_{DD}}{L}\frac{\partial L}{\partial V_{DD}}.$$

(2.10)

The fluctuation of the supply voltage VDD affects the inductance of the active inductor mainly by altering the dc operating point, subsequently the transconductances of the transconductors constituting the active inductor. By assuming that the load capacitance C of the gyrator-C active inductor does not vary with VDD and because $L = \frac{C}{Gm1Gm2}$, we arrive at:

$$\frac{\partial L}{\partial V_{DD}} = -L\left(\frac{1}{G_{m1}}\frac{\partial L}{G_{m1}} + \frac{1}{G_{m2}}\frac{\partial L}{G_{m2}}\right).$$

(2.11)

The normalized supply voltage sensitivity of the active inductor is given by:

$$S_{V_{DD}}^{L} = -\left(S_{V_{DD}}^{G_{m1}} + S_{V_{DD}}^{G_{m2}}\right),$$

(2.12)

Where *SGm*1*VDD* and *SGm*2 *VDD* are the normalized supply voltage sensitivity of *Gm*1and *Gm*2, respectively. Eq. (12) reveals that both *S Gm*1 *VDD* and *SGm*2 *VDD*

contribute equally to *SL VDD*. To minimize the supply voltage sensitivity of active inductors, transconductors with a constant *Gm* should be used.

2.2.7 Parameter Sensitivity

The minimum feature size of MOS devices in modern CMOS technologies has been scaled down more aggressively as compared with the improvement in process tolerance such that the effect of process variation on the characteristics of circuits becomes increasingly critical. For example, the resistance of poly resistors in a typical 0.18μm CMOSprocess has an error of ±20%approximately and that of n-well resistors has an error of ±30% approximately. Analysis of the effect of parameter spread is vital to ensure that the performance of circuits meets design specifications once the circuits are fabricated. Active inductors consist of a number of active devices and their performance is greatly affected by the parameter spread of these components. The normalized sensitivity of the inductance of an active inductor to a parameter *xj* of the inductor defined as

$$S_{x_j}^{L} = \frac{x_j}{L}\frac{\partial L}{\partial x_j} \tag{2.13}$$

By assuming that the parameters of the active inductor are Gaussian distributed and uncorrelated, the overall effect of the variation of the parameters of the active inductor on the inductance of the inductor is obtained from

$$\sigma_L^2 = \sum_{j=1}^{N} \left(\frac{\partial L}{\partial x_j}\right)^2 \sigma_{x_j}^2, \tag{2.14}$$

where σL and σxj denote the standard deviations of L and xj , respectively, and N is the number of the parameters of the active inductor.

There are two ways in which circuit designers can analyze the effect of parameter spread on the inductance of active inductors, namely worst-case analysis, also known as corner analysis, and Monte Carlo analysis. The former determines the inductance of active inductors at process corners while the latter quantifies the degree of the spread of the inductance of active inductors around the nominal inductance of the inductors. The

accuracy of Monte Carlo analysis increases with an increase in the number of simulation runs and is therefore extremely time consuming. Corner analysis, on the other hand, is time-efficient but the results obtained from corner analysis are typically over conservative. Despite of this, corner analysis is the most widely used method to quantify the effect of process spread.

2.2.8 Signal Sensitivity

Unlike spiral inductors whose inductance is independent of the voltage andcurrent of the inductors, the inductance of gyrator-C active inductors varies with the voltage and current of the transconductors constituting the active inductors. This is because the transconductances *Gm*1 and *Gm*2 of the transconductors are signal dependent when signal swing is large. When an active inductor is used in applications where the voltage of the active inductor experiences a large degree of variation, such as active inductor LC oscillators, the transconductances of the transconductors of the active inductor vary with the signal swing. As a result, the inductance, parasitic resistances, and quality factor of the active inductor all vary with the signal swing.

2.2.9 Power Consumption

Spiral inductors do not consume static power. Gyrator-C active inductors, however, consume dc power, mainly due to the dc biasing currents of their transconductors. The power consumption of gyrator-C active inductors themselves is usually not of a critical concern because the inductance of these inductors is inversely proportional to the transconductances of the transconductors constituting the inductors. To have a large inductance, *Gm*1 and *Gm*2 are made small. This is typically achieved by lowering the dc biasing currents of the transconductors. When replica-biasing is used to minimize the effect of supply voltage fluctuation on the inductance of active inductors, as to be seen shortly, the power consumed by the replica-biasing network must be accounted for. Also, when negative resistors are employed for boosting the quality factor of active inductors, their power consumption must also be included. Often the power consumption of an active inductor is set by that of its replica-biasing and negative resistor networks.

2.3 The Gyrator

Most of active inductor designs are based on the principle of gyrator able to function as an impedance inverter connected to a capacitive load as shown in Figure 2.7. This circuit is constituted by two transconductors in a feedback loop with an integrating capacitor (gyrator-C) in order to emulate an inductor effect. Historically, this network is called gyrator-C network.

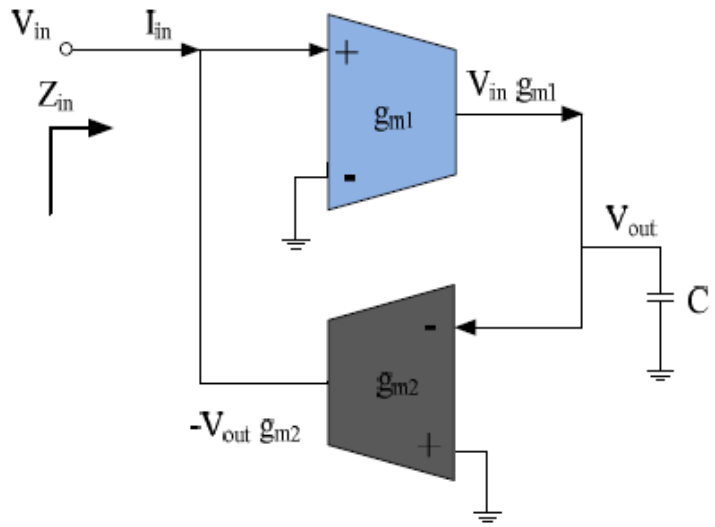


Figure: 2.7 Principle of lossless single-ended gyrator-C active inductors.

This model was proposed in 1949 by Henry Tellegen. This gyrator has at its input impedance directly proportional to the inverse of its load impedance. Indeed, the application of a positive voltage at its input makes it possible to circulate a current that generates a negative transconductance gm1 and a positive transconductance gm2 in the direction of counter-reaction.

This gyrator-C network is said to be lossless when the two impedances of the input and output transconductances of the network are infinite. However, this medialization is only available in the ideal case, because in reality it is impossible to find transistors having models with pure transconductances and infinite input impedances. Indeed, the impedances at nodes 1 and 2 are finite due to the direct dependence of the

conductances gds1 and gds2 of the intrinsic characteristics of two transistors realizing the gyrator-C network.

2.3.1 Basic Principle

The impedance of an ideal inductor is described by the signal flow graph (SFG) as illustrated in Figure: 2.8 and equation (1), where s is the Laplace operator and L is the inductance of the inductor.

$$\frac{Vin}{Iin} = sL \tag{2.15}$$

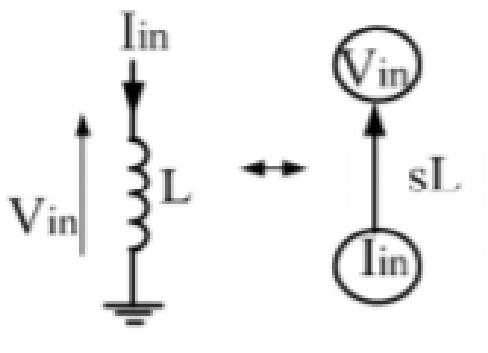


Figure: 2.8 an ideal inductor and its SFG representation

The same transfer function can be obtained by using one capacitor and two transconductance (one positive and one negative) amplifiers as shown in Fiigure: 2.7 is called as gyrator-C network. Considering Iin and Vin as current and voltage at input node, resultant impedance can be derived as:

$$\frac{Vin}{Iin} = \frac{sC}{Gm1Gm2} \tag{2.16}$$

$$L = \frac{C}{Gm1Gm2} \tag{2.17}$$

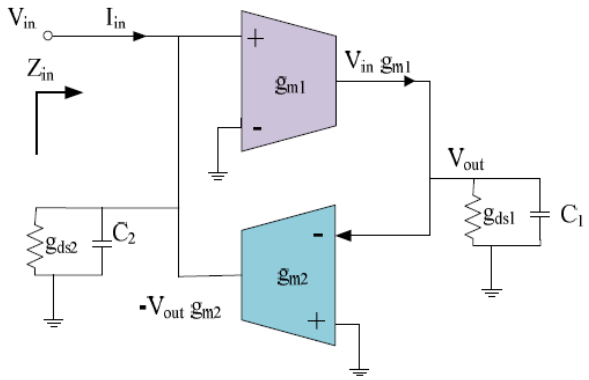


Figure: 2.9 Principle of lossy single-ended gyrator-C active inductors.

As shown in the figure: 2.9, we have

$$(sC1 + gds1)Vout – gm1\ Vin = 0 \tag{2.18}$$

$$(sC1 + gds2)Vin + gm2\ Vout - Vin = 0 \tag{2.19}$$

Therefore, we can conclude that:

$$V_{in}\left(\frac{(sC_2 + g_{ds2})(sC_1 + g_{ds1}) + g_{m1}g_{m2}}{sC_1 + g_{ds1}}\right) = I_{in} \tag{2.20}$$

The admittance Yin looking into port 2 of the gyrator-C network is expressed as:

$$Y_{in}(s) = sC_2 + g_{ds2} + \frac{g_{m1}g_{m2}}{sC_1 + g_{ds1}} \tag{2.21}$$

2.4 Principles of Gyrator-C Active Inductors

2.4.1 Lossless Single-Ended Gyrator-C Active Inductors

A gyrator consists of two back-to-back connected transconductors. When one port of the gyrator is connected to a capacitor, as shown in Figure: 2.10, the network is called the gyrator-C network. A gyrator-C network is said to be lossless when both the input and output impedances of the transconductors of the network are infinite and the transconductances of the transconductors are constant. Consider the lossless gyrator-C network shown in Figure 2.10(a). The admittance looking into port 2 of the gyrator-C network indicates that port 2 of the gyrator-C network behaves as a singleended lossless inductor with its inductance given by Gyrator-C networks can therefore be used to synthesize inductors.

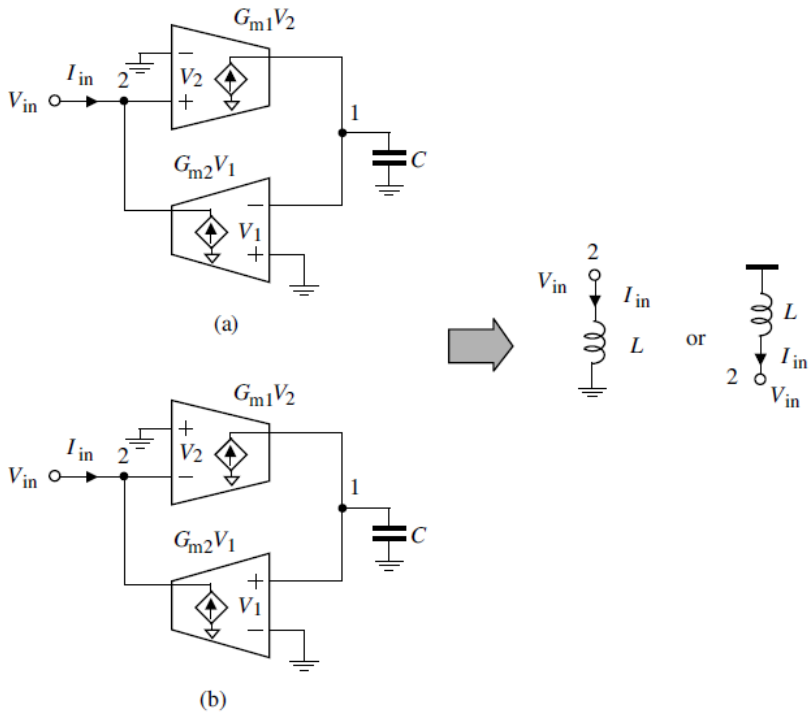


Figure: 2.10 Lossless singe-ended gyrator-C active inductors. *Gm*1 and *Gm*2 are the transconductances of transconductors 1 and 2, respectively, and *C* is the load capacitance at node1. (a) Transconductor in the forward path has a positive transconductance while the transconductor in the feedback path has a negative transconductance; (b) Transconductor in the forward path has a negative transconductance while the transconductor in the feedback path has a positive transconductance

These synthesized inductors are called gyrator- active inductors. The inductance of gyrator-C active inductor is directly proportional to the load capacitance *C* and inversely proportional to the product of the transconductances of the transconductors of the gyrator. Also, the gyrator-C network is inductive over the entire frequency spectrum. It should also be noted that the transconductor in the forward path can be configured with a negative transconductance while the transconductor in the feedback path has a positive transconductance, as shown in Figure 2.10(b).

2.4.2 Lossless Floating Gyrator-C Active Inductors

An inductor is said to be floating if both the terminals of the inductor are not connected to either the ground or power supply of the circuits containing the active inductor. Floating gyrator-C active inductors can be constructed in a similar way as single-ended gyrator-C active inductors by replacing singleended transconductors with differentially-configured transconductors, as shown in Figure: 2.11.

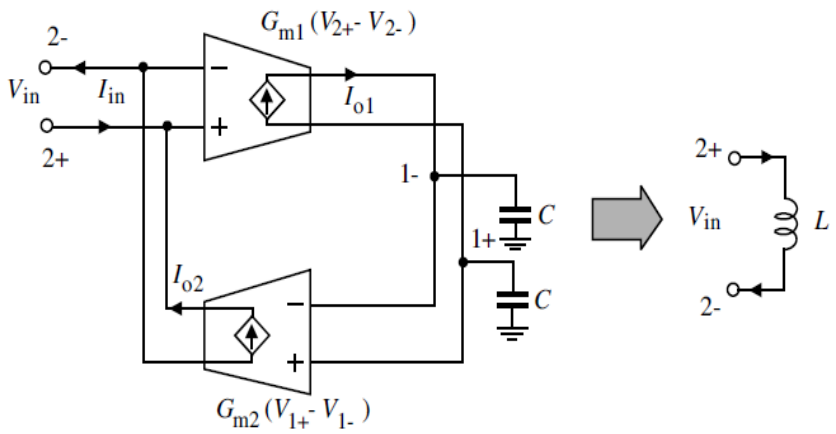


Figure: 2.11 Lossless floating gyrator-C active inductors. Gm1 and Gm2 are the transconductances of transconductors 1 and 2, respectively, and C is the load capacitance at nodes 1+ and 1-

Floating gyrator-C active inductors offer the following attractive advantages over their single-ended counterparts: (i) the differential configuration of the transconductors effectively reject the common-mode disturbances of the network, making them particularly attractive for applications where both analog and digital circuits are fabricated on the same substrate.

(ii) The level of the voltage swing of floating active inductors is twice that of the corresponding single-ended active inductors.

2.4.3 Lossy Single-Ended Gyrator-C Active Inductors

When either the input or the output impedances of the transconductors of gyratorC networks are finite, the synthesized inductors are no longer lossless. Also, the gyrator-C networks are inductive only in a specific frequency range. Consider the gyrator-C network shown in Figure: 2.12 where Go1 and Go2 denote the total conductances at nodes 1 and 2, respectively. Note Go1 is due to the finite output impedance of transconductor 1 and the finite input impedance of transconductor 2. To simplify analysis, we continue to assume that the transconductances of the transconductors are constant. Write KCL at nodes 1 and 2.

$$(sC_1 + G_{o1})V_1 - G_{m1}V_2 = 0 \tag{2.22}$$

$$-I_{in} + (sC_2 + G_{o2})V_2 - G_{m2}(-V_1) = 0 \tag{2.23}$$

The admittance looking into port 2 of the gyrator-C network is obtained from:

$$\begin{aligned} Y &= \frac{I_{in}}{V_2} \\ &= sC_2 + G_{o2} + \frac{1}{s\left(\frac{C_1}{G_{m1}G_{m2}}\right) + \frac{G_{o1}}{G_{m1}G_{m2}}}. \end{aligned} \tag{2.24}$$

Equation (24) can be represented by the RLC networks shown in Figure: 2.12, with its parameters given by:

$$R_p = \frac{1}{G_{o2}},$$

$$C_p = C_2,$$

$$R_s = \frac{G_{o1}}{G_{m1}G_{m2}},$$

$$L = \frac{C_1}{G_{m1}G_{m2}}.$$

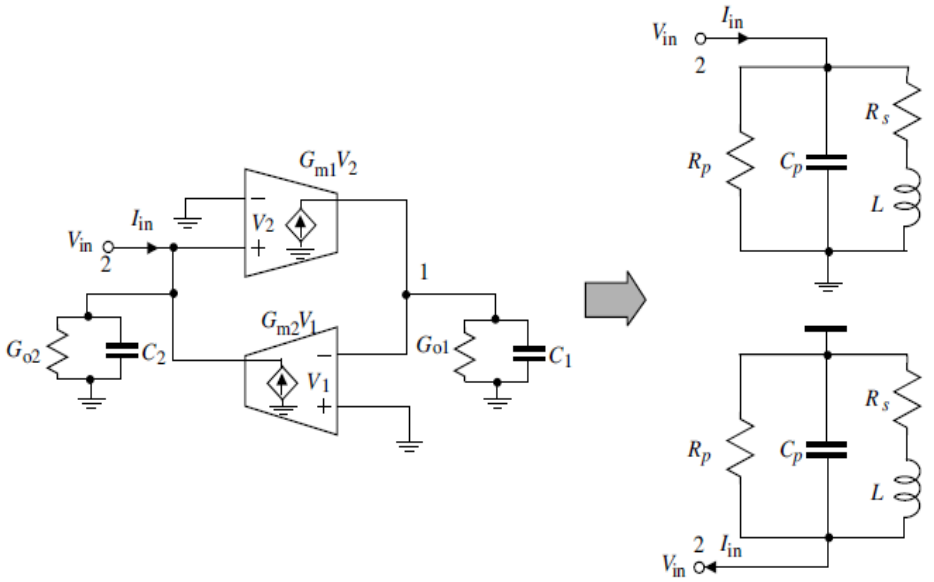


Figure: 2.12 Lossy single-ended gyrator-C active inductors. C1 and Go1, C2 and Go2 denote the total capacitances and conductances at nodes 1 and 2, respectively.

2.4.4 Lossy Floating Gyrator-C Active Inductors

Lossy floating gyrator-C active inductors can be analyzed in a similar way as lossy single-ended gyrator-C active inductors. Consider the lossy floating gyrator-C network shown in Figure: 2.13. We continue to assume that the transconductances of the transconductors are constant. Writing KCL at nodes 1-, 1+, 2-, and 2+ yields

$$-G_{m1}(V_2^+ - V_2^-) + \left(\frac{sC_1 + G_{o1}}{2}\right)(V_1^- - V_1^+) = 0,$$

$$I_{in} + \left(\frac{sC_2 + G_{o2}}{2}\right)(V_2^- - V_2^+) + G_{m2}(V_1^+ - V_1^-) = 0,$$

(2.25)

The admittance looking into port 2 of the gyrator-C network is obtained from:

$$\begin{aligned} Y &= \frac{I_{in}}{V_2^+ - V_2^-} \\ &= s\frac{C_2}{2} + \frac{G_{o2}}{2} + \frac{1}{s\left(\frac{C_1}{2G_{m1}G_{m2}}\right) + \frac{G_{o1}}{2G_{m1}G_{m2}}}. \end{aligned}$$

(2.26)

Equation (11) can be represented by the RLC network shown in Figure: 2.13 with its parameters given by:

$$R_p = \frac{2}{G_{o2}},$$

$$C_p = \frac{C_2}{2},$$

$$R_s = \frac{G_{o1}/2}{G_{m1}G_{m2}},$$

$$L = \frac{C_1/2}{G_{m1}G_{m2}}.$$

The capacitance and conductance at the interface nodes 1+ and 1− and those at the internal nodes 2+ and 2− will become C2/2 and Go2/2, and C1/2 and Go21/2, respectively.

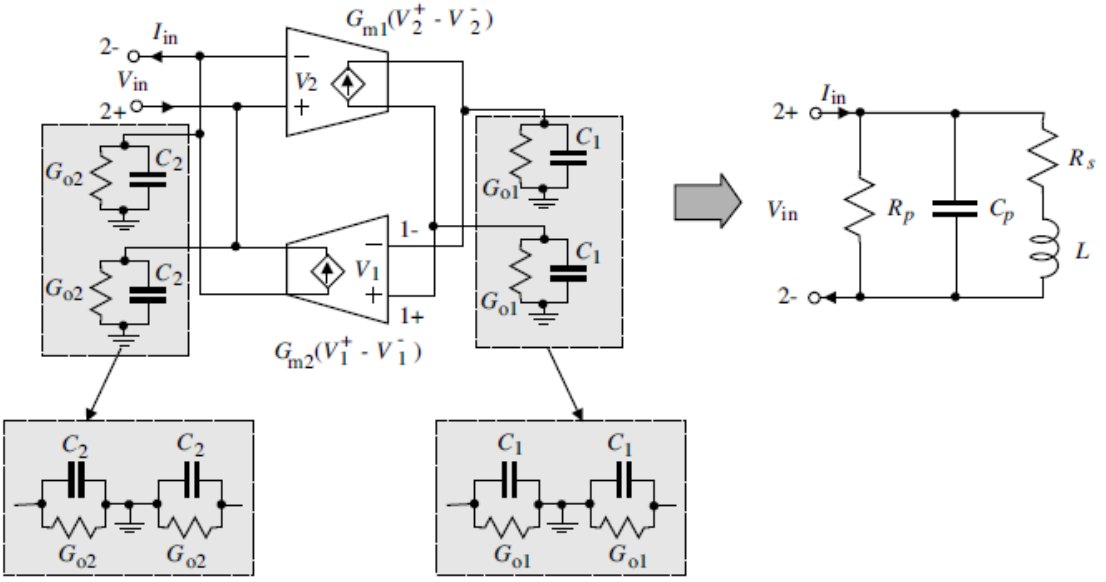


Figure: 2.13 Lossy floating gyrator-C active inductors. *C*1 and *Go*1, *C*2 and *Go*2 represent the total capacitances and conductances at nodes 1 and 2, respectively

Chapter 3

LITERATURE REVIEW

This chapter discusses the most recent work on the Active Inductor and the comparision between the proposed Active Inductor and other Active Inductors. Since, in a past few years with scaling in CMOS technology, autonomous communicating objects operating in wide frequency band have become very popular. While the most specification requirements of these above systems are wide tuning range, high gain and low noise, active devices especially active inductors, have become one of the most important alternatives solution for multi-band Integrated Circuits (ICs) designing.

3.1 Different topologies of adjustable active inductors

- Single MOS active inductor
- Karsilayan-Schaumann active inductor
- Thanachayanont active inductor
- Common source topology
- Common gate topology
- Cascode topology
- Low Power, High Q-Factor Grounded ActiveInductor

3.1.1 Single MOS active inductor

From the theory of analog circuit design, it is well known that the number of poles of a transfer function is dependent on the number of circuit nodes and thus, using a large number of transistor stages will degrade the frequency capability [9]. This is the reason why Hara has proposed an active inductor structure constituted by a single transistor and resistance as presented in Figure 3.1. The single solution while still using the gyrator principle is to reduce the transistors number, fact that signifies actually a consequently replace of transconductors with simpler stages with similar function.

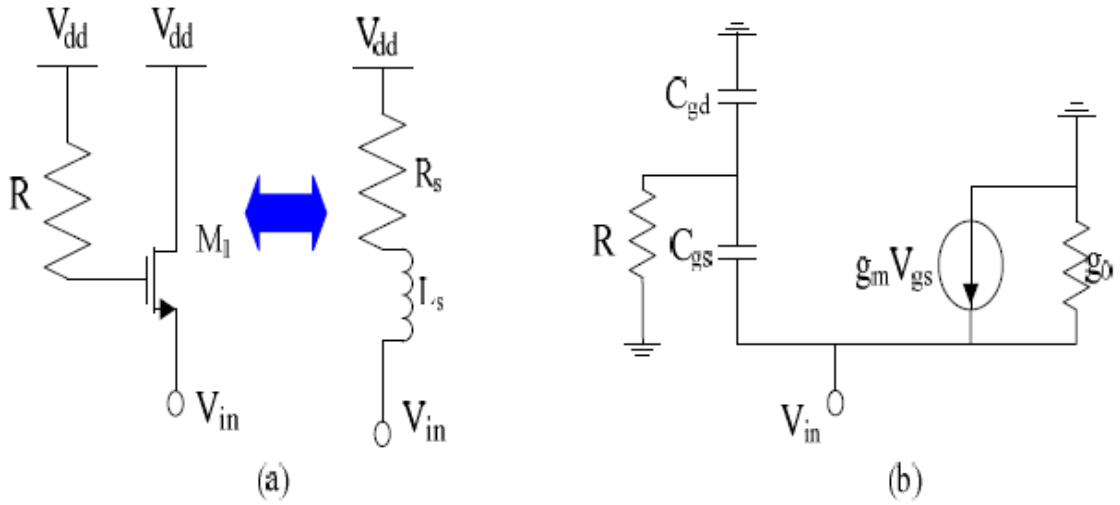


Figure: 3.1 Hara Active inductor; (a) Structure, (b) equivalent model.

The expression of equivalent impedance, series resistance and equivalent inductance are given by:

$$Z_{in}(s) \approx \left(\frac{1}{RC_{gs}C_{gd}}\right)\frac{sRC_{gd}+1}{s^2+s\frac{g_m}{C_{gs}}+\frac{g_m}{RC_{gs}C_{gd}}}$$

$$R_s = \frac{1}{gm}$$

$$L = \frac{RC_{gs}}{gm}$$

(3.1)

The tuning of theresistance R or the transconductance gm1 determines an independent tuning of the active circuit. Consequently, a lossless simulated inductor is obtained. In reference [1], this circuit can be tuned from 1 to 14 nH achieving a maximum quality factor around 65 at 8 GHz. However, the power consumption is very high and it can be greater than 70 mW. Nevertheless, Hara active inductor has been widely used in literature owing to its simplicity of implementation.

3.1.2 Karsilayan-Schaumann active inductor

In 2000, Karsilayan and Schaumann have developed a new adjustable active inductor as shown in Figure: 3.2. For this configuration, the transistors M1 and M2 have been implemented as a differential pair producing a negative transconductance while the positive transconductance is produced by transistor M3. An auxiliary capacitance Cgs3 is added between the gate and source of transistors M3 in order to enhance the equivalent inductance L [1].

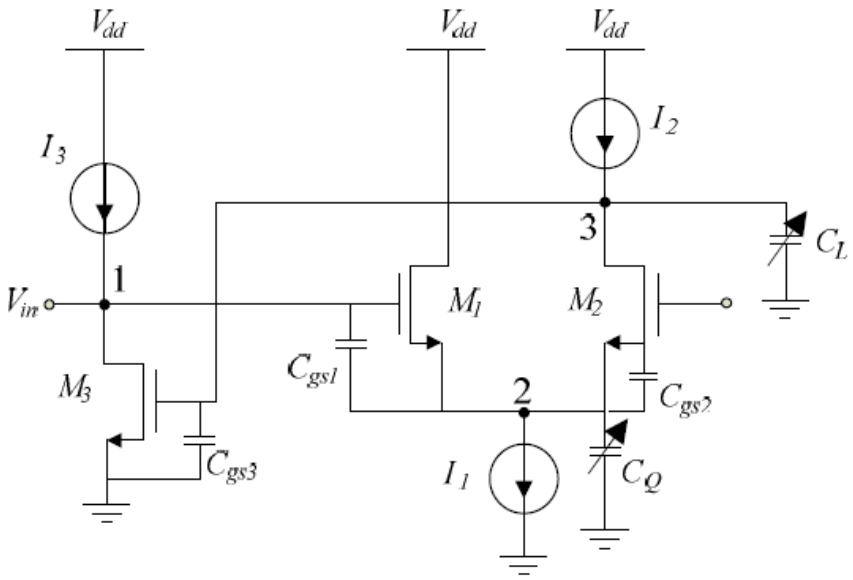


Figure: 3.2 Karsilayan and Schaumann Active inductor.

This structure introduces a possibility of reconfiguration through variable capacitances CQ and CL implemented as a PMOS varactor. Indeed, the inductor value can be tuned from 420 to 627 nH either by changing a capacitor CL via a substrate bias voltage or by a bias current, The tuning of the quality factor Q can be regulated independently from L from 30 to 390 by varying a varactor CQ substrate bias, with no additional power consumption. The equivalent inductance and quality factor are given by:

$$L = \frac{2(C_I + C_{gs})}{g_m g_{m3}} \tag{3.2}$$

$$Q = \frac{2\omega C_{gs}}{g_{ds2} + 2g_{ds3} - \omega^2 (\frac{C_Q + C_{gs}}{g_m})} \quad (3.3)$$

By analysing the accomplished performances for this circuit, we can conclude that although the obtained results are interesting, the adjustment in terms of inductance value is limited, the power consumption is higher and the quality factor still low.

3.1.3 Thanachayanont active inductor

This is the most used topology in the of active inductors design. In 1996, Thanachayanont and Payne proposed this structure (Figure: 3.3) that is known as the simple grounded active inductor [8]. It is composed by two transistors M1 and M2 where the drain of the first is connected to the gate of the second. These two transistors operate as an impedance inverter network performing the gyrator function. Two current sources I1 and I2 are used to polarize the circuit. This gyrator inverts the total capacitance at node 1 to an inductive impedance at node 2 (input voltage Vin).

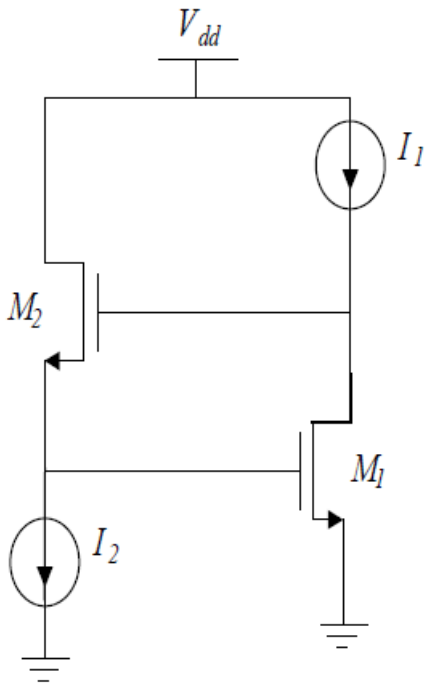


Figure: 3.3 Thanachayanont and Payne Active inductor.

The modeling of this architecture is based on an alternative strategy that can be called "parasitic method" making use of the intrinsic parameters to establish the necessary poles and the zeros in the transfer function. Since each transistor is modeled by Cgs, Cgd, gds and gm, then the equivalent input impedance of this circuit can be derived as follows.

$$Z_{in} \approx \frac{(g_{ds1} + g_{m2}) + s(C_{gs1} + C_{gd1} + C_{gd2})}{(sC_{gd1} + g_{ds1} + g_{m1})(s(C_{gs1} + C_{gd2}) + g_{m1})} \tag{3.4}$$

Where the equivalent inductance and quality factor are expressed as:

$$L \approx \frac{C_{gs1}}{g_{m1}g_{m2}}$$

$$Q \approx \sqrt{\frac{g_{m2}g_{m1}C_{gs1}}{g_{ds2}^2 C_{gs2}}} \tag{3.5}$$

Simulated with 0.8µm CMOS process provided by Northern Telecom, this topology can be tuned in the range of few hundreds of nH by varying the bias current source I1 and a self-resonance frequency up to 1 GHz can be achieved. The obtained quality factor is about 100 with power consumption higher than 10 mW.

3.1.4 Common Source Topology

Common source amplifier is typically used as a voltage or transconductance amplifier. It consists of a grounded-source MOS transistor with the drain having a resistor or a current source. Bandwidth of common source amplifier tends to be low, due to high capacitance resulting from the miller effect. It exhibits a very high input resistance however its output resistance is also high. This circuit can be designed to obtain a voltage gain of 15 to 100.

3.1.5 Common Gate Topology

Common gate amplifier is used as a current buffer or voltage amplifier. In this circuit the source terminal of the transistor serves as the input, the drain is the output and the gate is

connected to the ground or “common”, hence, its name. This configuration is used less often than the common source amplifier. Gain of this circuit is very less. Because the input impedance of the common gate is very low, the cascode topology is often used.

3.1.6 Cascode Topology

By placing a common-gate amplifier stage in cascade with a common-source amplifier stage, a very useful and versatile amplifier circuit results. It is known as the cascode configuration. The basic idea behind the cascode amplifier is to combine the high input resistance and the large transconductane achieved in a common-source amplifier with the current-buffering property and the superior high frequency response of the common-gate circuit. It can be designed to obtain a wider bandwidth.

3.1.7 Low Power, High Q-Factor Grounded ActiveInductor

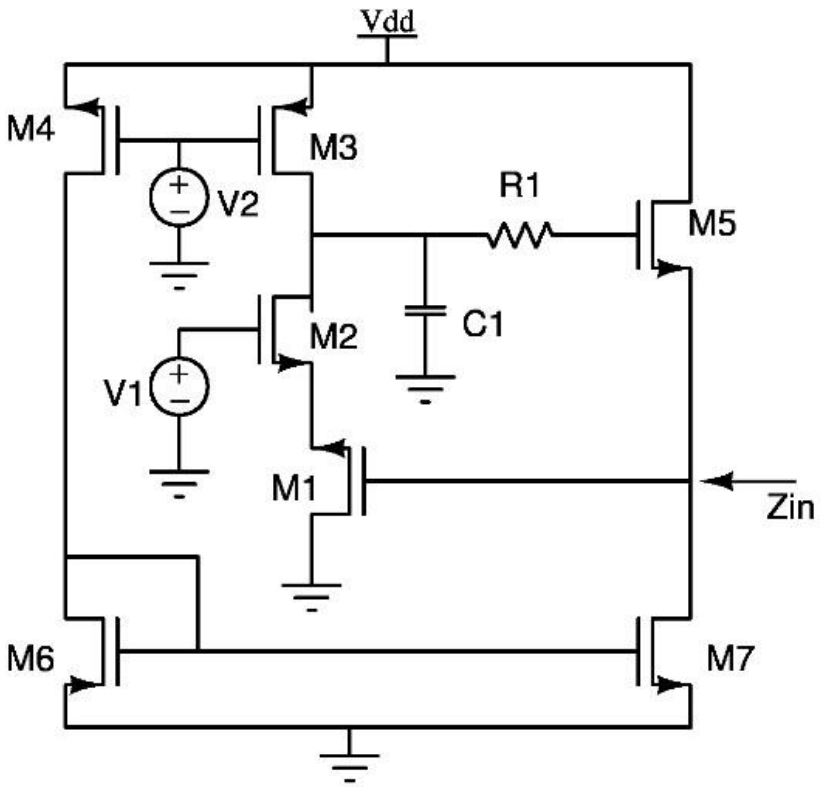


Figure: 3.4 Low Power, High Q-Factor Grounded ActiveInductor

Paper [10] presented a low power grounded active inductor based on gyrator-C topology. The proposed circuit is designed in 0.18 um CMOS process and simulated in cadence environment. The simulation results of the proposed active inductor shows maximum quality factor of 341 at 2.51 GHz. The inductive bandwidth of the circuit is obtained as 0.79-2.69GHz. The designed active inductor provides the inductance value of as high as 180nH which makes it suitable for a wide range of applications. The circuit shows good performance in all aspects while consuming only 1mW of Dc power. The circuit also shows very good noise performance compared to existing works.

In Figure: 3.4 transistors M1 and M5 form the basic topology of the circuit. To enhance the inductance value and the quality factor cascode structure is used in the design which is being implemented by adding transistor M2 in the feedback loop. A feedback resistor is included in the loop to further improve the performance of the circuit. The feedback resistor creates additional inductive reactance which increases the inductance of the designed active inductor. Transistors M3 and M7 works as current sources and transistors M4 and M6 form the current mirror circuit.

Two voltage sources are used to bias the respective transistors in saturation region. The biasing of transistor M2 is very important as it helps to reduce the output conductance which in turn improves the inductive behaviour of the circuit. The circuit is designed for low bias current to reduce the power consumption. Also wider transistors have not been used in the design as it reduces the self-resonant frequency.

3.2 Comparsion between CS, CG and Cascode topologies

There are three main topologies, which are common source (CS), common gate (CG), and cascode. The characteristics of the three topologies are shown in Table: 3.1 show a comparison of the three topologies. The cascode amplifier is the most popular solution for LNA since it provides the highest gain over the widest bandwidth with only a slight sacrifice in NF performance and design complexity. The structure of a cascode amplifier combines a CS stage and a CG stage. The CS stage provides the greatest stability which has better sensitivity to process, temperature variation immunity, power supply, and component variations.

Characteristic	**CS**	**CG**	**Cascode**
NF	Lowest	Rises Rapidly with Frequency	Slightly higher than CS
Gain	Moderate	Lowest	Highest
Linearity	Moderate	High	Potentially Highest
Bandwidth	Narrow	Fairly Broad	Broad
Stability	Often requires compensation	Higher	Higher
Reverse Isolation	Low	High	High

Table: 3.1 Characteristics of CS, CG, and Cascode Topologies.

Chapter 4

SOFTWARE

4.1 Introduction

The intention of this section is to serve as an introduction to the Cadence design environment and describe the methododology used when designing integrated circuits. The department is not giving courses in Cadence but in integrated circuit design so only the minimum knowledge, needed to run the laboraties, of Cadence can be gained from this manual. Also this manual describes the environment currently at the department which is Cadence version 4.45 in conjunction witch a Design Kit from AMS (AustriaMikro Systeme International AG) which contains a set of rules and designs for a 0.35 μm CMOS process.

The Cadence tool kit consists of several programs for different applications such as schematic drawing, layout, verification, and simulation. These applications can be used on various computer platforms. The open architecture also allows for integration of tools from other vendors or of own design. The integration of all this tools is done by a program called Design Framework II (DFW). The DFW-application is the cornerstone in the Cadence environment. It provides a common user interface and a common data base to the tools used. This makes it possible to switch between different applications without having to convert the data base.

4.2 Cadence User Interface

In Cadence the user interface is graphic and based on windows, forms, and menus. The main windows of DFW are: Command Interpreter Window (CIW) is controlling the environment. Other tools can be started from here and it also serves a log window for many applications. Library Manager gives a view of the design libraries and the different constructions that exists therein.

- Design Window (DW) shows the current design. It is possible to have several DW opened at the same time with different, or the same, tools

- Text Window (TW) show text. It can be a log or report that was asked for, or an editor.

4.3 The Design Process

The design tools have a common structure of the designs. It is hierarchical and consists of libraries, views, and instances.

4.3.1 Libraries and Views

All design data in Cadence are organized in libraries. There are Reference Libraries which contains basic building blocks usable in the construction and Design Libraries which embodies the current design. Every library consists of cells and their different views, as in Figure: 4.1. A cell is a database object which forms a building block, an inverter for instance. A view represents some level of abstraction of the cell. It can be a schematic drawing, layout, or maybe some functional description.

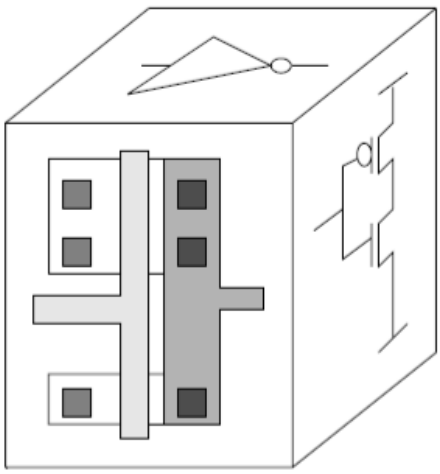


Figure: 4.1 an inverter cell with three views: layout, schematic, and symbol.

4.3.2 Instances and Hierarchy

The main reasons for using hierarchical designs are to save design time and minimize the size of the data base. Say that a design would need 500 gates of the same type.Then instead of building it 500 times, it is designed once and then used were it is needed.

In this way one cell can be used (not copied) several times and each such use are called an instance of the cell. In order to be instantiated every cell needs a symbol view which acts as a handle to the cell it represents. Only the symbol is shown when a cell is instantiated.

4.3.3 The Technology File

Since there are different semiconductor processes (with different set of rules and properties), Cadence has to know the specifications for the one that is to be used. This information is stored in a set of files called Technology Files which exists on different locations on the system. When a library is created it is therefore connected to a specific technology. The technology files contain information about:

4.3.4 The Design Flow

The abbreviated flow in Figure: 4.2 shows some of the steps in designing integrated circuits in the Cadence environment.

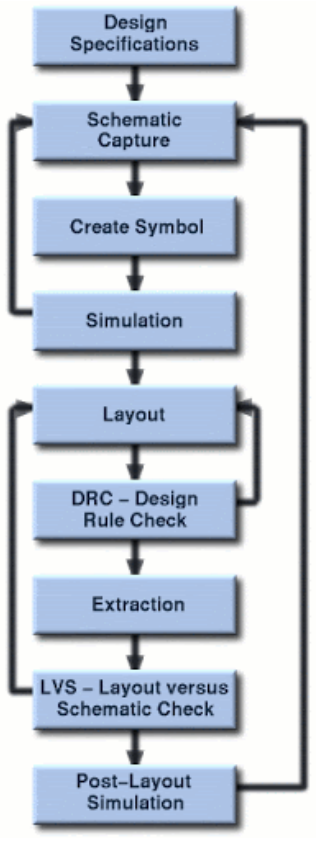


Figure: 4.2. The design flow

The step Create the Design consists of drawing schematic views of all cells and blocks. The schematic view contains transistor symbols, and maybe other component such as resistors and capacitances, and wires connecting them.

From the schematic view the symbol view is created (almost automatically) so that the cell can be used on a higher level in the hierarchy. The step Analyze the design includes functional verification (simulation) of the design on a schematic level. The third step, Create Layout, is done in a Layout Editor. Here the final semiconductor layers are represented by different colors. All the cells and blocks used have the size they will have on the final chip. The last step is Verification of the design. The layout is examined for violations against the geometric or electrical rules, and to verify the function of the physical implementation.

4.4 Simulation

The simulation tool is started directly from the schematic editor and all the necessary netlists describing the design will be created. A simulation is usually performed in a test bench, which is also a schematic, with the actual design included as an instance. The test bench also includes signal sources and power supply. By using parameters for the properties of the components used it is possible to quickly analyze the design for a wide range of variables. The simulator is run from within Affirma Analog Circuit Design Environment which is a tool that handles the interface between the user and the simulator. The current version of Cadence used at the department uses the Affirma Spectra Circuit Simulator.

The simulator offers a wide range of analyses (DC, frequency sweep, transient, noise, etc.) and the results can be presented graphically and be saved. The results (voltage levels, currents, noise, etc.) can be fed into a calculator which can present various parameters of the analyzed circuit - delay time, rise time, slew rate, phase margin, and many other interesting properties. It is also possible to set up algebraic expressions of in or output signal which can be plotted as a function of some other variable.

Chapter 5

PROPOSED DESIGN

Novel distortion reduction technique for active inductors is proposed. Low distortion active inductors using the proposed technique are introduced and they are applied to filter and voltage controlled oscillator (VCO). Validity of the proposed technique is confirmed by simulations.

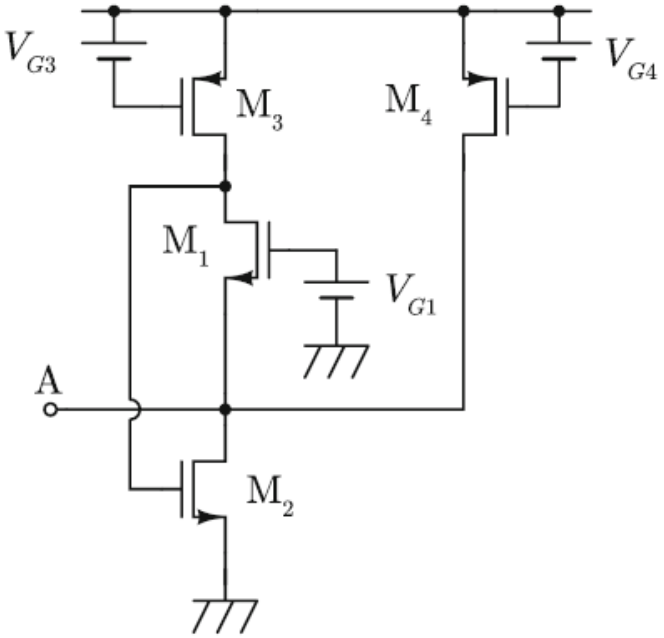


Figure: 5.1 Active inductor with high Q

Bias current of M1 and M2 is shared to reduce its power consumption. The configuration of gate-to-source capacitors of M1 or M2 is used as C. One of IN1 and IN2 can be used for input terminal. Its input admittance depends on the input terminal.

Self resonance angular frequency and Q are given by:

$$\omega o = \frac{1}{\sqrt{CpL}} = \sqrt{\frac{gm1gm2}{Cgs1Cgs2}} \quad (5.1)$$

$$Q = Rp\omega oCp = \sqrt{\frac{gm2Cgs1}{gm1Cgs2}}$$

(5.2)

Enlarging gm2 without increasing gm1 is effective in maximizing both of x0 and Q at the same time. In order to realize this condition a MOSFET M4 is often added as shown in Figure: 5.1, a part of bias current of M2 bypasses M1.

5.1 Proposed Distortion Reduction Technique.

Previous chapter, gm (transconductance) of a MOSFET is considered as constant and its non-linearity is ignored.However, drain current of a MOSFET is represented by

$$\begin{aligned} I_D &= K(V_{gs} + v_{in} - V_T)^2 \\ &= K(V_{gs} - V_T)^2 + 2K(V_{gs} - V_T)v_{in} + Kv_{in}^2 \\ &= I_{D0} + g_m v_{in} + \alpha v_{in}^2 \end{aligned}$$

(5.3)

Where Vgs and Vin is a gate-to-source bias voltage and an input signal voltage respectively and a is a constant coefficient. The first term of the right side of eq (5.3) means a constant bias current, the second term is a desired signal current which is proportional to the input voltage, and the last term is an undesired, nonlinear components.

Only when the input voltage is sufficiently small to ignore the third term of eq (5.3), a MOSFET is considered as linear transconductor. Only non-linearity of gm of a MOSFET is discussed because non-linearity of a transconductance gives more serious influence on the linearity of a active inductor.

Figure: 5.2 shows a basic concept of the proposed distortion reduction technique. Figure: 5.2 (a) or (b) is used instead of an n-channel MOSFET which acts as a transconductor. When a drain terminal of the MOSFET is used as an output terminal, the

MOSFET is replaced by Figure: 5.2 (a). When output node is a source terminal of a MOSFET, Figure: 5.2 (b) is used instead of the MOSFET

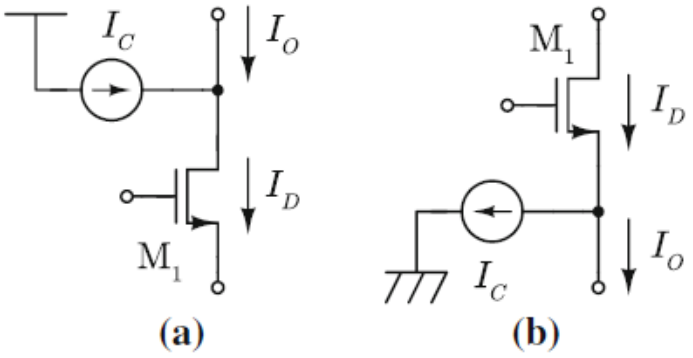


Figure: 5.2 Principle of distortion reduction technique

Output current of Figure: 5.2 is given as:

$$Io=Id- Ic \tag{5.4}$$

Where Ic is compensation current. If Ic contains the same nonlinear components with Id, Io becomes

$$Io = [Id0+gmVin + \alpha Vin\hat{}2]-[Ic0 + \alpha Vin\hat{}2] \tag{5.5}$$

$$Io= [Id0 +Ic0] +gmVin \tag{5.6}$$

Where Ic0 is a DC component of Ic. The nonlinear components of Id are canceled out. This compensation current Ic is also realized by a n-channel MOSFET Mc. It is assumed that M1 and Mc have the same channel width and length.

5.2 Low distortion active inductor design

Low distortion active inductor is derived from Figure: 5.1 The proposed technique is applied to M2 which acts as a common source amplifier because input voltage is amplified by M1 which acts as a common gate amplifier and it becomes the gate-to-

source voltage of M2. M2 is replaced by Figure: 5.2 (a) in order to suppress distortion occurs at M2.

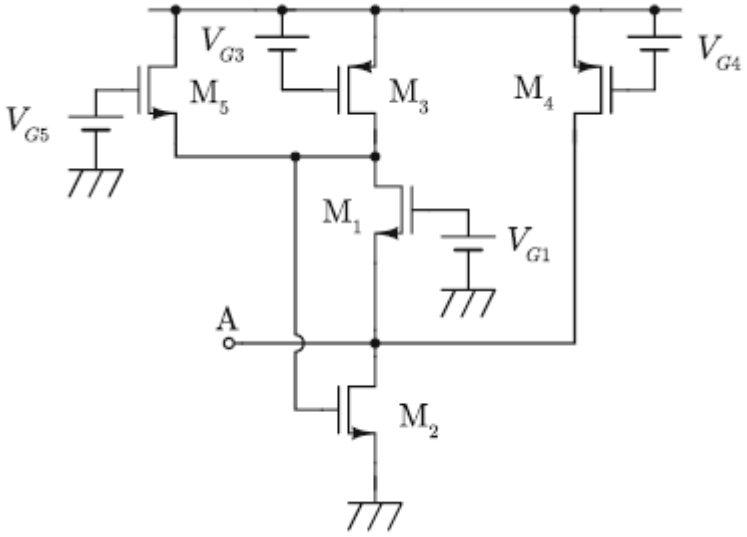


Figure: 5.3 proposed low distortion active inductor using M5.

Figure: 5.3 is a proposed low distortion active inductor derived from Figure: 5.1. A compensation current source M5 is inserted in parallel with a bias current source. The sum of gate-to-source voltage of M2 and M5 is kept constant since the source terminal of M5 is connected to the gate of M2.When a gate-to-source voltage of M2 is Vgs2 +vgs2, a gate-to-source voltage of M5 becomes Vgs5 =VG5- Vgs2- vgs2and the drain current of M5 acts as Ic. Insertion of M5 is simple and effective in improving linearity.

Chapter 6

SIMULATION RESULTS

To estimate the performance of the designed active inductor, it is simulated in cadence environment using 180nm CMOS technology. Periodic steady state analysis is performed to obtain the values of the two port parameters of the designed circuit. The Z-parameters have been used to calculate the inductance and the quality factor.

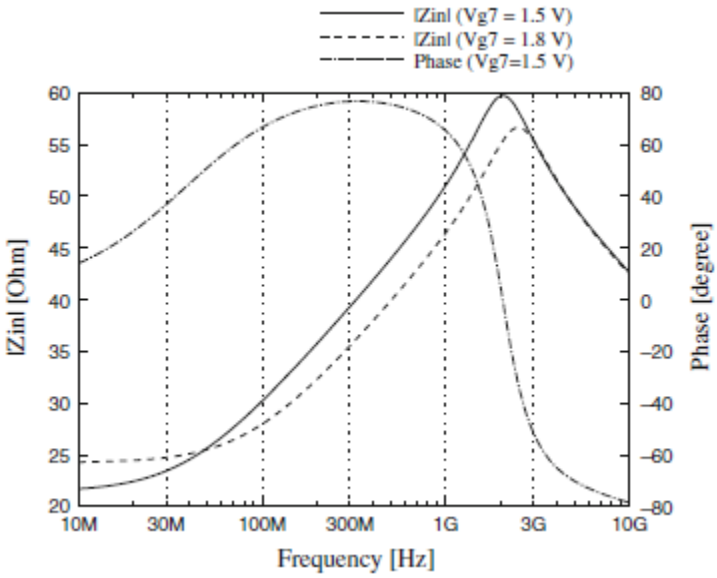


Figure: 6.1 Frequency characteristics of the active inductor

Frequency characteristics are shown in Figure: 6.1. The active inductor acts as an inductor from 70 MHz to about 1.1 GHz. Inductance of active inductor becomes about 21 nH. Figur: 6.1 also shows impedance controllability of the proposed design shown in Figure: 5.3.Even when the proposed distortion reduction technique is applied to the active inductor inductance of the active inductor can be controlled by Vg7. Its inductance is controlled from 19 to 21 nH.

Figure: 6.2 and Figure: 6.3 show the inductance and the Q-factor of the proposed Active inductor.

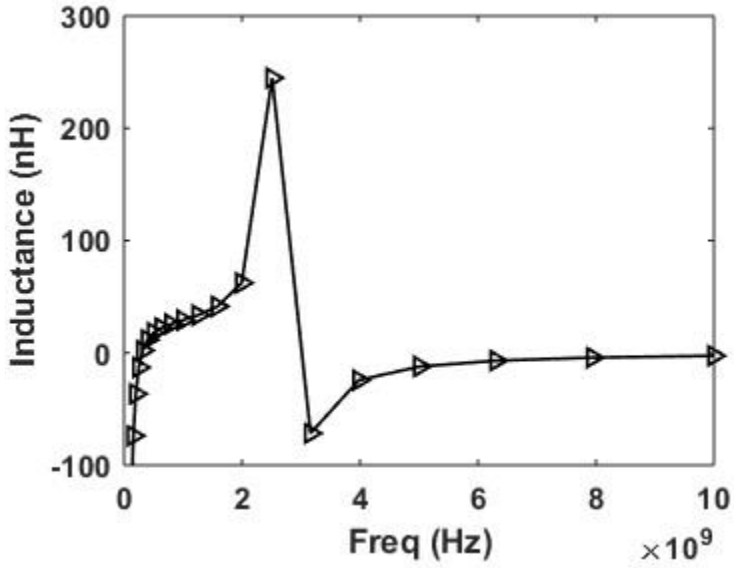


Figure: 6.2 Inductance versus frequency of the proposed circuit

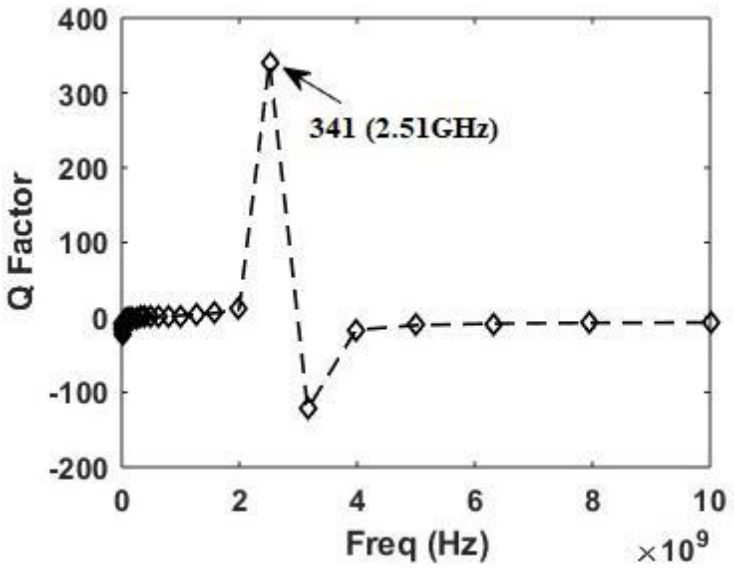


Figure: 6.3 The Q-factor plot of the proposed active inductor

Effects of the proposed distortion reduction technique are shown inFigure: 6.4. Total harmonic distortion (THD) of an active inductor using the proposed distortion reduction technique and that of Figure: 5.1 is shown in the same figure for the comparison. THD of Figure: 5.3 is much smaller than that of conventional one. THD of Figure: 5.3 also increase as input voltage becomes larger, however, it is kept below 5 % even when input voltage is 50 mV. On the other hand, THD of Figure: 5.1 increases rapidly.

When input voltage is 50 mV it becomes about 11 %. The proposed distortion reduction technique can reduce the distortion of input voltage drastically.

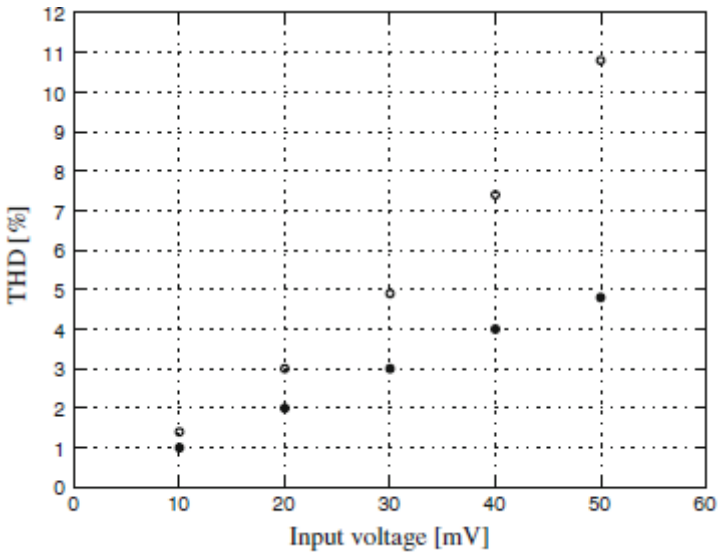


Figure: 6.4 THD of the proposed active inductor

Chapter 7

APPLICATION AND ADVANTAGES

An active inductor is widely used in the wireless communication and satellite communication systems. The scope for active inductor has increased rapidly in the recent times because of the increased usage of smartphones. Each smartphone will have a receiver which consists of a Low noise amplifier (LNA) which uses active inductor for a better performance. Highly linear Active inductors can improve the performance of VCOs as they are extensively used in the designing of the VCOs. An oscillator with low noise is implemented with the gyrator-C based active inductor which has a low output noise. The active inductor is also used High-quality-factor band pass filters for frequency selection and rejecting out of band interferers.

The active inductors are capable of working effectively in band pass filters at high frequencies and can be designed to achieve smaller chip area. The linearity of the active inductor plays a major role in the performance of band pass filters and the proposed linear design can hence improve the performance. Also compact and high-performance CMOS band-pass filter circuits can be designed for various RF devices. An active inductor has noise cancelling properties. These are used in the applications of RF components.

Chapter 8

CONCLUSION

This project work has proposed a distortion reduction technique for active inductors. A compensation current source is introduced to cancel out a distortion caused by nonlinearity of a MOSFET. The proposed technique requires only a few additional MOSFETs because a bias current source in the conventional active inductor can be used as a compensation current source. Low distortion active inductors based on a proposed technique have been introduced. Thanks to the proposed technique THD of the proposed low distortion active inductor becomes much smaller than that of conventional one. The proposed active inductors are applied to a second order bandpass filter and a VCO. The THD of the bandpass filter becomes 0.26 % at 1 GHz. This value is less than half of that of conventional one. The VCO using proposed active inductor outputs 950 MHz sinusoidal wave. It is confirmed that phase noise of the proposed VCO is improved by the proposed technique

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