Visvesvaraya Technological University, Belagavi.

PROJECT REPORT

on

"A NOVEL LEAKAGE REDUCTION TECHNIQUE FOR CMOS VLSI CIRCUITS"

Project Report submitted in partial fulfillment of the requirement for the award of the degree of

Bachelor of Engineering

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CERTIFICATE

This is to Certify that the dissertation work **"A novel leakage reduction technique for CMOS VLSI Circuits"** carried out by Student SATISH DOOGANAVAR, SHUBHAM KUMAR, ZABIULLA S, USN: 1CR16EC154, 1CR16EC163, 1CR16EC199, bonafide students of **CMRIT** in partial fulfillment for the award of **Bachelor of Engineering** in **Electronics and Communication Engineering** of the **Visvesvaraya Technological University, Belagavi,** during the academic year **2019-20**. It is certified that all corrections/suggestions indicated for internal assessment have been incorporated in the report deposited in the departmental library. The project report has been approved as it satisfies the academic requirements in respect of Project work prescribed for the said degree.

Signature of Guide	Signature of HOD	Signature of Principal
Guide1, Designation, Dept. of ECE., CMRIT, Bengaluru.	Dr. R. Elumalai Head of the Department, Dept. of ECE., CMRIT, Bengaluru.	Dr. Sanjay Jain Principal, CMRIT, Bengaluru.

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CHAPTER 1

INTRODUCTION

With recent advancements in semiconductor technology the density of transistors in Integrated Circuits is still growing, which in turn demands expensive cooling and packaging technologies. Keeping this in view, the supply voltages are scaled down for reducing the switching power dissipation. Moreover, the threshold voltage is also scaled down for the performance tradeoffs. However, the scaling of threshold voltage has resulted in exponential increase of subthreshold leakage current causing leakage (static) power dissipation. Static power dissipation is now growing considerably proportional to the switching dynamic power dissipation in deep submicron technologies and battery operated devices. The longer the battery lasts, the better the leakage power savings. Static power dissipation is mainly due to the leakage current components flowing in the CMOS transistor or CMOS circuits when there is no operation performed on it i.e.) during idle or standby mode. It is expected that the leakage power can increase 32 times per device by 2020.The four main sources of leakage current in a CMOS transistor are:

1. Reverse-biased junction leakage current
2. Gate induced drain leakage
3. Gate direct-tunnelling leakage and
4. Subthreshold (weak inversion) leakage current.

The subthreshold leakage current being the most predominant amongst all the leakage current sources becomes extremely challenging for research in current and future silicon technologies.

Power consumption of CMOS consists of dynamic and static component.

$$P_{Total}=P_{dynamic}+P_{shortcircuit}+P_{static} \qquad (1)$$

Dynamic power is consume when transistors are switching. Components of static power dissipation are junction leakage, sub-threshold leakage, gate oxide leakage.

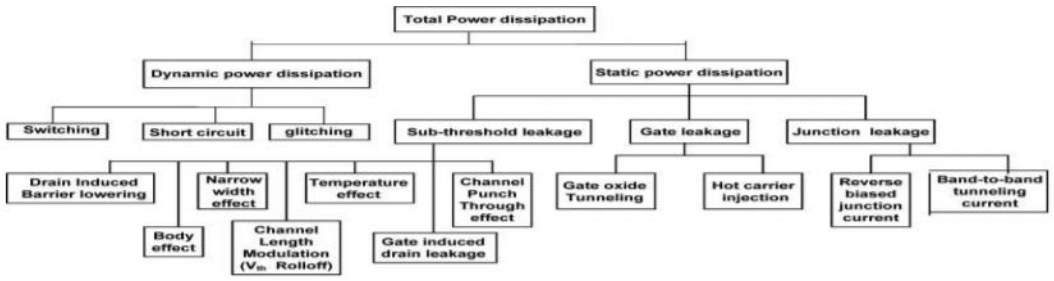

Figure 1.1:Types of Power Dissipation In VLSI Circuits

As the technology continue to scale down a significance portion of the total power consumption in high performance digital circuits is due to leakage current because of reduced threshold voltage and device geometry. Therefore leakage Power reduction becomes the key to a low power design. The leakage or static power dissipation is the power dissipated by the circuit when it is in standby mode and is given by (2)

$$P_{leak} = I_{leak} * V_{DD} \qquad (2)$$

Where is the leakage current that flows in a transistor in OFF state and VDD is the supply voltage. leakage current consist of various components.

Such as sub-threshold leakage, gate leakage, reverse– biased junction leakage, gate induced drain leakage, among these sub threshold leakage and gate leakage are dominant.Sub-threshold leakage current of a MOS device can be given as:

$$I_{ds} = I_{dso}\, e^{\frac{V_{gs} - V_t}{nvT}} [1 - e^{\frac{-V_{ds}}{V_T}}]$$

$$I_{dso} = \mu_{eff} c_{ox} (W / L) V_T^{\,2}$$

Where μ_{eff} is the charge carrier mobility, c_{ox} is the gate capacitance per unit area, W and L are width and length of channel respectively, V_t is the threshold voltage, V_T is the thermal voltage, n is the sub-threshold swing coefficient, V_{gs} is the transistor gate to source voltage and V_{ds} is the drain to source voltage.

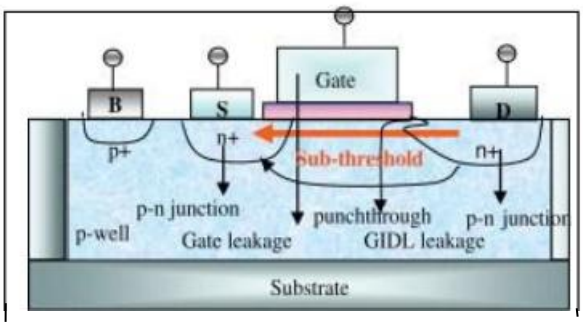

Figure 1.2:Static CMOS leakage sources

Leakage power of a CMOS transistor depends on gate length and oxide thickness. To decrease the dynamic power, the supply voltage is decreased which leads to the performance degradation. To speed up the device, the threshold voltage should also be scaled down along with the supply voltage, which results in exponential increase in the sub-threshold leakage current, thereby increase in the static power dissipation. The main components of leakage current in a MOS transistor are shown in Figure 1.2.

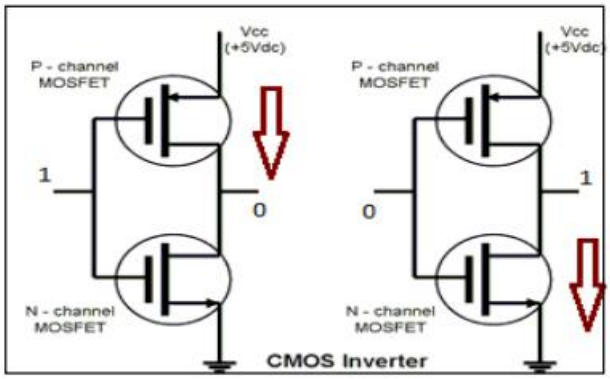

Figure 1.3:Reverse current in CMOS inverter

The leakage power in a CMOS is due to sub threshold leakage current; which is the reverse current flowing through the OFF transistor, indicated with arrows in Figure 1.3.

CHAPTER 2

SCOPE OF THE PROJECT

While implementing the circuits, the leakage current is considered to be neglected. So we are suppose to implement the CMOS circuits to reduce the leakage current in standby mode.

Techniques for leakage power reduction can be grouped into two categories:
(i) State-destructive techniques where the current boolean output value of the circuit might be lost and

(ii) State-saving techniques where circuit state is retained.

CHAPTER 3

LITERATURE SURVEY

Review of Mechanisms for Reducing Active Leakage In this section, we review the mechanisms behind mainstream active leakage reduction techniques whose influence on delay/leakage uncertainty we will expect in this work. The techniques considered include increasing gate length, Vdd/Vth optimization, body biasing, and stack forcing.

Increasing Gate Length

Since increasing the gate length not only reduces the leakage power but also reduces the leakage and delay uncertainties. Besides controlling the first order effect of variations, longer gate length also reduces the second order effect by lowering threshold roll-off and DIBL.

Vdd/Vth Optimization

Due to the strong dependence of both dynamic and leakage power on power supply voltage, lowering supply voltage is used in most low power designs. Meanwhile, as multi-threshold processes are increasingly common, power optimization through tuning supply voltage to threshold voltage ratio (Vdd/Vth) is used to achieve power-delay tradeoff.

Body Biasing

The body effect causes threshold voltage roll-off and in turn higher leakage power. By reverse biasing the substrate of a transistor in sleep mode, the leakage current can be reduced. For post-silicon optimization, body bias is used to tune the threshold voltage back to target value. - Stack Forcing The idea of “Stack Forcing” is to break a single transistor into a stacked transistor pair and thus the DIBL of the stacked transistor pair is reduced which in turn mitigates the leakage.

Leakage reduction techniques-a survey

There are various leakage power reduction techniques based on modes of operation of systems. The two operational modes are:

a) active mode and

b) standby (or) idle mode.

Most of the techniques aim at power reduction by shutting down the power supply to the system or circuit during standby mode.

3.1 Basic Gate Replacement Technique

Using basic gate replacement technique, the logic gate at worst leakage state (WLS) is replaced by another gate containing an extra sleep signal. When the circuit is in active mode i.e. SLEEP = 1, this condition exhibits the correct functionality of the circuit. On the other hand, when the circuit is in standby mode i.e. SLEEP = 0, this condition reduces leakage current of the replaced gate but may change the output of that gate. This replacement technique may affect the leakage of other gates too.

3.2 Modified Gate Replacement Technique

In modified technique, we can neglect the gates with higher fanout that leads to increase in overall leakage current. Using this technique, all the logic gates in a CMOS circuit are visited by topological order. The gates with lower leakage are skipped and gates at WLS are replaced. After each replacement, we will check the total leakage of the circuit that has to be reduced. Using the replacement, if the overall leakage of the logic circuit increases, it can be assumed that the output of replaced gate increases the leakage of other gates too. Therefore, we will skip the gate without any replacement.

3.3 State Destructive Technique

3.3.1 Multi-threshold CMOS

The multithreshold voltage CMOS circuit was proposed by inserting high threshold devices in series into low-Vth circuitry. Figure 3.1. shows the MTCMOS technique in which lower threshold voltage devices increases the performance of the circuit while the high threshold voltage sleep transistors decreases the standby current of the circuit. The power terminals of the standard design is not connected directly to the supply but to virtual Vdd and virtual Gnd. During the active mode sleep signal is off (sleepbar is on) and the circuit operates normally. During the standby mode, sleep signal is on (sleepbar is off)thus both the sleep control transistors are off the design is cut-off from the power supply. Since sleep transistors are high threshold voltage transistors, the leakage current is reduced.

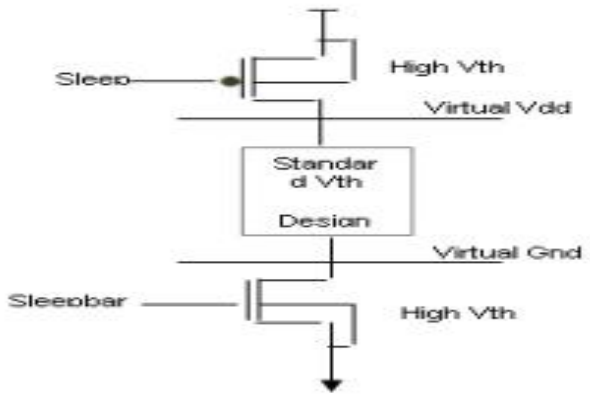

Figure 3.1:MTCMOS

3.3.2 Super-Cutoff CMOS

SCCMOS scheme is proposed to achieve high-speed and low stand-by current. By overdriving or under driving the gate of a cut-off MOSFET, the SCCMOS suppresses leakage current in a stand-by mode while high- speed operation in an active mode is possible with low-threshold voltage. Figure 3.2 shows the SSCMOS technique which is similar to MTCMOS instead of the low threshold voltage sleep transistors as compared to high threshold voltage sleep transistors in MTCMOS. The sleep (sleepbar) signal is overdriven or under driven to as to super cut-off the sleep transistors during standby mode thus reducing the leakage current. This has the advantage of have single threshold voltage devices in the design as compared to MTCMOS technique having two threshold voltages in the design. Circuit delay still increases due to the increased circuitry in the active mode.

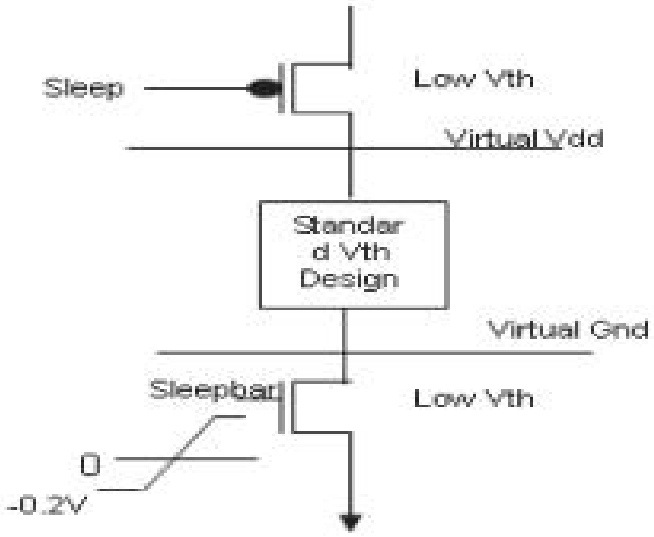

Figure 3.2:SSCMOS

3.3.3 Zigzag

The zigzag technique reduces the wake-up overhead of sleep transistors. This technique chooses a particular circuit state and then for that particular state, turning off the pull-down network for each gate whose output is high while turning-off the pull-up network for those gate whose output is low. Although the zigzag technique retains the particular state chosen prior to chip fabrication, any other arbitrary state chosen during regular operation is lost in power- down mode. Also, zigzag technique may need extra circuitry to generate a specific input vector. Figure 3.3 shows the zigzag technique. Input A is applied during standby mode due to which the output values are shown in figure. A pull-down sleep transistor is applied for output value '1' and a pull-up sleep transistor is applied for output value '0'.

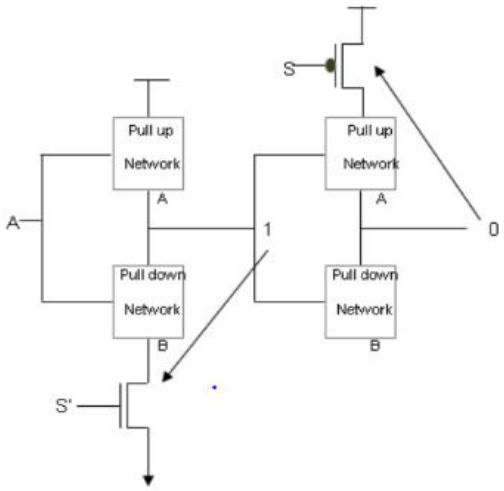

Figure 3.3:Zigzag Technique

3.3.4 Transistor Gating

This technique introduce PMOS sleep transistor between pull up network and pull down network while an NMOS sleep transistor between pull down network and ground. In Figure 3.4 during active mode, signal s is low (s' is high) turning on both the sleep transistors and normal operation of the circuit. During standby mode, signal s is high (s' is low) turning off both the sleep transistors creating a high impedance path from supply voltage to ground thus reducing the leakage power. When a full subtracter circuit is simulated in 45 nm CMOS technology, this technique reduces the leakage power by 24.38%.

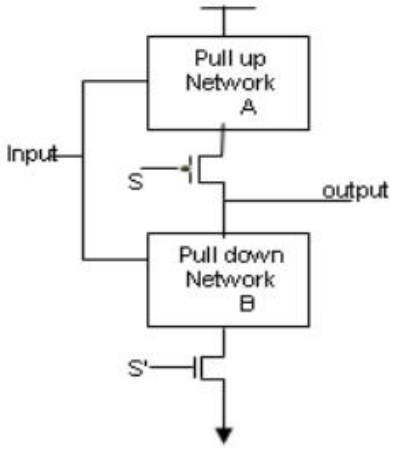

Figure 3.4: Transistor Gating

3.4 State-Preserving Technique

3.4.1 Transistor Stacking

Transistor Stacking: Stack effect is the phenomenon, where leakage current decreases due to two or more series transistors that are off. In some circuits Transistor Stacking already exist such as NAND gate. As the depth of the stack is increased, higher leakage power saving is observed. In some circuits, natural stacking does not exist and to utilize the stack effect force stacking is done by replacing a single transistor of width W by two transistors in series each of width W/2. Figure 3.5. shows the NMOS transistor stacking in CMOS inverter. Stack effect factor (X) is the ratio of leakage current in one off device to the leakage current in a stack of two or more off devices.

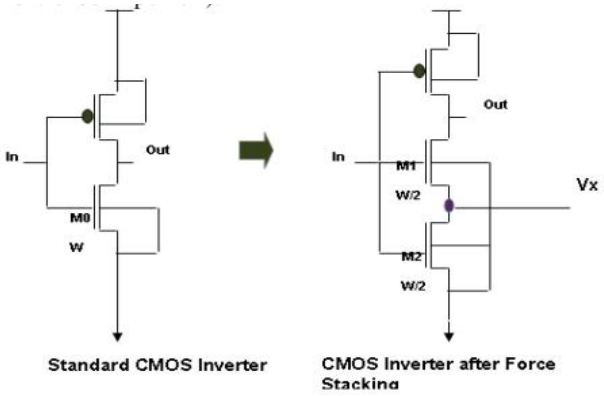

Figure 3.5:Transistor Stacking

3.4.2 Sleepy Keeper Approach

In this approach combination of PMOS and NMOS transistor which is connected paralleled inserted between pull up network and Vdd and pull down and GND, NMOS transistor of pull up sleep transistor connected PMOS pull down sleep transistor This approach reduces the leakage power efficiently and maintains the proper logic of the circuit with lesser area.

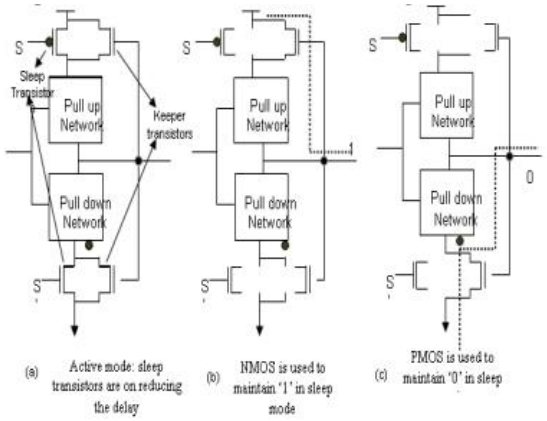

Figure 3.6:Working of Sleepy Keeper

3.4.3 Sleepy Stack

The sleepy stack technique has a combined structure of forced stack technique and sleep transistor technique. However, unlike sleep transistor technique, the sleepy stack technique retains exact logic state and unlike the forced stack technique, the sleepy stack technique can utilize high-Vth transistors without delay penalties. In order to use sleepy stack technique, for example in standard CMOS inverter (Figure 3.7.), first force stacking technique is applied by replacing the transistor with two or more series transistors. Then, sleep transistor is added in parallel to one of the stacked transistors. Figure 8. shows the working of sleepy stack circuit during active mode and during standby mode of operation. During the active mode, sleep transistors are on (sleep signal S='0'), thereby reducing the resistance of the path due to the presence of two parallel transistors. Thus the propagation delay is reduced during the active mode. During the stand-by mode (sleep signal S='1'), sleep transistors are off and the leakage is suppressed due to the transistor stacking effect as explained previously. The main disadvantage of this approach is that each transistor in the original is replaced by three transistors in the sleepy stack equivalent.

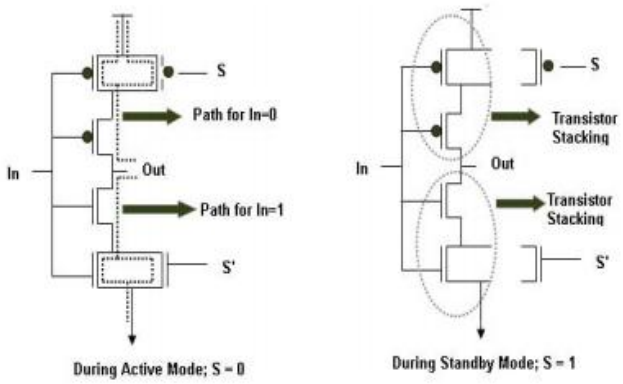

Figure 3.7:Working of Sleepy Stack

CHAPTER 4

PROPOSED TECHNIQUE

4.1 LECTOR

This technique is based on the observation that "a state with more than one transistor off in a path from supply voltage to ground is far less leaky than a state with only one transistor off in any supply to ground path". So, in order to ensure that there are more than one off transistors in the path of supply voltage and ground, Leakage Control Transistors (LCTs) are included in the path of supply voltage and ground as shown in Figure 4.1.

The gate of PMOS LCT is connected to the drain of pull down network while the gate of NMOS LCT is connected to the drain of the pull up network. With this wiring, with any input combination during standby mode one of the two LCTs is always near its cut-off region. This increases the resistance of the path from supply voltage to ground thus reducing the leakage power.

LECTOR technique of reducing the leakage power adds an extra circuitry as compared to the conventional design which reduces the performance of the circuit. Thus the sizing of the LCTs have to be done optimally so as to meet the performance.

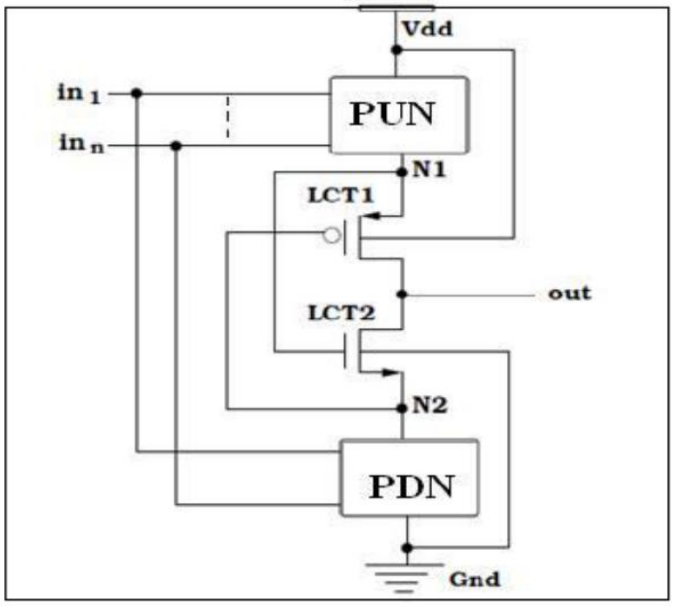

Figure 4.1: Lector Technique

In this method, two leakage control transistors are positioned in between the pull-up and pull-down network, this implies either one of the LCTs will continuously drives in its near cut-off region, this arrangement is shown in Figure 4.1.Between two nodes N1 and N2, LCT's are introduced. The gate of the LCT's is controlled by the source of the other. Since LCTs are self-controlled there is no need of external circuit.

CHAPTER 5

SIMULATION RESULTS AND SIMULATION

The CMOS inverter without and with LECTOR is shown in Figure 5.1 and Figure 5.2 respectively.

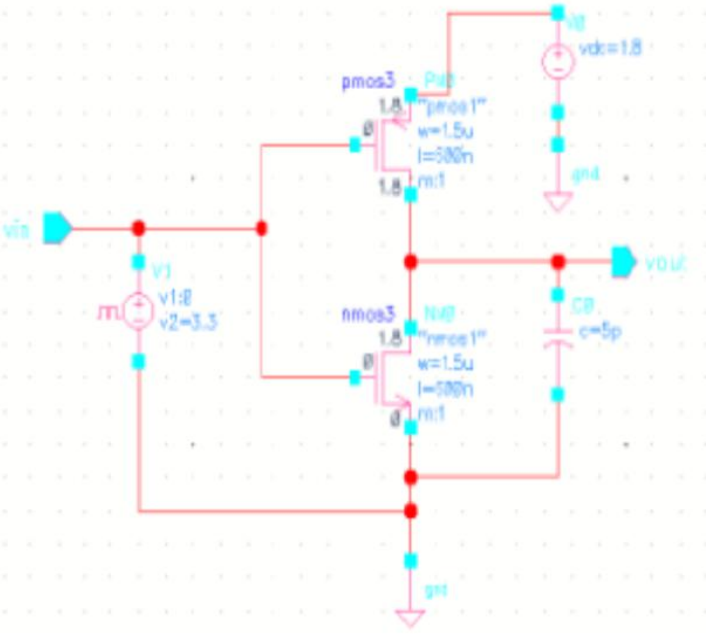

Figure 5.1:CMOS inverter without LECTOR

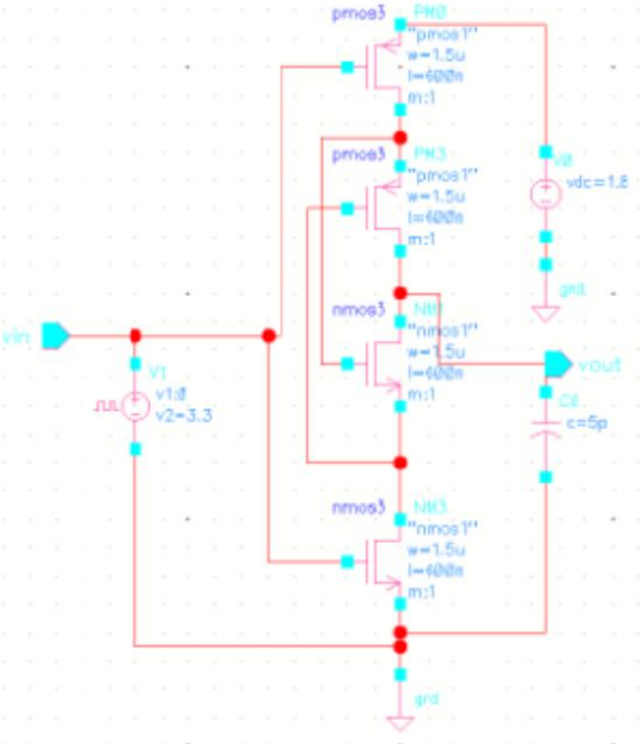

Figure 5.2:CMOS inverter with LECTOR

The simulation waveform for CMOS inverter with and without LECTOR is shown in the Figure 5.3 and Figure 5.4 respectively.

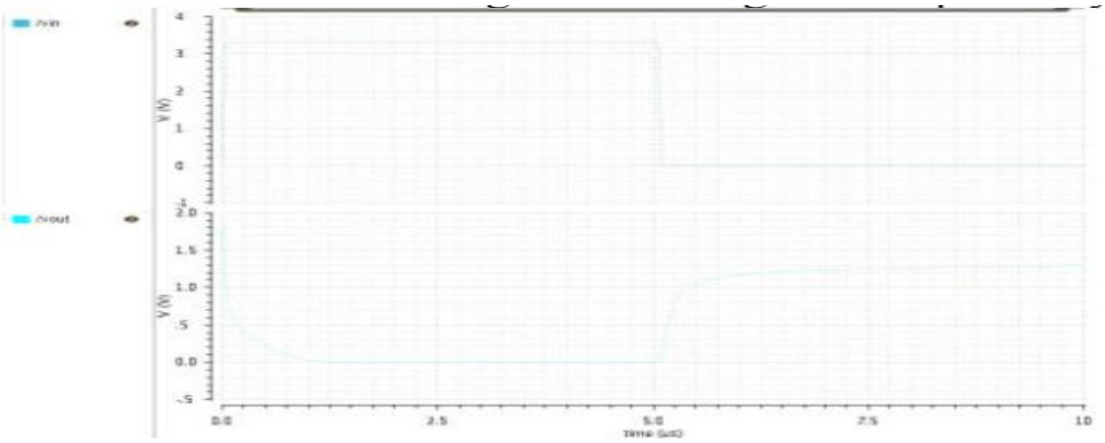

Figure 5.3: Waveform of CMOS inverter without LECTOR

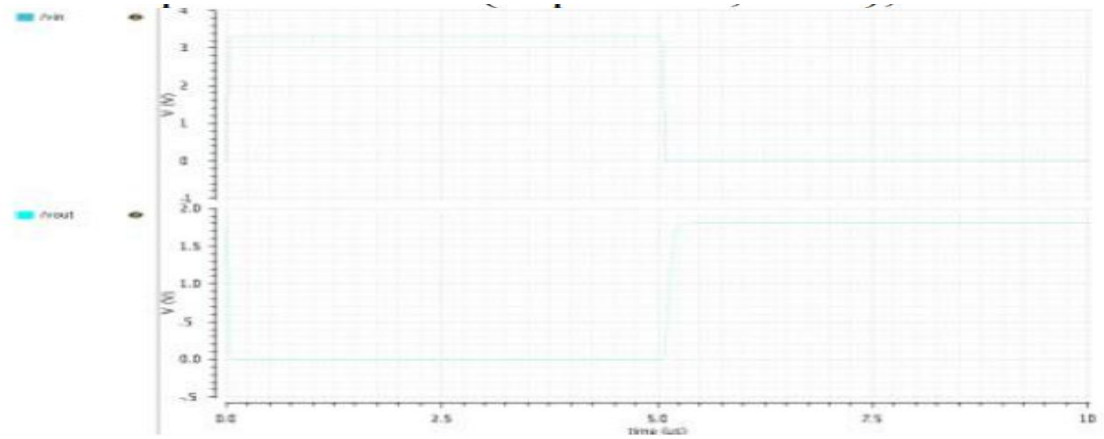

Figure 5.4: Waveform of CMOS inverter with LECTOR

The results show an average reduction of 79.4% in average leakage power dissipation with an average area overhead of 14%.

CHAPTER 6

CONCLUSION

Leakage reduction technique plays a key role in VLSI circuit design. Scaling down the appropriate parameter can reduce the leakage power. It can be concluded that there is a strong correlation between three performance parameters: leakage power, delay, power delay product.

Using the LECTOR method and modifying it with further transisters and reducing the leakage current in order to reduce the massive static power dissipation.

The leakage power reduction plays a key role in low power VLSI circuit designs. The scaling down of several device parameters and supply parameters for improving the performance of VLSI systems has contributed more to the increase in leakage power dissipation.

The present study provides an appropriate choice for leakage power minimization technique for a specific application by a VLSI circuit designer based on sequential analytical approach.

It can be concluded that the important performance parameters such as dynamic power, leakage power, propagation delay and the PDP are strongly inter related.

LECTOR technique founds to be more effective in both active mode and standby mode of operation. LECTOR technique is suitable for faster circuit operation, if propagation delay is the main criteria.

REFERENCES

[1] Dadoria AK, Khare K, Gupta TK, Khare N. Integrating sleep and pass transistor logic for leakage power reduction in FinFET circuits. J Comput Electron. 2017;16(3):867-874.

[2] Dadoria AK, Kavita K, Gupta TK, Singh RP. Ultra low power FinFET based domino circuits. Int J Electron. 2017;104(6):1-16.

[3] Dadoria AK, Khare K, Singh RP. Sleepy lector: a novel approach for leakage reduction in DSM technology. In Proc. of IEEE Confluence 2016, Amity University Noida, INDIA. January 13 -14, 2016.

[4] Varsha Bendre, Dr. A. K. Kureshi, "An Overview Of Various Leakage Power Reduction Techniques in Deep Submicron Technologies", International Conference on Computing Communication Control and Automation, 2015.

[5] Panwar U, Khare K. Gate replacement with PMOS stacking for leakage reduction in VLSI circuits. Int J Numer Modell: Electron Networks, Devices Fields. 2016;29(4):565-576.