Visvesvaraya Technological University, Belagavi

PROJECT REPORT

on

"FLASH ADC FOR LOW POWER APPLICATIONS"

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CERTIFICATE

This is to Certify that the dissertation work "FLASH ADC FOR LOW POWER APPLICATIONS" carried out by Niharika Kodiganti, Pallavi S Bhat, Priya M, Ranjitha P USN: 1CR16EC098, 1CR16EC103, 1CR16EC117, 1CR16EC128 respectively are bonafide students of CMRIT in partial fulfillment for the award of Bachelor of Engineering in Electronics and Communication Engineering of the Visvesvaraya Technological University, Belagavi**,** during the academic year 2019-20. It is certified that all corrections/suggestions indicated for internal assessment have been incorporated in the report deposited in the departmental library. The project report has been approved as it satisfies the academic requirements in respect of Project work prescribed for the said degree.

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ABSTRACT

ADCs are the key design blocks and are currently adopted in many applications to improve digital systems, which achieve superior performance with respect to analog solutions. Flash ADC has lot of applications in real time systems and mixed signal systems, where analog signals are converted to digital signals and then processed. The need for a high speed and low power ADC is very essential for various applications. Flash ADCs are always the architecture choice where maximum sample rate and moderate resolution is needed. Even though flash ADC is the fastest type available it takes enormous amount of IC's to implement.

In the present work, a new high performance Flash ADC is designed which employs fast processing encoder and low power comparator without kickback noise supporting low-power applications.

This design is simulated using 180nm technology in EDA Tanner tool. Simulation results are tabulated and analysis has been done.

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CHAPTER 1

INTRODUCTION

1.1 VLSI TECHNOLOGY

In modern technology Very Large Scale Integrated architecture has become a big driving force. It provides the basis for computing and telecommunications, and the sector continues to expand at an unprecedented rate. VLSI architecture is a resource-intensive discipline in engineering. Definitions of the project and the commodity are economically driven, and rivalry is very intense worldwide. The market potential for innovative designs is very diverse, but due to competitions and changing consumer demands the market is often short.

Current silicon-integrated circuitry's microscopic dimensions allow the design of digital circuits, which could be very complex and yet extremely economical in space, power requirements and cost, and potentially very fast. The aspects of space power and cost have made silicon the dominant manufacturing technology for electronics in wide range of application areas. The combination of complexity and speed is the finding of ready applications for VLSI systems in digital processing and especially in those areas of application requiring sophisticated high-speed digital computation.

1.2 VLSI Design Parameters

Power dissipation has become a crucial parameter in low power VLSI circuit designs due to widespread deployment of portable electronic devices and assessment of microelectronic technologies. In emerging VLSI technology, the **complexity** and **high speed** of the circuit imply significant increase in power consumption.

In low-power CMOS VLSI circuits, energy dissipation is triggered by charging and discharging internal node capacitors due to transfer operation, which is one of the major factors often influencing the dynamic dissipation of power. Reducing power, area and improving speed require optimization at all levels of design procedures.

Two opposing limitations in VLSI architecture are limited area and high performance. The activities of the Integrated Circuit (IC) designers were involved in the trading of those constraints. There are many possible design considerations which have made the power efficiency significant.

Minimizing a device's supply voltage is one of the best strategies for reducing the power dissipation. The trade-off of this strategy is that, as VDD reaches the threshold voltage, delay can increase considerably. So to mitigate this problem, the devices must be properly scaled. Scaling has the advantages of:

- Improve the device characteristics
- Reduce the geometric and junction capacitances
- Enhanced interconnect technology
- High density of integration

1.3 Basic MOS Transistor

MOSFETs are high input impedance devices that are tri-terminal, unipolar, voltage-controlled and form an integral part of a wide variety of electronic circuits. These devices may be divided into two categories, depletion-type and enhancement-type, based on whether or not they have a channel in their default state. Furthermore, each of them can be either p-channel or n-channel devices because of holes or electrons respectively, as they can have their conduction current. All of them have nearly similar characteristic curves but for different voltage values.

A MOS transistor is considered a majority carrier unit, where a voltage applied to the gate modulates the current in a conducting channel (the area directly underneath the gate) between the source and the drain. MOS transistors conduct electrical current by transferring the charge from the source side to the drain side of the device using the applied voltage. The majority carriers of an nMOS transistor are Electrons and that of a pMOS transistor are Holes.

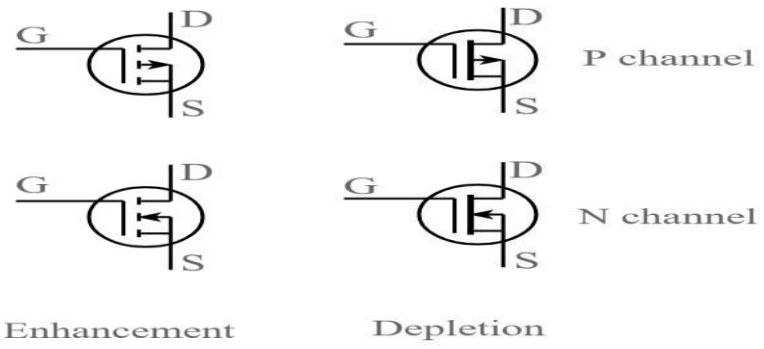


Figure 1.1: Circuit symbol for MOS transistor

The Four modes of transistors-

1. Enhancement mode nMOS transistor:
   - Vtn > 0
   - If Vgs > Vtn, the transistor starts to conduct. The number of electrons in the channel increases so that Idsn increases accordingly.
   - If Vgs < Vtn, the transistor is cut off and Ids is almost zero.
2. Depletion mode nMOS transistor:
   - Vtn < 0 (in the textbook it is referred as -Vtn and Vtn > 0)
   - Even if Vgs = 0 > Vtn, the transistor is “on”.
   - If Vgs < Vtn < 0, the transistor is cut off.
3. Enhancement mode pMOS transistor:
   - Vtp < 0 (in the textbook it is referred as -Vtp and Vtp > 0)
   - If Vgs < Vtp < 0, the transistor starts to conduct. The number of holes in the channel increases so that Idsp increases accordingly.
   - If Vgs > Vtp, the transistor is cut off.
4. Depletion mode pMOS transistor:
   - Vtp > 0
   - Even if Vgs = 0 < Vtp, the transistor is “on”.
   - If Vgs > Vtp > 0, the transistor is cut off.

1.3.1 Working of MOSFET

MOSFET is seen to exhibit three operating regions-

1. CUT-OFF Region

   Cutoff area is a region where the MOSFET is going to be OFF, because there is no current flow into it. In this region, MOSFET behaves as an open switch and is thus used to operate as electronic switch when required.

2. Linear Region

   Ohmic or linear region is an area where the current IDS decrease with a change in VDS value. When MOSFETs are designed to work in this region, they can be used as amplifiers.

3. Saturation Region

In the saturation region, despite an increase in VDS, the MOSFETs have their IDS constant, and occur once VDS exceeds the pinch-off voltage VP value. Under this condition the device will operate as a closed switch with a saturated IDS value flowing through it. As a result, this area of service is chosen if MOSFETs are needed to perform switching operations.

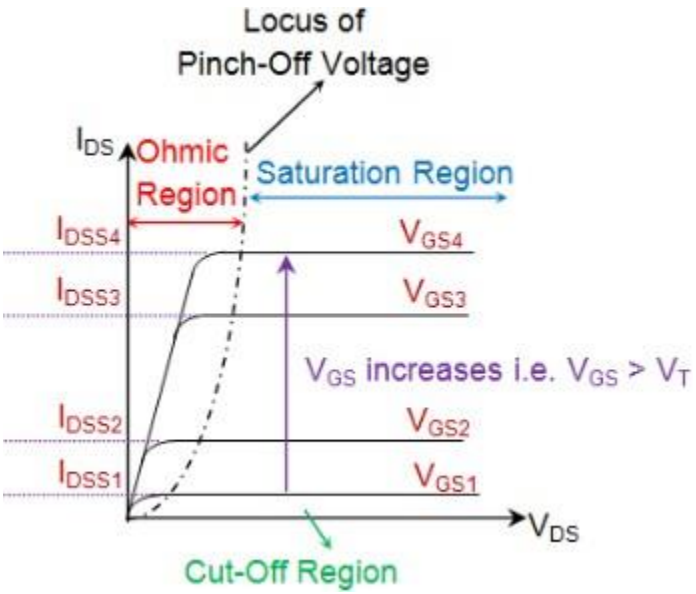


Figure 1.2: Output Characteristics of MOSFET

Kind of MOSFET	Region of Operation		
	Cut-Off	**Ohmic/Linear**	**Saturation**
n-channel Enhancement-type	$V_{GS} < V_T$	$V_{GS} > V_T$ and $V_{DS} < V_P$	$V_{GS} > V_T$ and $V_{DS} > V_P$
p-channel Enhancement-type	$V_{GS} > -V_T$	$V_{GS} < -V_T$ and $V_{DS} > -V_P$	$V_{GS} < -V_T$ and $V_{DS} < -V_P$
n-channel Depletion-type	$V_{GS} < -V_T$	$V_{GS} > -V_T$ and $V_{DS} < V_P$	$V_{GS} > -V_T$ and $V_{DS} > V_P$
p-channel Depletion-type	$V_{GS} > V_T$	$V_{GS} < V_T$ and $V_{DS} > -V_P$	$V_{GS} < V_T$ and $V_{DS} < -V_P$

Table 1.1: Regions of Operations of MOSFETs

1.4 Introduction to ADC

The development in field of digital signal processor field is rapid because of the advancement in the integrated circuit technology over the recent decade. Besides, advantage of digital processing is that it is more resistant to noise. Hence analog to digital converter plays a crucial role in between analog and digital signal processing system. The continuous performance improvement of the wireless communication systems has resulted in huge demands in speed and power specifications of high-speed analog to digital converter.

An analog to digital converter is a system being used to convert analog signals from real world signals such as voltage, temperature, speed, pressure, light etc. into digital values like 0's and 1's. This is an integrated electronic circuit that directly converts the continuous signal to discrete form. It can be represented in either A/D or A-to-D or A-D or ADC. The analog input to this device can have any value in a range and are directly measured. But for digital output of an N-bit analog to digital converter, it should have 2^N discrete values. Most of ADCs take a voltage input as 0 to 10V, -5V to +5V, etc. and generates digital output as some sort of a binary number accordingly. One of the significant advantages of ADC converter is high information procurement rate even at multiplexed inputs.

1.5 Analog to Digital Conversion Techniques

Analog to digital converter samples the analog signal at each falling or rising edge of sample clock, in each cycle, the ADC receives analog signal, analyses it and converts it into a digital value. The ADC transforms the output data into set of digital values by having the signal approximate with defined precision. Two factors determine the precision of the digital value that captures the original analog signal. These are quantization level and sampling rate.

The process of analog to digital conversion involves two phases.

1. Sampling and Holding
2. Quantizing and Encoding

1.5.1 Sampling and holding:

- Sampling theorem / Nyquist's theorem-

The theorem, developed by H. Nyquist, which states that an analog signal waveform may be uniquely reconstructed, without error, from samples taken at equal time intervals. The sampling rate must be equal to, or greater than, twice the highest frequency component in the analog signal.

$$\text{Nyquist rate, } f_s = 2*f_m$$

Sampling generally is done with a Sample-And-Hold circuit. In order to be able to reconstruct the signal we must consider the sampling theorem which states that a sampling frequency is twice the highest frequency we are expecting is needed. sampling can be defined in simple way as the process of taking samples from the continuous time function x(t) and in order to reconstruct the signal we must consider the sampling theorem which states that the sampling frequency must be always higher than or equal to twice the highest frequency.

In the process of Sample and hold (S/H), the continuous signal is sampled and value is frozen for a specific minimum period of time at steady level. It is done to remove input signal variations that can alter the conversion process and thus increases the accuracy. The minimum sampling rate must be maintained as defined by sampling theorem called as Nyquist rate.

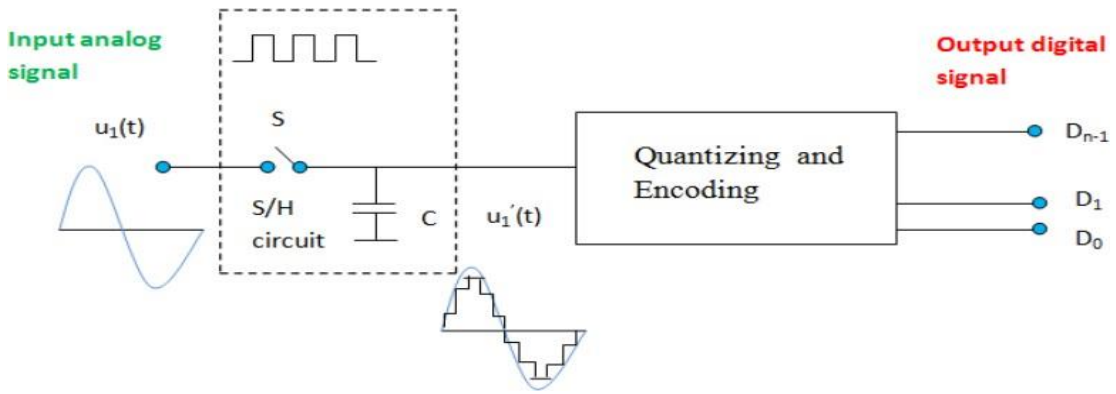


Figure 1.3: Sampling and Holding Process

1.5.2 Quantization and encoding:

Quantization is the mechanism whereby a continuous voltage signal is taken and mapped to a discrete number of voltage levels. The number of voltage levels influences

the noise that occurs in quantization. Since digital computers are binary in nature, the number of quantization levels is a power of 2, i.e.

$$N = 2^n$$

Where n is the number of quantization bits.

Until reaching ADC, the signal may be amplified or attenuated so that the maximum and minimum voltage levels provide the best compromise between resolution of the signal levels and clipping minimization.

Encoding is the process of converting the quantized signals into a digital representation. This encoding is performed by giving each quantization level a unique label. For instance, if four bits are used, the lowest level may be (in binary) 0000, and the next highest level 0001, etc.

1.6 Introduction to FLASH ADC

While comparing with other ADCs Flash ADC is the fastest type available that is used in wireless communication, radar detection, and ultra-wideband receivers. Flash ADC is often known as parallel ADC and is the fastest ADC which is an analog to digital converter that uses a linear voltage ladder with comparators to match the input voltage to successive reference voltages. The conversion is performed simultaneously through the series of comparators. In general, the output of these comparators is fed into a digital encoder which converts the input into a binary value. Flash ADCs are suitable for applications requiring very wide bandwidth, but they use more power and much bigger in size than other ADC architectures.

A Flash ADC needs a huge number of comparators compared to other ADCs, particularly as the resolution increases. A Flash converter needs $\mathbf{2^N-1}$ comparators and $\mathbf{2^N}$ resistors for an N-bit conversion. The resistors supplying the reference voltage for each comparator are one least significant bit (LSB) greater than the reference voltage for the comparator immediately below it. Each comparator produces outputs value 1 when its analog input voltage is greater than the reference voltage applied to it. Otherwise, the comparator output is 0.

The output of the comparators is known as thermometer code. This name is used because the design of mercury thermometer is similar in nature. The thermometer code is then decoded to appropriate digital output code using an encoder.

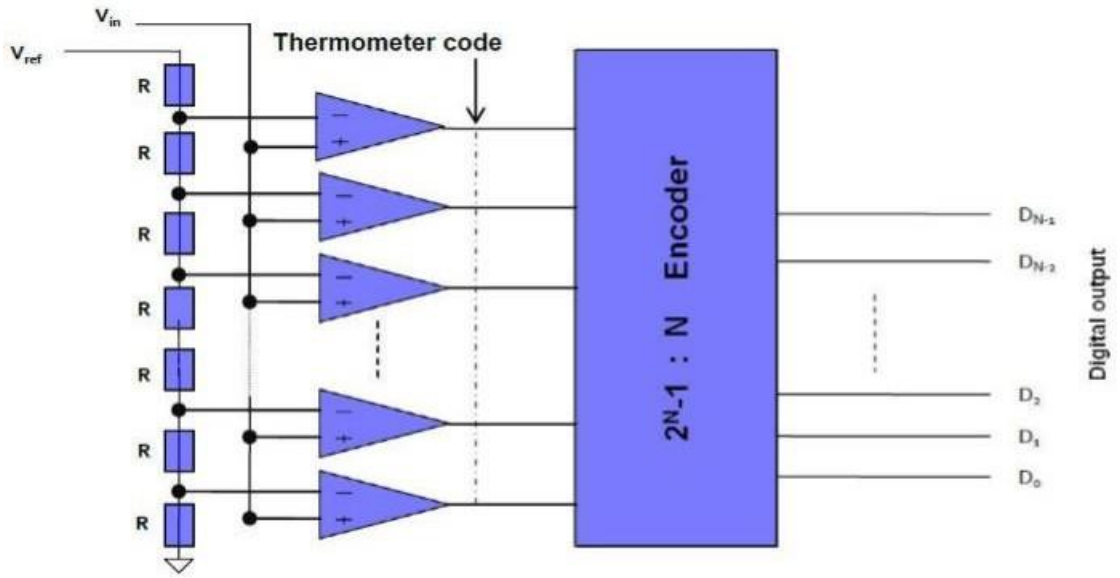


Figure 1.4: Typical Flash ADC block diagram

1.7 Objective

Flash ADC is one of the most preferred architectures for high speed analog-to-digital data conversion applications. The comparator is a building block of all analog-to-digital converter architecture. The kickback noise in the comparator is one of the important factor which leads to power dissipation.

Hence the objective of the project is to design and implement a 4 bit Flash ADC by using effective comparator which reduces the kick back noise. Kickback noise is the disturbance caused due to large voltage variations in the regenerative phase of the comparator at the input.

Reduction of the kickback noise makes it possible to drive the ADC with higher impedance, which in turn reduces the power dissipation. Here the designs of different types of comparators are analyzed. Comparator without kickback noise is proposed for the Flash ADC due its less power consumption. The proposed ADC offers a low-power solution with reduced Kickback noise.

This design is simulated and analyzed in 180nm technology in EDA Tanner tool. Simulation results are tabulated and analysis has been done.

CHAPTER 2

LITERATURE SURVEY

In [1] overcoming of Flash ADC's wide area and power dissipation was inferred by reducing the number of comparators by utilizing multiplexers. Here the reference voltages were produced by the multiplexers. When it is operated at 1.2 V, the circuit shows a power dissipation of 23 m W and can provide maximum sampling frequency of 2 GS/s. This work is used for wireless application. It can also be used in portable ECG systems.

In [2] a Flash ADC was designed using 180nm technology that uses four low power consumption comparators. The reference voltages are selected through the multiplexers from the diode connected transistor-voltage divider network and fed to the comparators. Power dissipation of 1.19mW is achieved in the circuit for 4-bit conversion.

[3] Presented a Flash ADC designed in 0.18um using CMOS technology. It consumes 42mW with supply voltage of 1.8V. Chip area of this type of Flash ADC is lowered as fewer components and interconnectors are used. It was designed for UWB applications.

[4] This Flash ADC uses multiplexer based encoder developed using 90nm CMOS technology. The average power consumption obtained was 17.5uW for 1MHz input frequency.

In [5] the author introduced the traditional comparator which is replaced by an open loop comparator and the non-ROM type encoder is used as an alternative for the conventional encoder. The proposed method can increase up until 500MHz of sampling frequency in the proposed Flash ADC with 1.8V power supply.

[6] Presented Flash ADC architecture using a dynamic comparator and encoder block using 2:1 MUX. The propagation delay obtained in conventional is 8.5584ns which was further reduced to 3.9151ns in proposed comparator.

[7] Presents analysis of a competent low power thermometer code to binary code converter. The first stage of encoder is designed using dynamic logic and the second stage by Wallace tree style.

[8] A progressive study of VLSI and MOSFETs from the textbook “Basic VLSI design”.

[9] Presented the study of various types of encoders suitable for process, few among them are discussed in later chapters.

CHAPTER 3

ARCHITECTURE

3.1 Architecture OF FLASH ADC

As known from section 1.6 the architecture of Flash ADC consists of primarily three blocks i.e., resistor ladder, comparators and thermometer code to binary code converter which is an encoder. These blocks are integrated together to obtain the functionality of 4-bit Flash ADC. The high speed 4 bit Flash ADC is designed and simulated in Tanner software. In this chapter, we shall discuss these blocks individually.

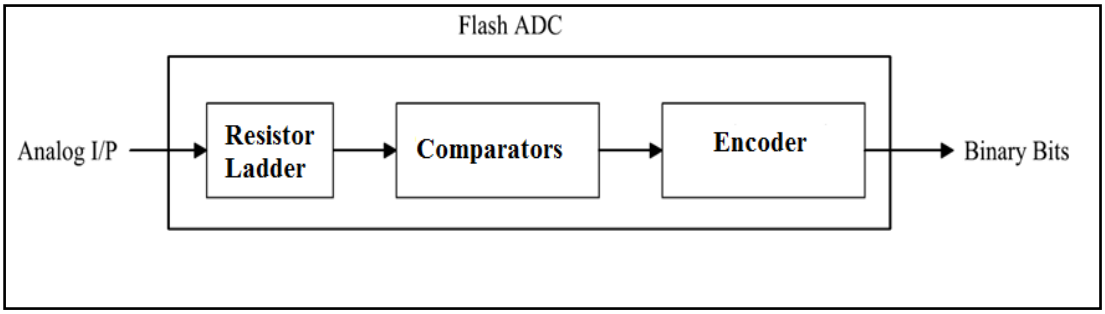


Figure 3.1: Components of Flash ADC

3.1.1 Resistor Ladder

The resistor ladder is primarily designed to provide a stable reference voltage to the comparators. The resistor ladder network consists of 2N resistors which generates the reference voltage to the each comparator. The reference voltage for all comparator is one least significant bit (LSB) less than the reference voltage for the comparator immediately above it. The ladder divides main reference voltage into 2N equally spaced voltages using the voltage divider formulae.

$V_n = [n*R / (R+ (2^N-1*R))]*V_{ref}$

Where,

N = resolution of Flash ADC, here 4

V_n = is the voltage at each comparator input

V_{ref} = reference voltage

R = resistance of 1KΩ

V_{in} = input analog voltage

Therefore, for n=1 and 4 bit resolution reference voltage at the point V_1 is given as

$V_1 = [R/16R]*V_{ref}$

.

.

.

$V_{15} = [15*R/16R]*V_{ref}$

Similarly, the main reference voltage is divided using the resistors to each comparator's input node. This voltage V_n is then compared to the input voltage V_{in} by the comparator.

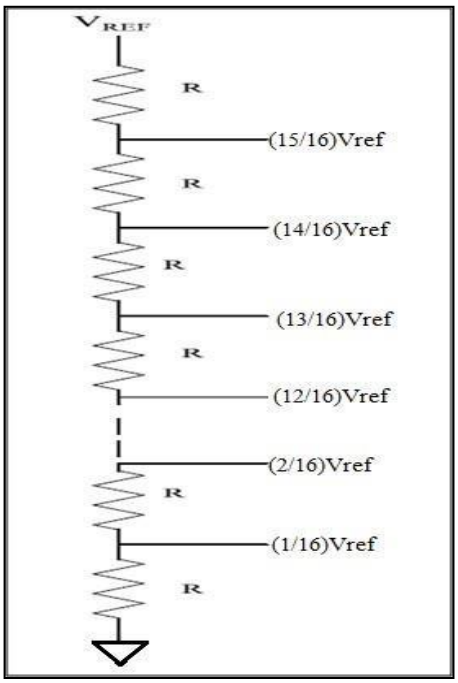


Figure 3.2 Resistor ladder

3.1.2 Comparator

The most significant portion of ADC architecture is comparator. It is used to compare two voltages or currents which are provided at the two inputs of the comparator. That means it takes two input voltages, then compares them and gives either high or low-level signal for differential output voltage. When an arbitrary varying input signal exceeds the reference level or a given threshold level, the comparator senses it. The comparator can be constructed by using different components like diode, transistors or operational amplifiers.

The comparator has analog **inverting (V_-) and non-inverting (V_+)** input terminals and one binary digital output V_{out}.

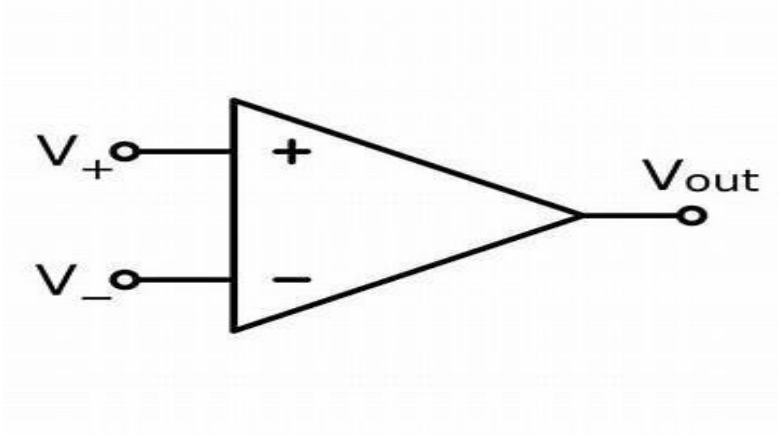


Figure 3.3: comparator symbol

$$V_0 = \begin{cases} 1, & \text{if } V_+ > V_- \\ 0, & \text{if } V_+ < V_- \end{cases}$$

Here, the *input voltage* is given to the non inverting terminal and *reference voltage* to the inverting terminal of the comparator. The comparator compares the input voltage signal (V_{in}) with the reference voltage (V_{ref}) generated by the resistor ladder and produces the corresponding high or low binary voltage at the output terminal.

Since the circuit has 15 (2^4 -1) comparators in parallel, we get 15 output bits at this stage which is called as **thermometer code**.

A comparator consists of a specialized differential amplifier for high gain. They are commonly used in devices which measure and digitize analog signals, such as analog to digital converters. It can be regarded as a circuit for decision making because it makes a decision based on the value of input signal and reference signal.

In General comparators are categorized into open loop and regenerative comparators. Open loop comparators are op-amps without feedback. Regenerative comparators utilize positive feedback mechanism to carry out comparator operation.

Various Comparators are designed and their performances are compared in the upcoming chapters.

3.1.3 Encoder

Output code of a decoder typically has more bits than its input code. If the output code of the device has fewer bits than the input code, it is commonly called an encoder. Thus an encoder plays the opposite function to that of a decoder. The given information is encoded in a more compact form. Binary encoders and Priority Encoders are the most widely used encoders.

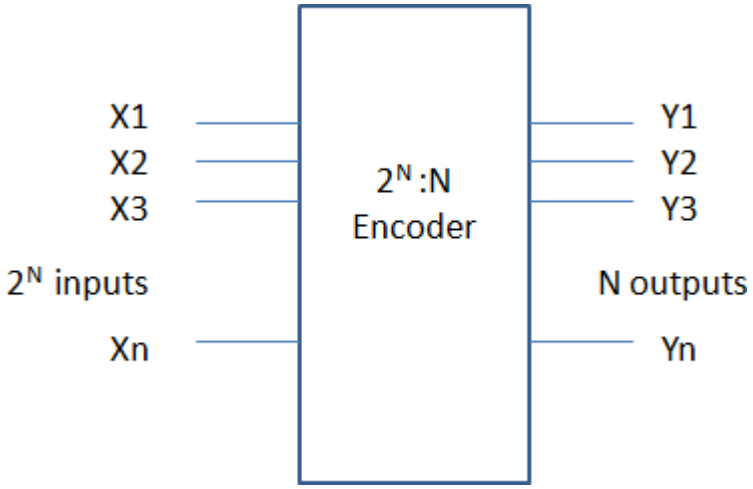
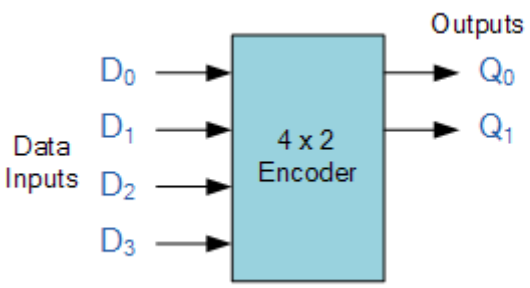


Figure 3.4: Block diagram of Encoder

3.1.3.1 Binary Encoders

A Binary Encoder takes all of its data inputs one at a time and then transforms it to a single encoded byte. So we can assume that a binary encoder is a combinational multi-input logic circuit that at its output transforms the logic level "1" data to an analogous binary code. Based on the number of data input lines, digital encoders typically produce outputs of 2-bit, 3-bit, or 4-bit codes. An "n-bit" binary encoder has 2n input lines and n-bit output lines of popular forms that include combinations of 4-to-2, 8-to-3, and 16-to-4.



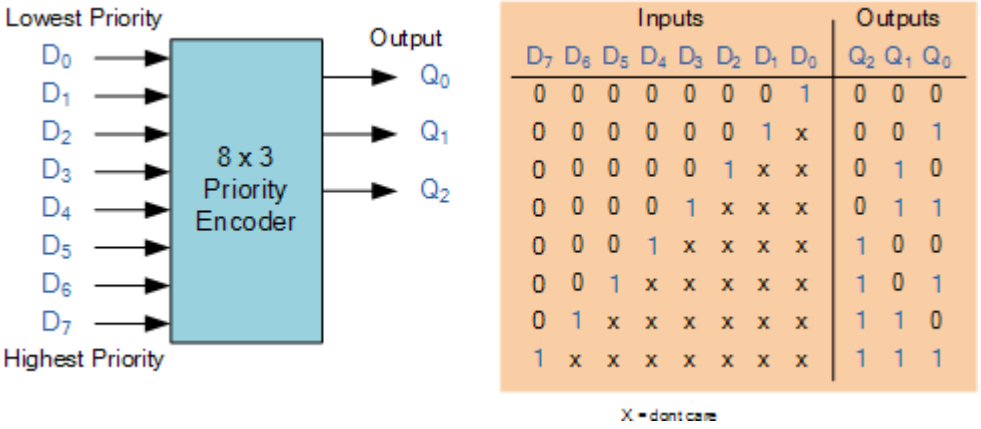
Inputs				Outputs	
D_3	D_2	D_1	D_0	Q_1	Q_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1
0	0	0	0	x	x

Figure 3.5: 4-to-2 Encoder block diagram and truth table

One of the main drawbacks of standard digital encoders is that they can generate the incorrect output code when there is more than one input of logic level "1". One easy way to solve this problem is by "prioritizing" the degree of each pin entry. This kind of computer encoder is generally known as a Priority Encoder.

3.1.3.2 Priority Encoder

The Priority Encoder addresses the above-mentioned issues by allocating a priority level to each input. The real output code will only refer to the input with the highest assigned priority because there was more than one input at the logic level "1" at the same time. So when an input with a higher priority is present it can neglect all other inputs with a lower priority. An example of an 8-input priority encoder is shown below.



Inputs								Outputs		
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	x	0	0	1
0	0	0	0	0	1	x	x	0	1	0
0	0	0	0	1	x	x	x	0	1	1
0	0	0	1	x	x	x	x	1	0	0
0	0	1	x	x	x	x	x	1	0	1
0	1	x	x	x	x	x	x	1	1	0
1	x	x	x	x	x	x	x	1	1	1

X = dont care

Figure 3.6: 8-to-3 priority encoder with truth table

Generally, for this particular application, a regular priority encoder with all its inherent complexity isn't sufficient. Hence we have few special digital encoders that becomes suitable for the analog to digital conversion technique like ROM encoders, XOR encoders, Multiplexer based encoders, Fat tree encoders, Wallace tree encoders etc. Few of them are discussed in the next chapter.

The encoder in Flash ADC circuit converts the thermometer code to equivalent binary format. The thermometer code is the output of comparator which is series of 1's followed by series of 0's.

CHAPTER 4

SOFTWARE

4.1 Tanner EDA Tool

Tanner Tools is a complete set of software for the design, simulation and inspection of electronic integrated circuits (IC) and Micro-Electro Mechanical System MEMSs. This product is actually a complete product line for circuit schematic design, layout design, and inspection of integrated and analog circuits and MEMS devices. Graphic Designer Mentor is one of the leading technology companies for the electronic and semiconductor circuit design in the field of automation. This collection includes complete tools for electronic circuit design that can do all the work of circuit design, SPICE simulation, physical circuit design as well as checking circuit design rules such as DRC and LVS. For this process there are three tools used, one being S-edit for circuit schematic design, the T-SPICE circuit simulator engine integrated with S-edit, and finally L-edit for physical circuit design or printed circuit board case.

Tanner EDA Tools has an incredible reputation for high performance and affordability for verification of design, layout, analogue or composite signal (AMS), as well as IoT and MEMS applications. The tools in this package are easy to design and user friendly. Its user interface is highly functional and the UI design team has made every effort to maintain its elegance while also increasing usability of products. This product processing speed is high and has good compatibility with different hardware and software systems. It needs no heavy hardware and can be built with minimal hardware.

Tanner S-Edit schematic capture enhances your design productivity while handling the most complex IC designs. This powerful environment facilitates fast, 64-bit rendering and cross-probing between schematic, layout, and LVS reporting at net and device levels.

The Tanner T-Spice simulator, which is a part of the Tanner Tool Suite, blends easily with other design tools in the flow and is complaint with industry-leading standards. It enhances simulation accuracy with advanced modeling, multi-threading support, device-state plotting, real-time waveform viewing, and analysis, and a command wizard for simple SPICE syntax creation.

CHAPTER 5

DESIGN METHODOLOGY

5.1 Designing of a Comparator

As comparator is the most significant part of Flash ADC various designs were analyzed to choose a suitable one with least power and area parameters.

5.1.1 Comparator Using Logic Gates

Comparator circuit was designed using basic digital logic gates such as AND, XOR, Inverter and OR logics which is also called as **2-bit comparator**. To obtain the necessary Expressions the truth table with two inputs A and B and three output cases are considered and K-Map is designed.

INPUTS		OUTPUTS		
A	B	A>B	A<B	A=B
0	0	0	0	1
0	1	0	1	0
1	0	1	0	0
1	1	0	0	1

Table 5.1: Truth Table of 2-Bit Comparator

Using the following expressions the logic circuits were designed.

1. A>B ----- A.(~B)
2. A<B ----- (~A).B
3. A=B ----- (~A).(~B)+A.B

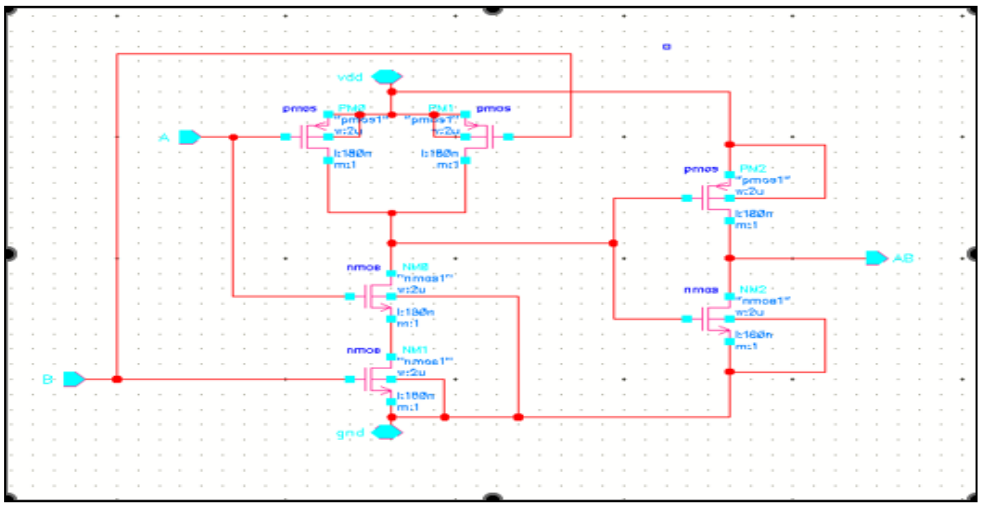


Figure 5.1 AND logic

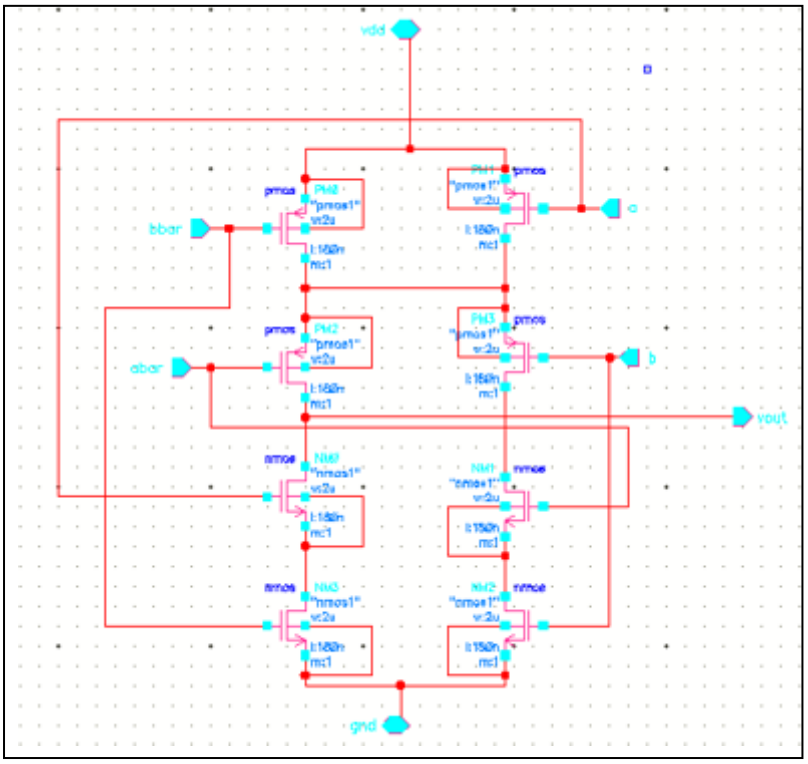


Figure 5.2 XOR logic

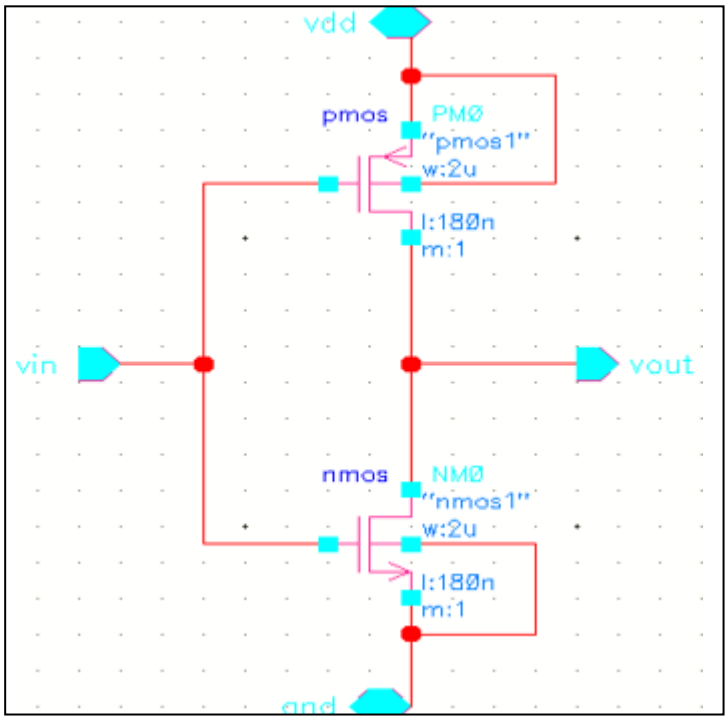


Figure 5.3: Inverter logic

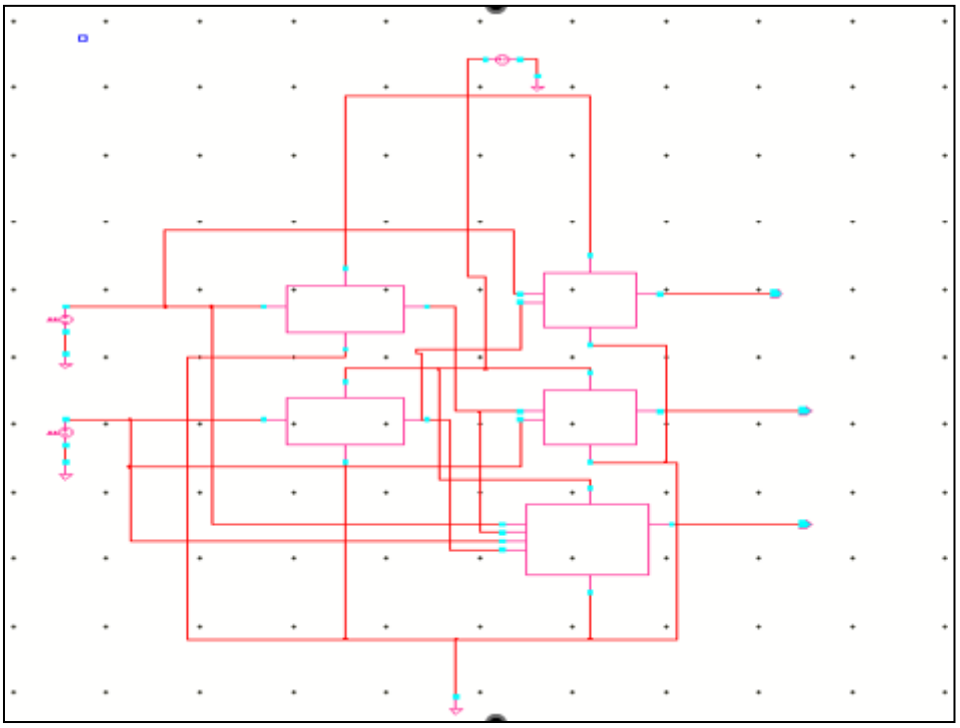


Figure 5.4: Schematic of 2-bit Comparator

As there were large number of MOSFETs incorporated in the design, the processing speed was reduced which in turn increased power consumption. This becomes unsuitable for the Flash ADC processing.

5.1.2 Open-Loop Comparator

An open-loop comparator is an operational amplifier designed to operate with its output saturated, close to the supply rails, depending on the polarity of the differential input applied. The op-amp does not use feedback. Therefore no compensation is needed to achieve device stability. It does not pose a concern as the linear operation is of no interest in comparator design. The key advantage of not compensating the op-amp is that it can be designed to achieve the largest possible bandwidth, thereby increasing its time response. Open Loop Comparator consists of two stages: input stage and output stage, as shown in Figure 5.5.

The input stage is a differential pair with current mirror, which providing high gain and the output stage is a buffer that provides large output swing and high stability. The benefit of this circuit is that the circuit consumes minimal number of transistors and thus the total circuit area is small. Open loop comparator is ideally suitable for low power applications, and requires only lesser area and providing the highest performance.

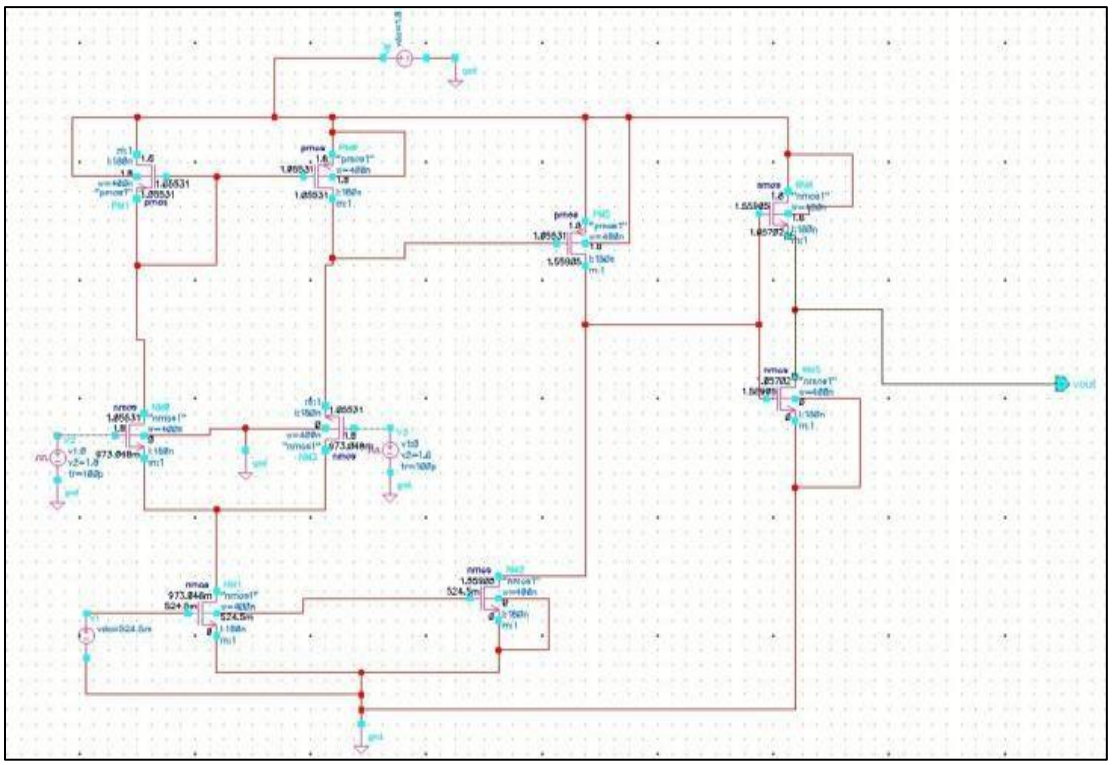


Figure 5.5: Open loop comparator

The first stage is a NMOS differential-pair consisting of transistors M1 and M2, with PMOS transistors M3 and M4 serving as a diode-connected active load. NMOS Transistor M3 is used to bias the pair of inputs. The output stage is a current- sink inverter composed of transistors M5 and M6.

In the open – loop configurations, clipping of the output waveform can occur when the output voltage exceeds the saturation level of op-amp. This is due to the very high open – loop gain of the op-amp. This feature actually makes it possible to amplify very low frequency signal of the order of microvolt or even less, and the amplification can be achieved accurately without any distortion. However, signals of such magnitudes are susceptible to noise and the amplification for those applications is almost impossible to obtain in the laboratory. Thus the design was simulated resulting low stability and large power consumption on chip.

5.1.3 Dynamic Comparator

The dynamic latch comparator shown in figure below is most widely used because it has many advantages such as high-speed, zero static-power consumption, high input-impedance and full swing output. During the pre-charge phase both the output nodes are charged to power supply voltage and during the evaluation phase the output of the comparator depends on the differential input. The basic principle of a dynamic latch comparator comes from its positive feedback that triggers the regenerative action. This operation becomes quite slow when the voltage is in the small signal range and a large capacitive load at the output will greatly degrade the speed.

The major drawback of the dynamic latch comparator is the offset error caused by transistor mismatch and unbalanced charge residues.

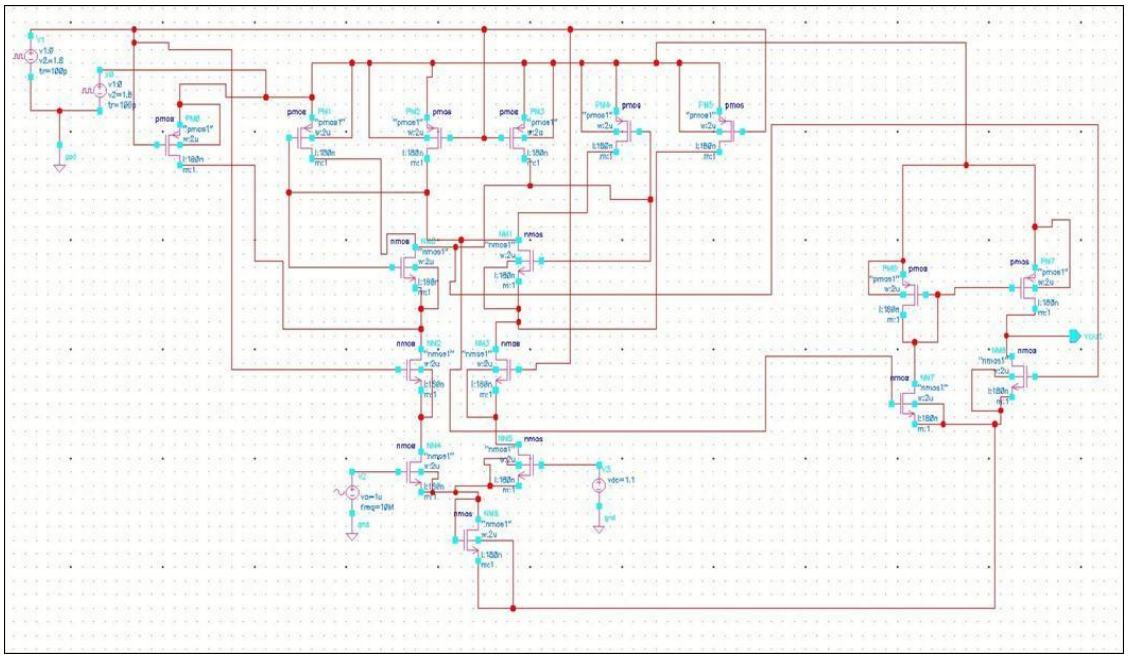


Figure 5.6: Schematic of Dynamic Comparator

5.1.4 Current Mirror Comparator

A current mirror may be a circuit designed to repeat a current through one active device by controlling the present, in another active device of a circuit, keeping the output current constant regardless of loading. The current being "copied" sometimes is a varying signal current. Conceptually, a perfect current mirror is just a perfect inverting current amplifier that reverses the present direction also. Or it can contain a current-controlled current source (CCCS). The current mirror is employed to supply bias currents and active loads

to circuits. The circuit topology covered here is one that appears in many monolithic ICs. It is a Widlar mirror without an emitter degeneration resistor within the follower (output) transistor. Another topology is the Wilson current mirror. The Wilson mirror solves the first effect voltage problem during this design. Mirror characteristics

The first is that the transfer ratio (in the case of a current amplifier) or the output current magnitude (in the case of a continuing current source CCS).

The second is its AC output resistance, which determines what proportion the output current varies with the voltage applied to the mirror.

The third specification is that the minimum drop across the output part of the mirror necessary to make it work properly.

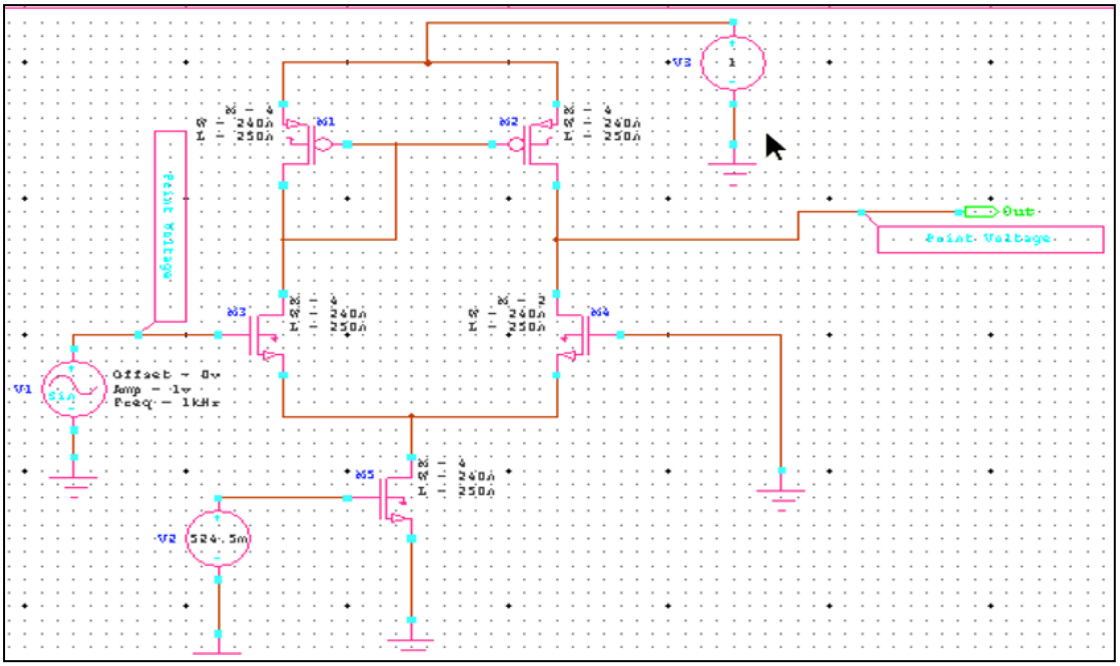


Figure 5.7: Current mirror comparator

The current mirror uses the principle that if the gate-source voltages of the two identical MOSFETs are equal then the current flown through their drain terminals should be same.

The figure above shows the circuit implemented using simulation tool. The transistors M1 and M2 are operating in saturation mode, so the output current is directly related to reference current.

$$I_{out} = \frac{1}{2} \mu_n C_{ox} (W/L)_2 (V_{gs} - V_{th})^2$$

$$I_{ref} = \frac{1}{2} \mu_n C_{ox} (W/L)_1 (V_{gs} - V_{th})^2$$

The disadvantages can be considered as follows, the output resistance is finite and small value. The mirror adds noise and distortion.

5.1.5 Proposed Comparator Design

Two-stage OP-AMP with output inverter was selected to achieve the best performance of Flash ADC. Op-Amp is basically a DC-coupled high-gain electronic voltage amplifier having differential input signals and, generally a single-ended output waveform. The op-amp consists of a differential input stage which driving a current mirror load and followed by a common-source amplifier stage and a buffer stage.

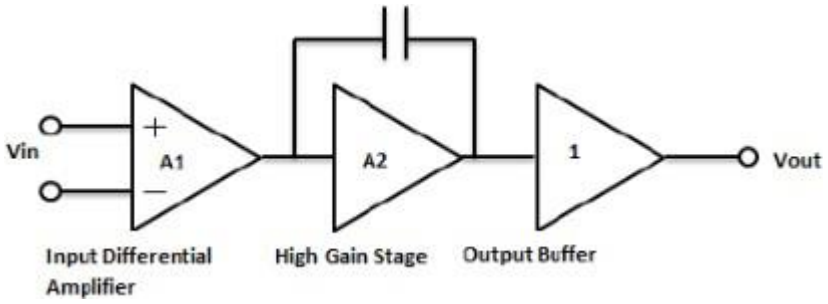


Figure 5.8: Block diagram

The input differential amplifier block is designed to provide high input impedance, large CMRR and PSRR, low noise, high gain and low offset voltage. The second stage of the op-amp performs level shifting which added gain as well as the conversion of differential to single ended. The output buffer is the last block where it produces low output impedance.

Differential stage has two inputs, inverting input and non-inverting input. A differential input signal is applied across the two input terminals that will be amplified according to the gain of the differential stage.

In the first stage, transistor M5 provides the biasing to entire circuit, transistors M1 and M2 form the differential input pair actively loaded by a current mirror pair formed by

transistors M3 and M4. In the second stage, transistor M6 is a common source amplifier actively loaded by transistor M7.

This design has comparatively lower power consumption along with a lower propagation delay.

The current mirror topology helps to conversion of the input signal from differential to single-ended. And load helps with common mode rejection ratio. Common source amplifier is used to improve gain and output swing of first stage.

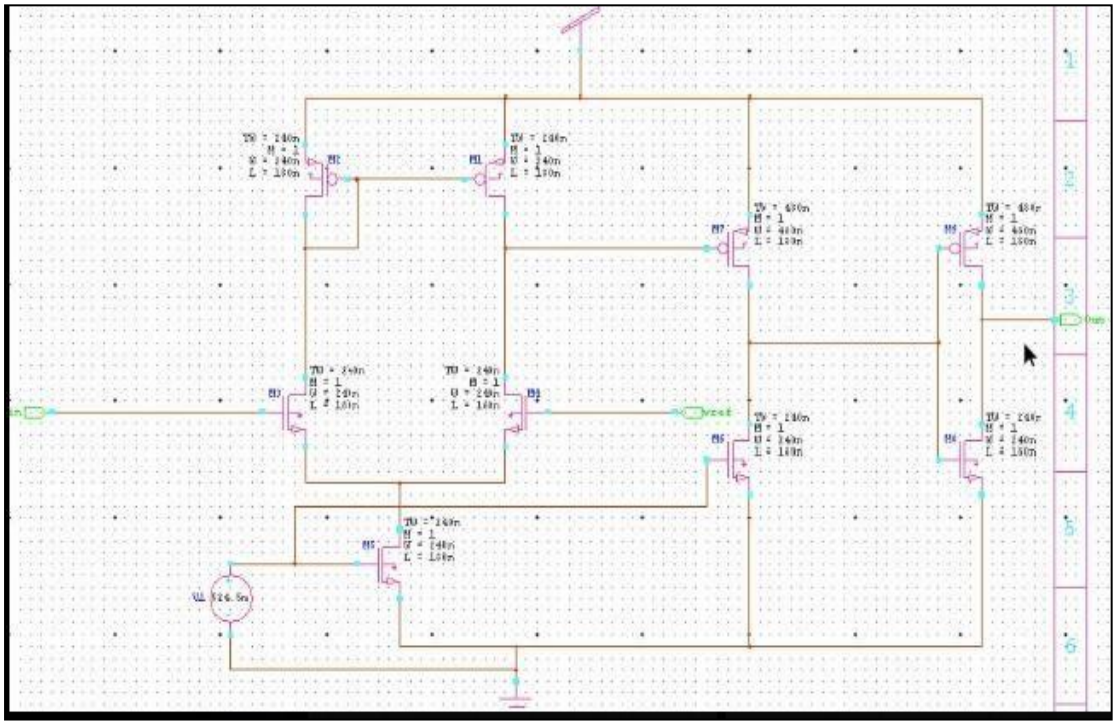


Figure 5.9: Two Stage Op-Amp with Output Inverter

Buffer stage is added in order to maintain stability of system. Op-amp uses a dual-polarity power supply V_{dd} and V_{ss} so the given AC signals can swing above and below ground.

The design specifications shown in Table 5.2 were used to simulate the design.

Parameters	**Values**
Power supply, V_{dd}	1.8v
Input voltage, V_{in}	2v
Reference voltage ,V_{ref}	1v
M1 (W/L)	240n/180n

Table 5.2: Design Specifications

5.2 Digital Encoder Design

The last block of Flash ADC is Encoder. This block converts series of 0's and 1's, which is output of array of comparators often called Thermometer-Code to Binary Code. Hence it is also called as thermometer to binary converter.

The ability to tolerate errors and the power dissipation are two critical parameters in the architecture of the thermometer to binary code converter. In the comparator offset voltage produces a **bubble error** in the thermometer code. The bubbles are digital zeros introduced in the code.

There are primarily two methods for mitigating the bubble error effect. The first approach is to convert the code of the thermometer to gray code (intermediate step) and convert to binary code afterwards. But the accuracy of the gray code declines gradually as the thermometer code produces more number of bubble errors. The second approach is the implementation of **Wallace tree encoder**. Because of its inherent global bubble error correction / suppression capability, this technique provides high robustness to bubble error and stuck to fault error. Few basic encoder types have been discussed below.

5.2.1 Rom Encoder

A standard and uncomplicated method to convert the thermometer code to binary code is to utilize ROM encoder. The ROM based approach has two stages. In the initial stage, the thermometer code is converted into 1 out of 2^{N-1} code. This can be achieved by using NAND gates array. The second stage is the configuration of ROM which receives the 1 out of 2^{N-1} code as input and selects suitable row in the ROM and generates the binary outputs.

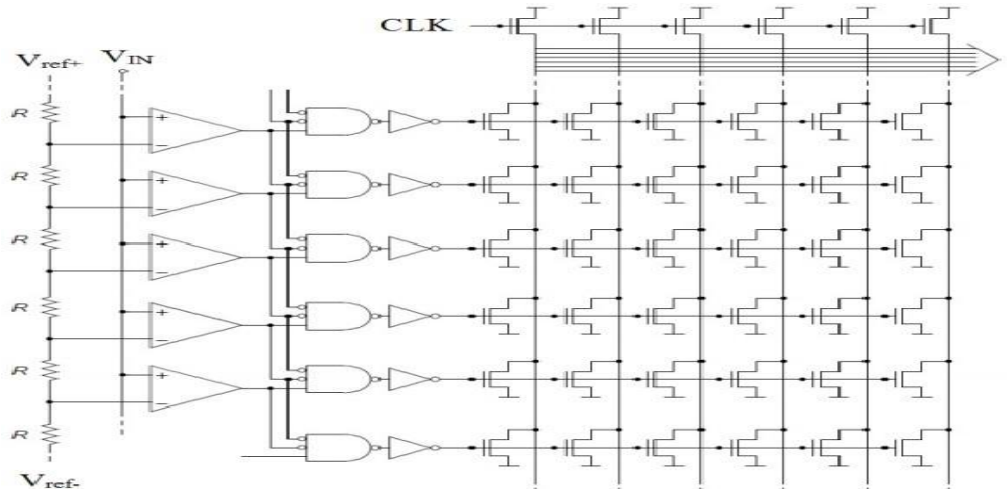


Figure 5.10: ROM encoder

5.2.2 Multiplexer Based Encoder

Multiplexer based encoder requires less hardware and has a smaller critical path compared to Wallace tree encoder. If half of the outputs in the thermometer code are high logic, it indicates that most significant bit (MSB) of the binary output is logic high. So MSB is the thermometer output at level of 2N-1. In order to find out the value of second most significant bit, the original thermometer code is divided into two partial thermometer codes spaced by 2N-1. The encoding is done with aid of 2:1 multiplexers. The multiplexer control input is the binary output which was previously encoded. The second most significant bit is computed with the use of two partial thermometer codes and 2:1 multiplexers. This cycle is sustained continuously until one 2:1 multiplexer endures. The last 2:1 multiplexer output is the least significant bit.

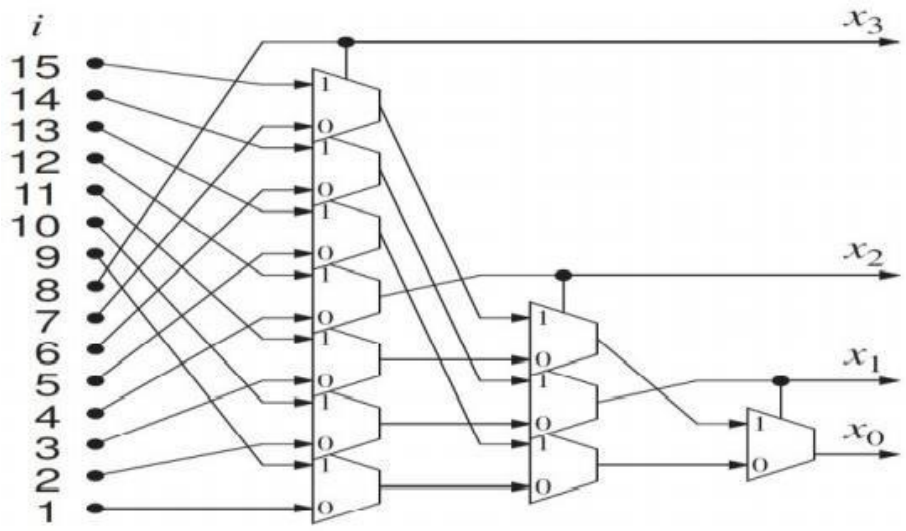


Figure 5.11: Multiplexer Based Encoder

5.2.3 Fat tree encoder

The thermometer to binary encoding is achieved in two steps in the fat tree encoder. The first stage converts the thermometer code to 1 out of N code indicating there is only single logic high is present in the code. The second stage translates the 1 out of N code into binary code using multiple trees of OR. The binary bits are produced using Fat tree encoder which has high speed of operation with less power dissipation in compared to ROM encoder. Fat tree encoder doesn't need a clock signal or pull up resistors. Noise immunity of the fat tree encoder is greater than that of the ROM encoder.

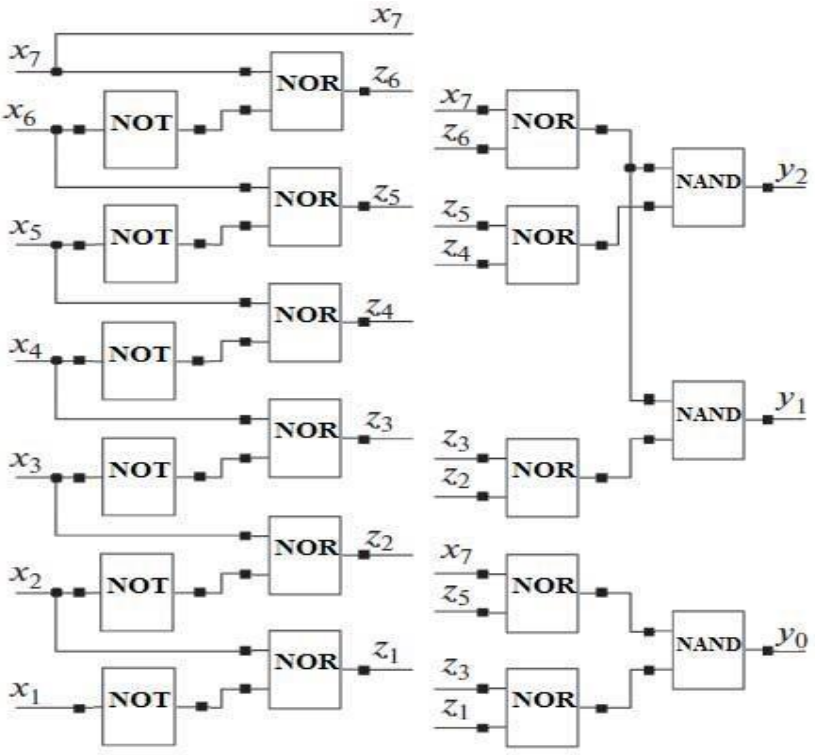


Figure 5.12: Fat Tree Encoder

5.2.4 Proposed Encoder

Wallace tree encoder consists of full adders. For each 1 bit increase it adds one more stage to the design. This can be used for correcting bubble errors in greater order. Power dissipation is also less in case of Wallace tree encoder when compared to ROM encoder. It is also known as ones counter. It counts the number of ones at the input and provides corresponding binary output hence the bubble errors of any order can be corrected.

It is also considered as fast multiplier because it uses carry save algorithm in order to reduce latency. In low power applications this encoder can be used. It provides better results for any resolution but still speed is compromised. This encoder also serves as a fast multiplier.

As output produced by comparators stage is a thermometer code due to multiple non-idealities and mismatches in comparators and their inputs, the output may not be a symbol of thermometer code, but has some irregularities. So, the thermometer to binary converter stage may not be able to convert it to binary code as it is generally a state machine that accepts only thermometer code as input and may produce a garbage output if provided some other input that is not thermometer code.

There may be some zeroes in-between a series of ones. For example, the output may be "01011111" instead of "01111111". "01011111", when fed to thermometer to binary converter will produce garbage value. Either "01111111" should be given or "00111111" or "00011111". This will reduce the error. The presence of zeroes in a series of one or presence of ones in a series of zeroes in the comparators' output is termed as bubble error. In order to reduce bubble error to highest order and to obtain desired Flash ADC output we chose Wallace tree.

The Wallace tree encoder is built with full adder cells. The full adders are arranged to sum the inputs so as to form Wallace tree (refer table). Even when bubble errors are present, this encoder converts output of comparator into correct binary output. Another advantage of this encoder is flexibility such that suitable topology can be selected according to speed and power requirements. The number of full adder cells needed to implement an N bit encoder is given by the equation,

$$X_N = \sum_{i=1}^{N} (i-1).2^{N-1}$$

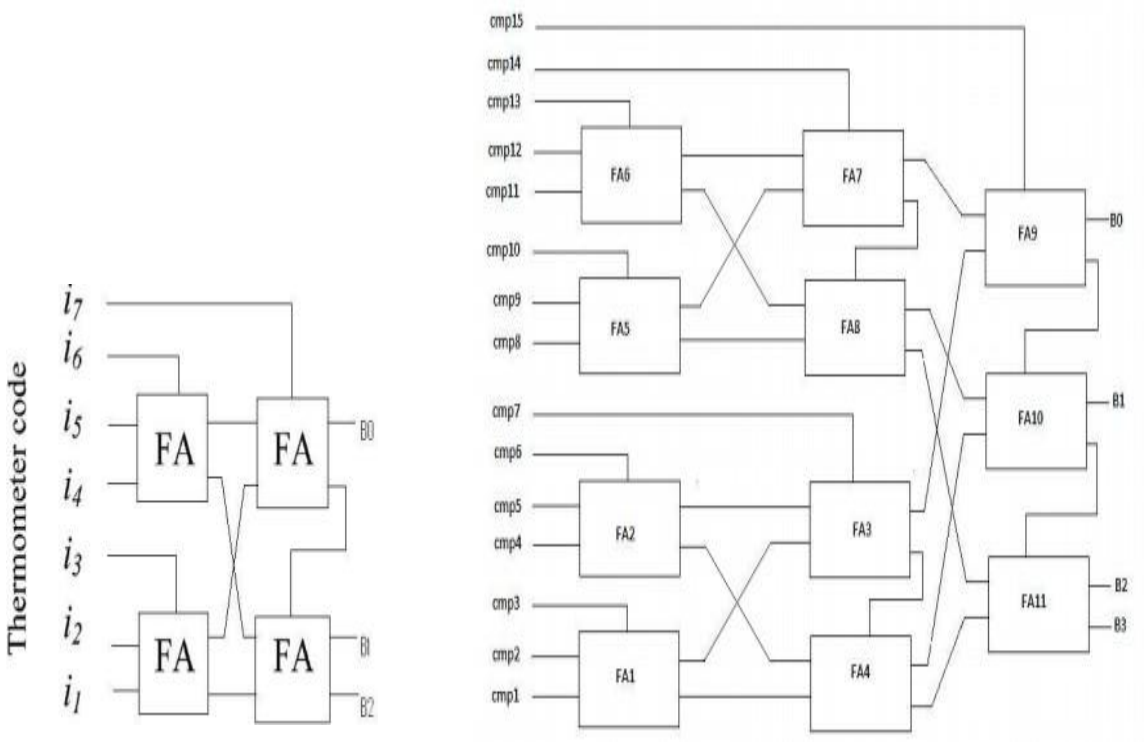


Figure 5.13: 3-bit and 4- bit Wallace tree encoder

A 3- bit and 4- bit Wallace encoder are shown in figure 5.13 and the truth table for counting number of one's is given in table below.

A	B	Cin	Cout	Sum	Decimal equivalent of no. of ones in input
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	0	1	1
0	1	1	1	0	2
1	0	0	0	1	1
1	0	1	1	0	2
1	1	0	1	0	2
1	1	1	1	1	3

Table 5.3: Full Adder used as Ones Counter

The encoder designed using Tanner tool is shown below in figure.

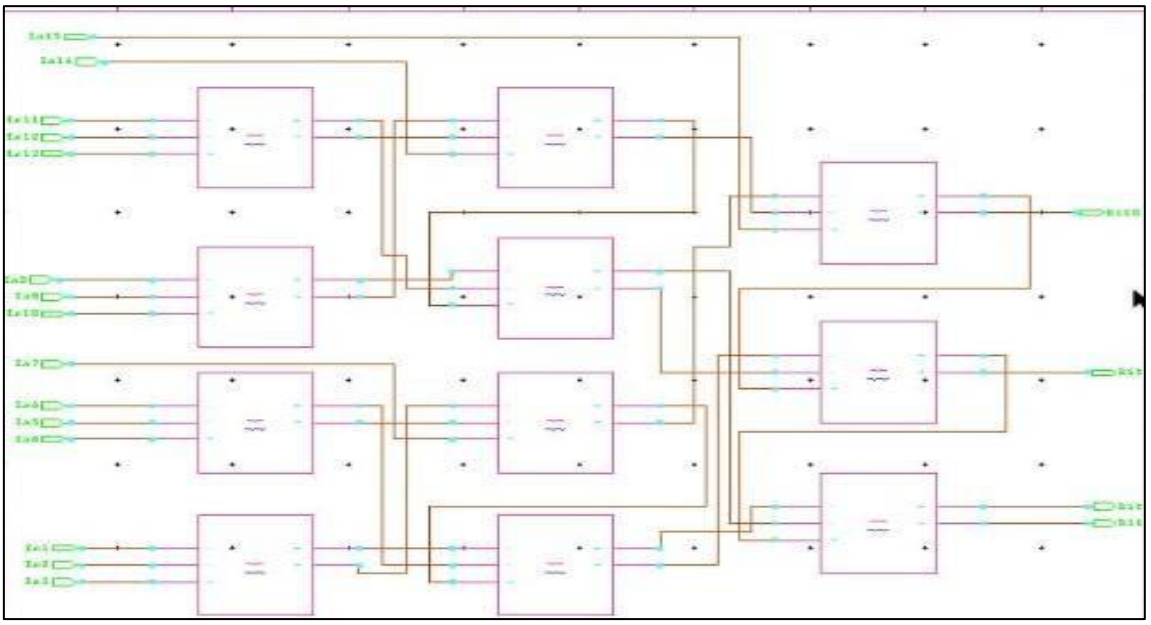


Figure 5.14: Proposed Encoder

CHAPTER 6

RESULTS

All the components were successfully designed and analyzed by the Tanner tool using 180nm technology.

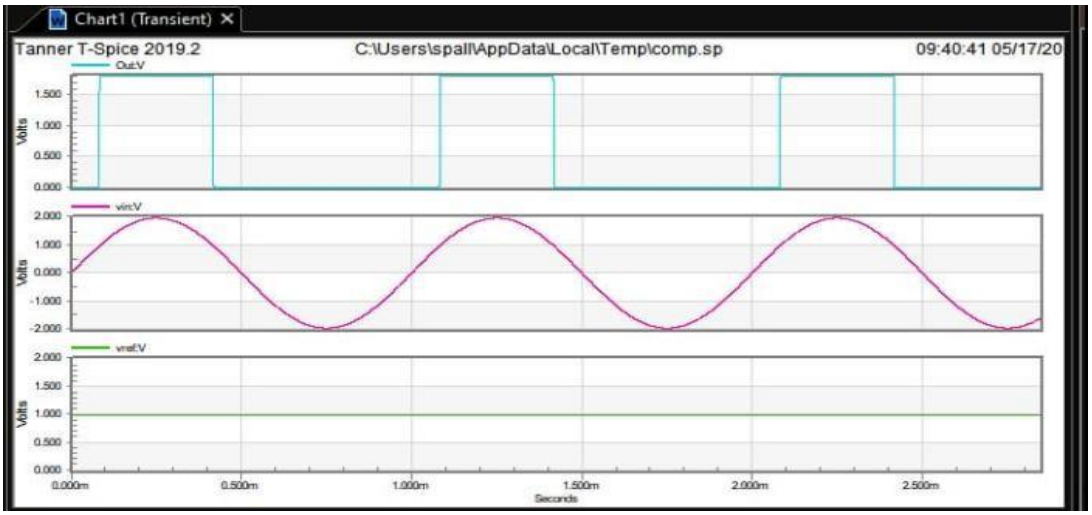


Figure 6.1: Output waveform of proposed comparator

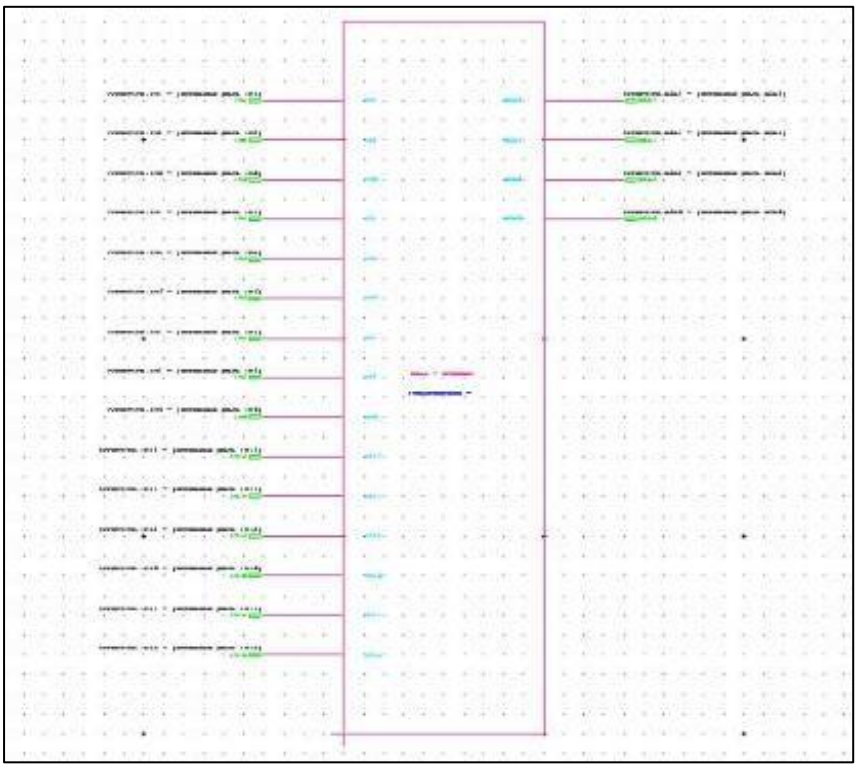


Figure 6.2: Encoder symbol

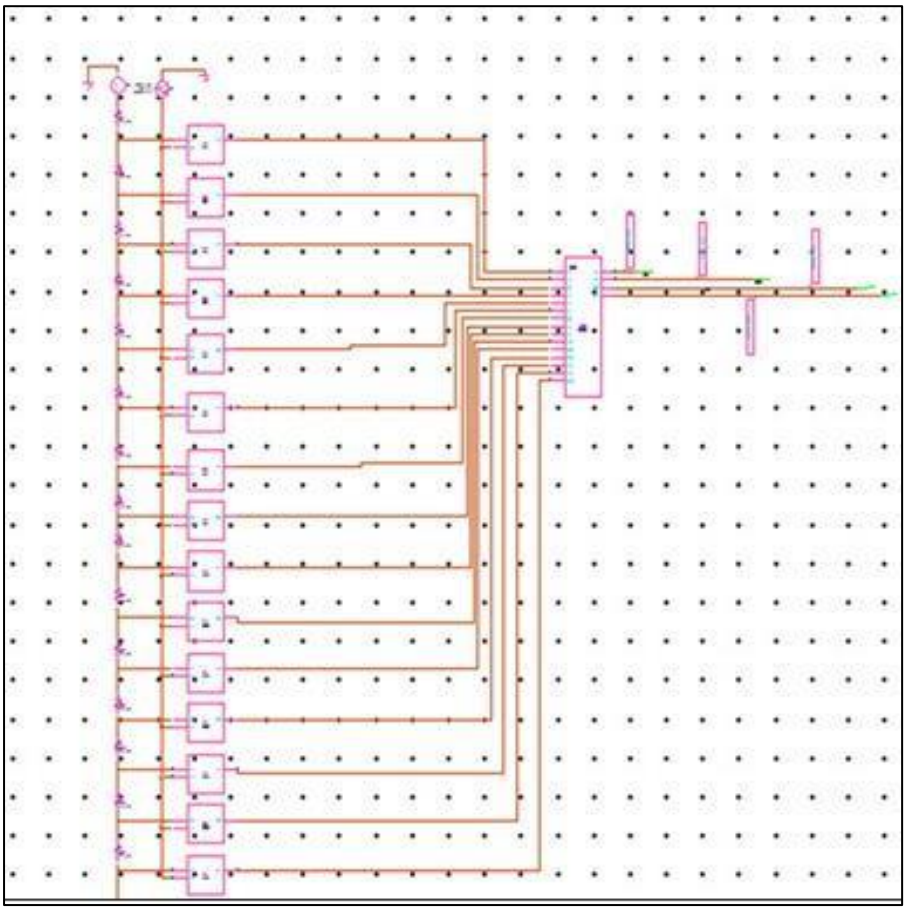


Figure 6.3: Flash ADC Schematic

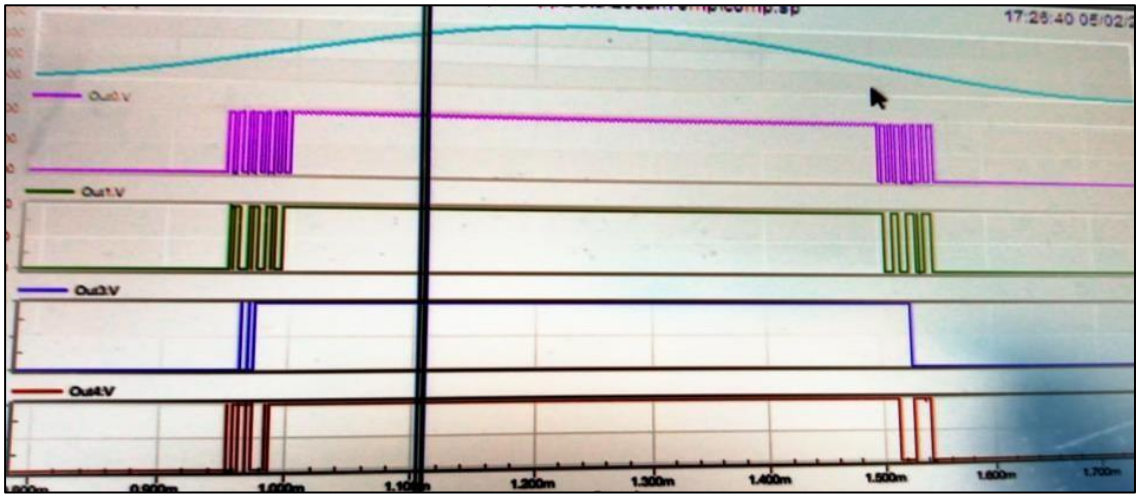


Figure 6.4: Output Waveform of Flash ADC

The proposed design offers a low-power solution with reduced Kickback noise for low power applications. This design is simulated and analyzed using 180nm technology. Simulation results are tabulated and analysis has been done.

Parameter	COMPARATOR
Architecture	Flash ADC
Resolution	4-bit
CMOS Technology	180nm
Power supply	1.8v
Power	0.078nW

Table 6.1: Simulation Results

CHAPTER 7

APPLICATIONS AND ADVANTAGES

1. The very high sample rate of ADC enables high-frequency applications such as
    - Detecting radar
    - Wideband radio receivers
    - Sampling oscilloscopes
    - Optical communication links
    - Ultra wideband applications
2. It is used in the applications where the conversion speed of analog input into digital data should be very high.
3. It is used in NAND Flash memory, where upto 3 bits are stored per cell as 8 voltages level on floating gates.
4. Flash ADC is embedded in a large IC containing many digital decoding functions. These are suitable for applications which require large bandwidth.

CHAPTER 8

CONCLUSION

Flash ADC is considered as best architecture for high speed and low power applications. Different comparators and encoders were designed and analyzed. Among them a two stage op-amp with output buffer stage was selected with power dissipation of 14nW.

Also Wallace tree encoder can be easily pipelined, giving the assurance that it will never appear as the limiting part of an analog-to-digital converter design in terms of speed. If there is any bubble in the comparator output, then this encoder can only generate a maximal error of one LSB. Finally by integrating the resistor ladder along with comparator and encoder, a 4 bit Flash ADC is designed and its performance is verified. Power dissipation of designed Flash ADC is 0.078nW.

In CMOS circuits, most of the power dissipates through dynamic power dissipation than static power dissipation. In CMOS circuits, static power dissipation is in the range of nano watts. The most significant source of dynamic power dissipation is caused by transition activities of the circuits. A higher operating frequency leads to more transition activities in the circuits and results in increased power dissipation. Using proper encoding techniques may reduce switching activity in the circuit. This will reduce the overall transition activity. Hence, the dynamic power dissipation can be reduced in VLSI circuits effectively.

From reference	Resolution	Power (µW)
[4]	4-bit	17.5
[3]	4-bit	0.042
[1]	4-bit	0.023
[5]	4-bit	0.00198
[2]	4-bit	0.00119
Proposed design	4-bit	0.000078

Table 8.1: Comparison to Previous Designs

CHAPTER 9

FUTURE WORK

- Further optimization of circuit can be done by using less number of transistors.
- All parameters of Flash ADC can be considered to implement high resolution Flash ADC.
- We can further work on the project to reduce power consumption and to increase the speed.
- In order to reduce offset in comparator which improves efficiency of total Flash ADC, offset can be adopted.
- We are looking towards same design in 90 nm and 45 nm technology so as to get lesser power and lesser area based chip of ADC.

CHAPTER 10

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