VISVESVARAYA TECHNOLOGICAL UNIVERSITY

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PROJECT REPORT

ON

"16.8/15.2/33.7 PPM/℃, 81 nW High PSRR Single/Dual-output CMOS Voltage Reference for Portable Biomedical Application"

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CERTIFICATE

This is to certify the Project Report entitled **"16.8/15.2/33.7 PPM/℃ , 81 nW High PSRR Single/Dual-output CMOS Voltage Reference for Portable Biomedical Application",** prepared by **Md Istiyak , Malob Chaudhri, Manish Kumar** bearing **USN-1CR16EC079, 1CR16EC075, 1CR16EC076** a bona fide student of **CMR Institute of Technology, Bengaluru** in partial fulfillment of the requirements for the award of **Bachelor of Engineering in Electronics and Communication Engineering** of the V**isvesvaraya Technological University, Belagavi-590018** during the academic year 2018-19.

This is certified that all the corrections and suggestions indicated for Internal Assessment have been incorporated in the report deposited in the departmental library. The seminar report has been approved as it satisfies the academic requirements prescribed for the said degree.

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ABSTRACT

An important part in the design of analog integrated circuits is to create reference voltages and currents with well-defined values. To accomplish this on-chip, so called bandgap reference circuits are commonly used. A typical application for reference voltages is in analog to-digital conversion, where the input voltage is compared to several reference levels in order to determine the corresponding digital value. The emphasis in this thesis work lies on theoretical understanding of the performance limitations as well as the design of a bandgap reference circuit. A dual-output voltage reference circuit with two reference voltages of 60 mV (Vref1) and 172 mV (Vref2) & single output voltage reference of 400mv is presented in this report. With a novel and precise circuit structure, the proposed circuit, operating in the sub-threshold region, integrates two different output voltages into a circuit to form a dual-output voltage reference, and cascade current mirrors are used to enhance the power supply rejection ratio (PSRR). The proposed circuit was designed in a standard 180nm CMOS process and has a series of attractive features: low-temperature coefficient (TC), high-PSRR, low-Line sensitivity (LS), small-chip area and low-power consumption.

In this project, we are making Bandgap Reference circuit of temperature coefficient of 12.38/15.5/33.7 ppm/℃ , High PSRR , dual output , low power are implemented in an 180nm CMOS technology.

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Chapter1

INTRODUCTION

Bandgap reference circuit generates a voltage that is constant over process, temperature, and DC power supply variations, and rejects power supply noise and ripple as well. Bandgap circuit has a nominally zero temperature coefficient (Zero TC) since its voltage is constant across temperature variation. The voltage and bias current from the bandgap reference circuit is feed into another circuit blocks such as current mirror or differential pair as a reference or biasing voltage to power up it.

The Challenge with the small medical wearable devices is low power High performance, Noise immune, i.e ability to reject noise so the PSRR should be high.

When MOSFET was introduced that time PMOS and NMOS were the technology used for devices . The question is that in which mode these IC's should be used for better efficiency and which one to choose PMOS or NMOS. Since PMOS consumes and dissipates more power compare to NMOS so that NMOS was chosen. If we talk about the mode of operation than we know that in cutoff region MOSFET consumes zero power but also Tx is in off mode , Now we come to triode mode , in this mode Tx act as resistor whose resistance is a function of the voltage to the gate terminal . Due to change in power consumption we decided to choose to work in saturation mode , In this mode Tx need fixed amount of power to work , soon after CMOS is Introduced and decided to replace NMOS with CMOS which has features like very low

power consumption ,High performance and also High noise immunity. Hence we decided to pursue with CMOS technology which is more efficient compare to MOSFET and BJT.

Chapter 2

LITERATURE SURVEY

2.1 Principles of a Bandgap voltage reference circuits

In 1964 Hilbiber studied the possibility of creating an integrated circuit without low dependency of temperature. This uses an avalanche diode as a reference voltage source, theshorttermstabilityoftheproducedreferencevoltagewas10-50ppm within a certain temperature range. The problem was to extend this behavior for a period longer than 1000 hours. To solve this problem, a new reference voltage source was presented with a nominal output of 1.25670 V and a long-term stability for a period over 12000 hours. For an ideal p-n junction, the forward voltage (VF) and temperature dependence (d_{VF}/d_T) are function of current density and junction impurity profile that is given by Shockley's equation.(eq.2.1)

$$P_n = \frac{(n_i)^2}{N_D} \quad \text{AND} \quad n_p = \frac{(n_i)^2}{N_A} \qquad 2.1$$

$$I = I_s \left[e^{\left(\frac{qV}{kT}\right)-1} \right]$$

Where Dp,n are the diffusion coefficients of holes and electrons and Lp,n are the diffusion lengths. From equation 2.1 is possible to verify that the base-emitter voltage for a transistor is a function of the base current. Where IS is given by:

$$I_S = q\left(\frac{D_p}{L_p}P_n + \frac{D_n}{L_n}n_p\right) \quad 2.2$$

As observed by Hilbiber, 2.1 and 2.2 it is possible to express (V_{BE}) in a Taylor's series expansion and obtain the temperature and current dependence as shown in Eq. 2.3.

$$V_{BE} = \frac{KT_O}{q}\left\{ln\frac{I_C}{I_S(T_O)} + \left[ln\frac{I_C}{I_S(T_O)} - \left(\beta + \frac{E_{GO}}{kT_O}\right)\right]\left(\frac{T}{T_O} - 1\right) - \frac{\beta}{2}\left(\frac{T}{T_O} - 1\right)^2 + \ldots + \frac{\beta(-1)^{n-1}}{n(n-1)}\left(\frac{T}{T_O} - 1\right)^n + \ldots\right\}$$

$$V_{BE} > \frac{4kT}{q} T < 2T_O \quad 2.3$$

Where β is a constant which takes in consideration the temperature dependence of the diffusion coefficients and the diffusion lengths. As seen in Fig. 2.1 for the 2N917 and 2N1893 transistors, with the increasing of the junction doping density or current density, V_{BE} will increase and dV_{BE}/d_T will become less negative.

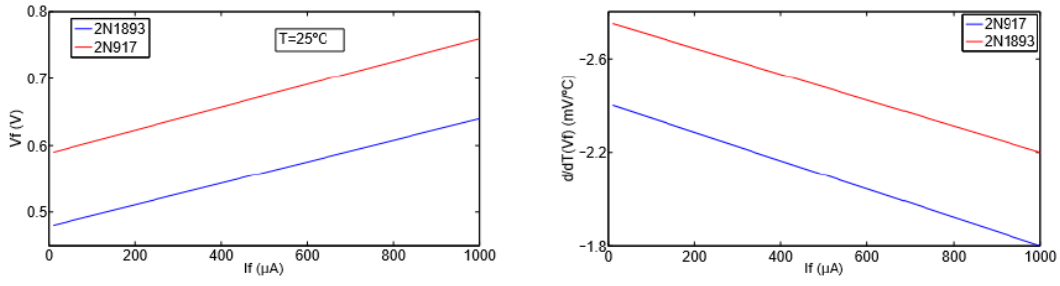


Figure 2.1: Forward voltage in order of current and temperature dependence of a forward Voltage in order of current in a diode configuration transistor.

Those different types of transistor have the same behavior with different magnitudes that is due to the emitter junction impurities that varies in those transistors affecting the forward voltage. In Fig. 2.1 the emitter current is represented, but if the gain is high, IB << IC, it is possible to consider by approximation IE = IC.

It is known that:

$$n_i{}^2 = C_O T^3 exp^{\left(\frac{-E_G}{kT}\right)} \quad 2.4$$

Thus

$$I_S = q n_i{}^2 \left(\frac{D_p}{N_D L_p} + \frac{D_n}{L_n N_A}\right) 2.5$$

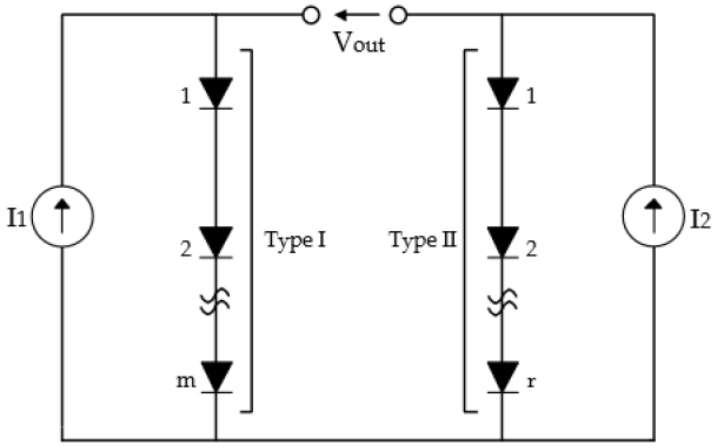


Figure 2.2: The basic circuit of the reference voltage source.

Which becomes,

$$I_s = C1 T \beta_p exp^{\left(\frac{-E_G}{kT}\right)} \quad 2.6$$

For a p+n junction and

$$I_s = C2T\beta_p exp^{\left(\frac{-E_G}{kT}\right)} \quad 2.7$$

For a n+p junction and

As seen in Fig. 2.2, Vout is given by the difference between V_{BEm} and V_{BEr}. Eq. 2.10 shows the simplification of Vout equation. Where θ is represented in eq. 2.8 and φ is represented in eq.2.9.

$$\theta = rln\frac{I_{c2}}{I_{s2}(T_O)} - mln\frac{I_{c1}}{I_{s1}(T_O)} \quad 2.8$$

$$\emptyset = r\beta_{II} - \beta_I \quad 2.9$$

$$V_{out} = \frac{kT_O}{q}\left[\theta + \left(\theta - \emptyset - \frac{E_{GO}}{kT_O}\right)\left(\frac{T}{T_o} - 1\right) - \frac{\emptyset}{2}\left(\frac{T}{T_o} - 1\right)^2\right] \quad 2.10$$

Where E_{GO} is the energy gap voltage at 0°K. The voltage source used in the simulations introduces an error of 3 to 5 ppm and the diodes introduces an error of 150 ppm to 200 ppm. Those errors have origin in the type of material of the semiconductors.

To obtain a stable temperature point it is important to achieve a stable point which is the balance between the voltage drop of the resistor and the diodes or the MOS in diode configuration. The fig.2.3 shows the positive temperature dependency generated by the voltage between the two p-n junctions, which generate a proportional current that permits the creation of an equivalent voltage drop in the resistor. The figure also shows the negative temperature dependency generated by the V_{BE} voltage. The diodes have a negative dependency of the temperature decreasing

2.2mV/℃ and the resistor has the voltage drop generated by the current and an additional error as represented in eq.2.11.

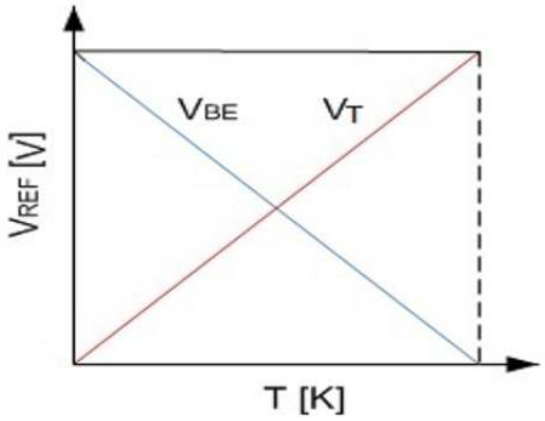


Figure 2.3: Temperature dependence of V_{BE} and resistance with the graphics superimposed.

$$R = R_O[1+\propto (T - T_O)] \qquad 2.11$$

Where α is the temperature coefficient of the resistor.

The methodology described before is represented in fig.2.4, where the thermal voltage increases 0.086mV/℃ and the V_{BE} decreases 2mV/℃. The factor K is the multiplier or the ΔV_{BE} which will allow the variation of the proportional to absolute temperature voltage. To demonstrate how a basic circuit works and understand how this balance between voltage drops in resistors and diode occur, the circuit in fig.2.5 was analyzed. The circuit shows in one side the voltage drop in V_{BE1} and on the other side a voltage drop in a resistor R and $N*V_{BE2}$. The current is assumed to be equal in both sides. The voltage drop in both V_{BE} is given in eq.2.12.

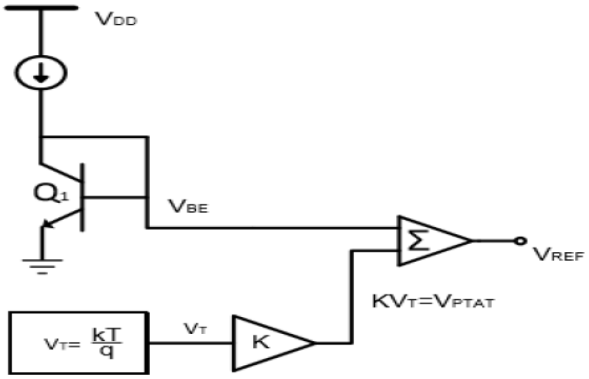


Figure 2.4: Block diagram of bandgap voltage reference .

$$V_{BE1} = nV_T ln\left(\frac{I_1}{I_S}\right) \qquad 2.12$$

$$V_{BE1} = nV_T ln\left(\frac{I_1}{NI_S}\right)$$

Assuming the difference between V1 and V2 is null , it is possible to obtain eq 2.13

$$V_{BE1} = RI_2 + V_{BE2} \qquad 2.13$$

$$RI_2 = V_{BE1} - V_{BE2}$$

$$RI_2 = V_T ln\left(\frac{NI_1}{I_2}\right)$$

Assuming $I_x = I_1 = I_2$

$$I_x = \frac{V_T ln(N)}{R}$$

This demonstrates that the voltage drop in the resistor must be equal to the difference between V_{BE1} and V_{BE2}. As known, V_T = kT/q , where k is the Boltzmann Constant and q is the magnitude of the electrical charge on the electron which is also

constant. Then, V_T is dependent of Temperature and the voltage drop is inversely dependent. Another way to obtain the temperature voltage dependency issuing MOS transistors, as shown in fig.2.6. The MOS transistors have a completely different behavior, although if the MOS transistors operate on the weak inversion region, the function of the circuit is equivalent to eq. 2.14.

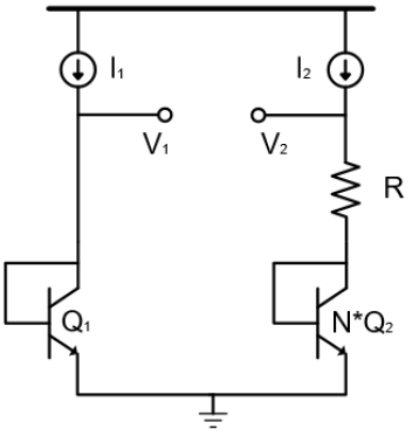


Figure 2.5: Basic temperature independent voltage operating with bipolar transistors

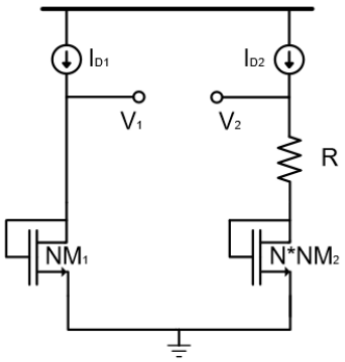


Figure 2.6: Basic temperature independent voltage using MOS transistor in the weak inversion region.

The mechanism of the bandgap circuit is very similar, but in this case the voltage drop will be V_{GS} instead of V_{BE}. The voltage drop in V_{GS} is shown in eq. 2.14

$$V_{GS1} = n\frac{kT}{q} ln\left(\frac{I_D}{Au_n C_{ox}(n-1)V^2{}_T}\right) + V_{THn} \qquad 2.14$$

$$V_{GS2} = n\frac{kT}{q} ln\left(\frac{I_D}{Au_n C_{ox}(n-1)V^2{}_T}\right) + V_{THn}$$

Following the same steps as in circuit with bipolar transistors, the final equation is obtained in eq.2.15.

$$V_{GS1} = RI_2 + V_{GS2} \qquad 2.15$$

$$RI = V_T ln\left(\frac{NI_{D1}}{I_{D2}}\right)$$

Assuming $I_x = I_{D1}=I_{D2}$

$$I_x = \frac{V_T ln(N)}{R}$$

$RI_2 = V_{GS1} - V_{GS2}$

As it is possible to observe, the equations 2.13 and 2.15 are equal. Although the transistors have different behaviors and different results as it will be shown next.

Next a few examples will be shown and compared, in order to conclude about the consumption, accuracy and other relevant factors of both.

2.2 Evolution of bandgap voltage reference circuits

After the study of Hilbiber, In 1971Robert Widlar proposed the first bandgap circuit. As can be observed in fig. 2.7 The circuit developed by Widlar produced a voltage Reference of 1.236V with a variation of nearly 4mv with a supply voltage of 7 to9V.Although it had poor performance, the main idea was there and a conventional bipolar bandgap reference circuit was created.

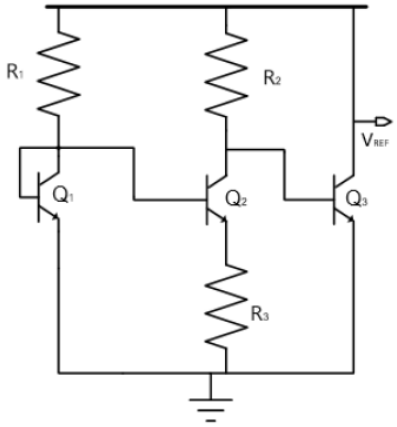


Figure 2.7: Low voltage reference in simpler form

Afterwards, in 1974 Brokaw developed a new voltage reference as shown in fig.2.8 with better performances namely the power dissipation ,the voltage input and the current values, although the stability of the reference voltage deteriorated. This circuit works with an input voltage of 4 V generating a reference voltage of 2.5 V with an error of 2%.

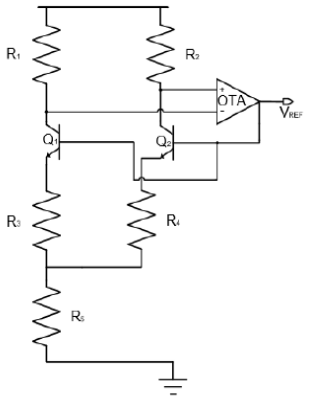


Figure 2.8: Low voltage reference deployed by Brokaw

2.2.1 Different Approaches on Voltage Reference Develop

During the development of a Voltage Reference Bandgap it is necessary to choose the elements of the circuit which guarantee a better performance and a low power dissipation. In this subsection it will be discussed the effects of the different elements in the circuit performance when applied to a conventional voltage reference circuit.

2.2.1.1 MOS vs. Bipolar Transistors

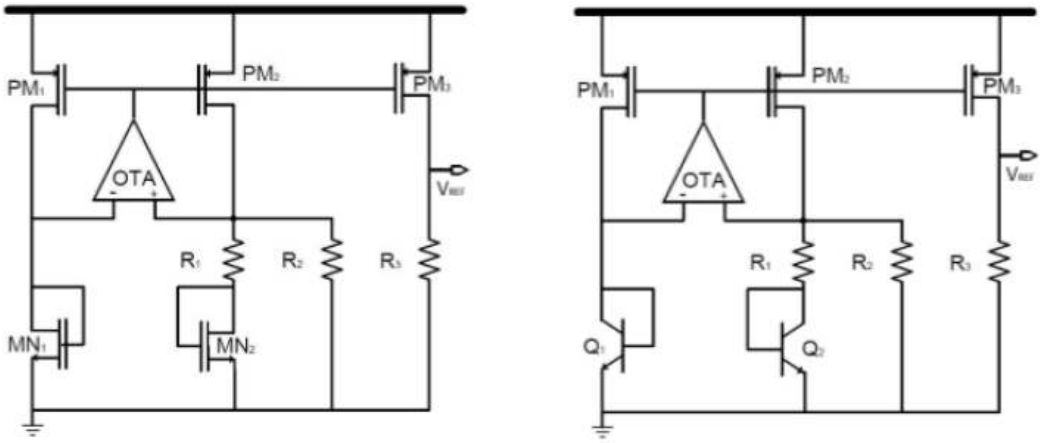


Figure 2.9: Conventional voltage reference circuit with (a) MOS transistor (b) bipolar transistor

Considering those two cases, primarily it is possible to verify that the second case needs a higher voltage supply. In order to guarantee the active zone of the transistors, at least 700 mV are needed for a bipolar transistor. Adding other elements, the supply voltage as to be at least 1 V. When using MOS transistors it is necessary to have a V_{DS} higher than the V_{DSAT}, as known a MOS transistor only has a linear behavior in the saturation zone. Usually circuits are developed paring the voltage necessary to supply both transistors, it is possible to realize that MOS needs 14 times less voltage then the bipolar to conduct normally. The equations of both circuits are similar as shown in eq. 2.16 and eq. 2.17. Considering that the voltage on the nodes A and B is equal due to the amplifier,

$$I_{R1} = \frac{V_{GS1} - V_{GS2}}{R_1} = \frac{\Delta V_{GS}}{R_1} \qquad 2.16$$

$$I_{R2} = \frac{V_{GS1}}{R_1}$$

it is possible to obtain the current flowing in resistor R1 and R2. Assuming that the current that flows in point B is the reference, than

$$I_{REF} = I_{R1} + I_{R2}$$

$$V_{REF} = \frac{\left(\frac{W}{L}\right) MP_3}{\left(\frac{W}{L}\right) MP_2} R_3 \left[\frac{V_{GS1}}{R_2} + \frac{\Delta V_{GS}}{R_1}\right]$$

$$I_{R1} = \frac{V_{BE1} - V_{BE2}}{R_1} = \frac{\Delta V_{BE}}{R_1}$$

$$I_{R2} = \frac{V_{BE1}}{R_1}$$

Assuming that the current that flows in point B is the reference , than

$$I_{REF} = I_{R1} + I_{R2}$$

$$V_{REF} = \frac{\left(\frac{W}{L}\right)MP_3}{\left(\frac{W}{L}\right)MP_2} R_3 \left[\frac{V_{BE1}}{R_2} + \frac{\Delta V_{BE}}{R_1}\right] \qquad 2.17$$

Analyzing the previous equations, it is possible to conclude that the difference between the two approaches has to be in the linearity of the coefficients of V_{BE} and V_{GS}. The temperature affects both V_{DS} and V_{GS}, which influences the current in the MOS transistors. In bipolar transistors only V_{BE} is affected.

2.2.1.2 MOS vs. Resistor

As it will be seen next, some circuits do not use a resistor to measure the thermal voltage by the voltage drop. Those circuits also don't balance the Thermal voltage increase with the gate-source voltage to obtain Vref. Instead the balance is made by summing the negative and positive gate source voltage, allowing to obtain a stable Vref. This approach also do not need an amplifier

which represents the major problem in reducing supply current value, so it use a supply current typically below 1μA, which is nearly impossible to obtain in a Bandgap with an opamp. On the other hand, in order to allow all the MOS transistors to work normally, the balance between the MOS transistors will force to increase the minimum voltage input, which as to be normally higher than 1V. As a result of this, the power consumption will be quite similar although the balance between gate source voltages with source-gate voltages will allow a most stable voltage references.

2.3 CMOS Bandgap Voltage Reference Circuits Approaches

In this section, some examples of Bandgap Voltage Reference are presented. The circuits symbolize three different type of approaches. In the first, the use of Bipolar Transistors with some resistors to form the PTAT and CTAT voltages. In the second approach MOS transistors are used with some resistors to produce the same effect as in the first and in the last approach only MOS Transistors are used performing PTAT and CTAT by V_{SG} and V_{GS} respectively.

2.3.1 A Sub-1 V MOS Bandgap Reference

In this subsection the Bandgap Voltage Reference with current mode structure (fig. 2.10) using Bipolar Transistors to generate the PTAT and CTAT voltages will be used.

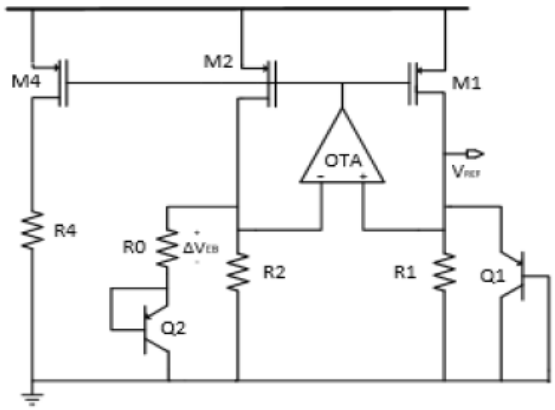


Figure 2.10: Bandgap reference with current mode structure

The concept of this circuit is using two different currents, which are proportional to V_{BE} (CTAT) and V_T(PTAT).The PMOS transistors have the same lengths and the resistors R1 and R2 the same value, the use of an amplifier will force an equal voltage in the inputs. Using the current mirror will force the currents that flow in PM1, PM2 and PM4 transistors to be the same. Then, it is possible to obtain eq.2.18 and eq.2.19

$$I_4 = I_1 = I_2 = \frac{V_{EB1}}{R_1} + \frac{V_T ln(N)}{R_O} \qquad 2.18$$

$$V_{REF} = I_4 R_4 = \frac{R_4}{R_1}\left(V_{EB1} + \frac{R_4}{R_0} V_T ln(N)\right) \qquad 2.19$$

Adjusting the values of the resistors ratio and the value N (multiplier of the transistor) it is possible to obtain a stable Voltage Reference value. Another aspect to consider is the minimum

voltage supply of the circuit and it is possible to calculate the value by eq.2.20.

$$\mathbf{minV_{DD} = \{max\ \{V_{REF} + VSDsat,\ V_{EB1} + |V_{TP}| + 2VSDsat\}\}} \quad \textit{2.20}$$

The minimum value for the voltage supply in this circuit will be round 900mV.In this case, after the curvature compensation the circuit produced a V_{REF} of 635 mV, adding the 50 mV equivalent of the VSDsat, the obtained value would be 685 mV. As known, to supply a V_{EB1} a minimum of 700 mV is required, so adding the $|V_{TP}|$ and 2VSDsat the minimum of 900 mV are obtained for the voltage supply. The circuit performance is presented in table 2.1.

Table 2.1: Performance Summary of the Bandgap

Parameter	**Value**
Supply Voltage	1.2v
Technology	0.13 µm MOS
Power Consumption at 27℃	29.2 µV
Reference voltage at 27℃	634.93 mV
TC (-40℃<T <125℃)	7.93 ppm
Minimum Operating Voltage	800mV
Gain and phase margin	85dB , 80℃

2.3.2 Voltage Reference Circuit Consisting of Subthreshold MOSFETs

A new approach appeared in the last years, the idea is to develop a bandgap voltage reference circuit without resistors or bipolar transistors. The main idea is to balance the VGS forming the CTAT voltage with VSG formed by the PTAT voltage. The circuit is divided in 2 parts, the part of the current source sub circuit and a bias voltage sub circuit.

Table 2.2: Performance Summary of the Bandgap

Parameter	**value**
Supply Voltage	>1.1v
Technology	0.16 µm MOS
Current Supply at 27°C	1.4 µA
Reference voltage at 27°C	944 mV
TC (-45°C< T <135°C)	30 ppm/°C
Area	0.0025mm^2

The current source circuit is a self-biasing circuit that uses a PMOS resistor instead of resistors. This part also generates the current IP. The part of the bias voltage circuit is composed by the transistor M4 and 2 coupled pairs (M3-M6 and M5-M7). All MOSFETs are in subthreshold region, excepting MR1 that operates in strong-inversion. This circuit combines 2 PTAT voltages with 2 CTAT voltages, as demonstrated in eq.2.21

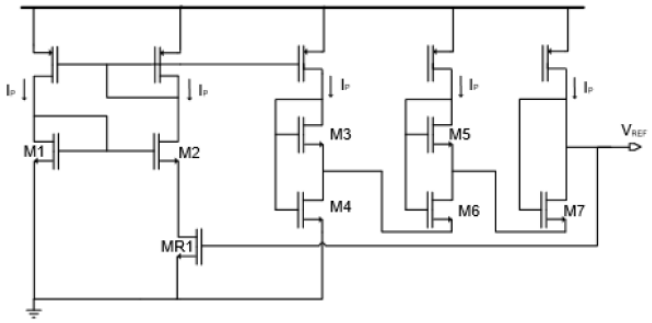


Figure 2.11: Schematic of Reference voltage

$$V_{REF} = V_{GS4} - V_{GS3} + V_{GS6} - V_{GS5} + V_{GS7}$$

$$= V_{GS4} + \eta V_T ln\left(\frac{2K_3K_5}{K_6K_7}\right) \qquad 2.21$$

$$= V_{TH} + \eta V_T ln\left(\frac{3I_P}{K_4I_O}\right) + \eta V_T ln\left(\frac{2K_3K_5}{K_6K_7}\right)$$

As known, the thermal voltage V_T has a positive TC and the threshold voltage V_{TH} has a negative TC . Adjusting the sizes of transistors is it possible to obtain a stable voltage reference. As known, VGS has coefficients with a worst linearity than VBE, consequently the TC error of the circuit should be larger, instead of this VGS cancels each other non-linearity factors. Although the circuit works with supply voltages below1V, as shown in fig. 2.12, in the table is represented a minimum voltage supply of 1.4 V. Probably with a shorter voltage supply the TC error will be larger, in table Tabletab3 is represented the circuit performance.

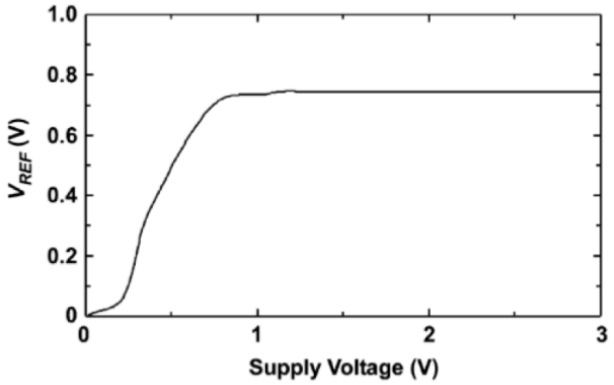


Figure 2.12: Voltage reference as a function of voltage supply

Table 2.2: Performance Summary of the Bandgap

Parameter	**Value**
Supply Voltage	1.4-3v
Technology	0.35µm CMOS
Current Supply at 27°C	0.3µW
Reference voltage at 27°C	745 mV
TC (20°C< T <80°C)	7 ppm/°C
PSRR	-45dB (@100Hz)
Area	$0.055mm^2$

Chapter 3

EXISTING TECHNIQUES

Traditional Bandgap Reference circuit were using BJT because gm/Ic of BJT is larger than gm/Id of MOSFET but the problem with the BJT is that they act like parasites that mess up with switching circuits by latching up, also CMOS dissipates less power compared to BJT also cascade current mirror circuits made from MOSFET are far better than with BJT and hence BJT doesn't satisfy the development of ultra-low power and high performance application.

Some the circuits were able to provide two reference output voltage but for that they need to have more than 1 start-up circuit and also current reference circuits but this make structure complex , and also consume too much area and high power consumption and hence it also doesn't satisfy the criteria for low power application.

In some circuit MOSFET used in sub-threshold conduction mode , sub-threshold region is used where Tx operation is around the threshold voltage i.e bit below threshold voltage . This region is useful for system that should at low voltage around 1v. It increases the Transconductance of MOSFET and helps in getting high gain, Although it satisfy the criteria for low power but it limits the PSRR which is not good.

The proposed works of Ref 1, 2 and 5 have used concept of

temperature compensation technique for low TC's. Most of Them follow first order or 2nd order and also High order Temperature compensation technique. Some of them also use ATC(adjusted temperature curvature) which also helps to reduce temperature drift and to enhance the voltage of band gap reference circuit. But ATC makes circuit complex which increases area. Using 2nd order technique helps to stabilize the temperature.

MOSFET should work in sub-threshold (Ref 7) region . It helps to reduce in supply voltage as well as power dissipation .But along with the pros it also has some cons which applies only high precision circuits only. As discussed in Ref 1,7sub- threshold region problem is the variation of threshold voltage, this result in variation of ±15% in reference voltage. To solve this problem, a new sub-threshold band gap voltage reference circuit is proposed, In which they do not use same body bias voltage and apply current trimming technique for the purpose to dynamically control the threshold voltage of MOS. This compensation technique has reduced the deviation of the reference voltage by 0.6%, and 3.8% without trimming. since I am not going for implantable medical application hence sub-threshold region is good for this kind of application. For any band gap reference circuit PSRR value should be high for this purpose Ref 2and 6 have used current mirror circuits. The purpose of resistance of high value is to achieve low current in sub-threshold region but the problem with the high value resistance is that it increases the

area of the circuit and make unsuitable for ultra –low power large scale integrated circuits (Ref 4). Researchers have solved this problem by the development of a band gap reference circuits without the use of resistor as well as BJT.

Finally we need a circuit we need which should a qualities like low power consumption, small size, Low Temperature coefficient and high PSRR.

The proposed circuit consists of start-up circuit, cascade current mirror circuit which is acting as current reference circuit and voltage reference circuit.

Chapter 4

CIRCUIT DESIGN & WORKING

CIRCUIT-1

The proposed dual-output voltage reference circuit is illustrated in fig 4.1. It consists of two parts, namely a start-up circuit and a core dual-output voltage reference circuit, and transistors of dual-output voltage reference circuit are operating in sub-threshold region, except transistors of

start-up circuit.

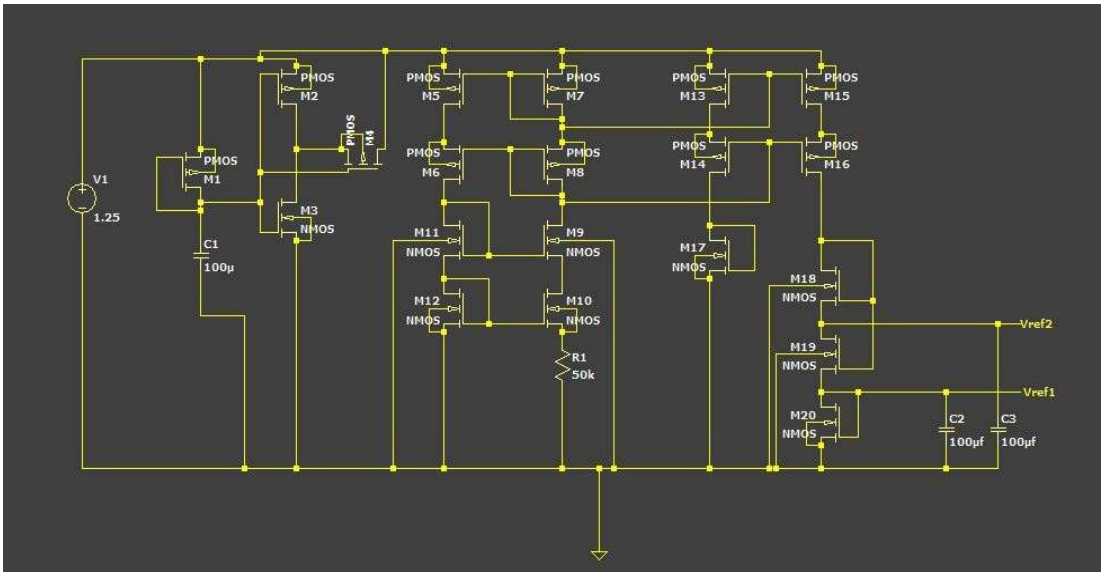


Figure 4.1: Proposed dual-output voltage reference circuit

4.1 Start-up Circuit

The start-up circuit is composed of M1, M2, M3, M4 and capacitor C_O. When the system works normally, it will turn-off the start-up circuit and can reduce power consumption. The start-up circuit is used to obtain start-up current and get rid of the degenerate bias points. The start-up circuit in the Bandgap reference circuit is used

to push the circuit from the undesired operating point to desired operating point. Once the circuit reaches the desired operating point, the start-up circuit automatically turns off, and doesn't interfere with the working of other parts of circuit.

4.2 Current Source Circuit

The Current source circuit is used to provide bias current for dual-output voltage reference circuit.

M5 and M6, operating in the sub-threshold region with the same aspect ratio, is a cascode current mirror. The bias current of the current source circuit is copied to the core dual voltage reference circuit through the cascode current mirror. The current, which is generated by the MOS operating in the sub-threshold region, is nano-ampere magnitude.

The current-voltage (I-V) characteristic of MOSFETs in the sub-threshold region is expressed as.

$$I_D = KI_O exp\left(\frac{V_{GS}-V_{TH}}{\eta V_T}\right)\left[1 - exp\left(-\frac{V_{DS}}{V_T}\right)\right] \qquad 4.1$$

I_D is the drain-current , K is the aspect ratio of the MOSFETs , V_{GS} is gate- source voltage ,V_{DS} is the drain – source voltage , V_{TH} is the threshold voltage , η is the sub-threshold slope factor , $I_o = \mu C_{OX}(\eta-1)V_T^2$is characteristic current , in which $V_T = k_BT/q$ is the thermal voltage , k_B is the Boltzmann constant , q is the elementary charge , $\mu=\mu_o(T/T_o)^m$ is the carrier mobility , in which μ_o is the electron

migration rate of MOSFETs at room temperature , T_o is the absolute temperature , and m is the mobility temperature exponent.

When $V_{DS} > 4V_T$, the effect of V_{DS} can be ignored, and Equation (1) is simplified as Equation (2).

$$I_D = KI_O exp\left(\frac{V_{GS}-V_{TH}}{\eta V_T}\right) \quad 4.2$$

VGS in the subthreshold region can be expressed as Equation (4.3).

$$V_{GS} = V_{TH} + \eta V_T ln\left(\frac{I_D}{KI_O}\right) \quad 4.3$$

In Figure 1, the current source circuit current ID is obtained by R1, M11 and M12, and can be expressed as Equation (4.4).

$$I_D = \frac{V_{GSM11}(T) - V_{GSM12}(T)}{R_1}$$

$$= \frac{V_{TH}+\eta V_T ln\left(\frac{I_D}{K_{11}I_O}\right)-V_{TH}-\eta V_T ln\left(\frac{I_D}{K_{12}I_O}\right)}{R_1} \quad 4.4$$

$$= \frac{\eta V_T}{R_1} ln \frac{K_{12}}{K_{11}}$$

$$= \frac{\eta k_B T}{R_1 q} ln \frac{K_{12}}{K_{11}}$$

From the above equation, the relationship between the current source circuit current I_D and the temperature can be expressed as Equation (4.5).

$$\frac{\partial I_D}{\partial T} = \frac{\eta k_B}{R_1 q} ln \frac{K_{12}}{K_{11}} \quad 4.5$$

Carrier I_D is copied from current source circuit to voltage reference circuit by setting a proper aspect ratio of the current mirror; a bias current is provided for M13-M20 in voltage reference circuit which finally produces two output from the respective references circuit . To filter this reference, an external capacitor C1 and C2 is used.

Table 4.1- Device size of the proposed circuit-1.

Transistor	W/L (µm/µm)	Transistor	W/L (µm/µm)
M1	0.42/0.42	M12	9/3
M2	0.42/0.42	M13	10/1
M3	0.42/0.42	M14	10/1
M4	0.42/0.42	M15	10/1
M5	2*10/2	M16	10/1
M6	2*10/2	M17	5.5/2
M7	2*10/2	M18	1/20
M8	2*10/2	M19	1/5
M9	2*10/2	M20	20/1
M10	15/4	RESISTANCE	(KΩ)
M11	2*10/2	R1	50

CIRCUIT- 2

The proposed CMOS sub-bandgap voltage reference circuit is illustrated in fig 4.1. It consists of two parts, namely a start-up circuit and a BGR core circuit.

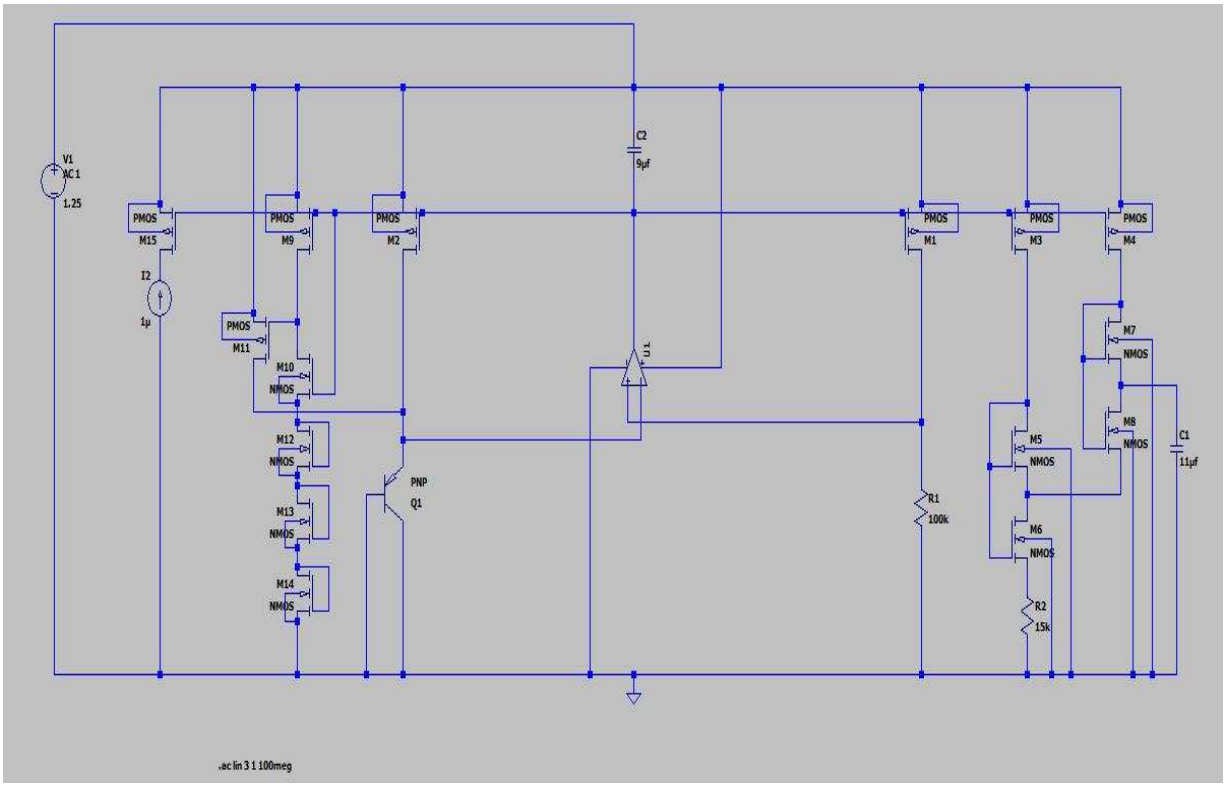


Figure 4.2- proposed CMOS sub-bandgap voltage reference circuit

The start-up circuit is composed of MS1, MS2, MS3, MS4, MS5, MS6 and capacitor C_O. When the system works normally, it will turn-off the start-up circuit and can reduce power consumption. The start-up circuit is used to obtain start-up current and get rid of the degenerate bias points. The start-up circuit in the Bandgap

reference circuit is used to push the circuit from the undesired operating point to desired operating point. Once the circuit reaches the desired operating point, the start-up circuit automatically turns off, and doesn't interfere with the working of other parts of circuit.

In order to generate a bandgap reference circuit having a nominally zero TC, two voltage quantities inside the bandgap reference circuit need to have opposite TC's so that they will cancel each other with proper weighting/ratio.

The proposed design employs MOS transistors working in subthreshold regions to achieve low voltage and low power operations. The proposed CTAT circuit consists of a vertical PNP BJT and two resistors to reduce the power. The improved PTAT circuit is made up by two cascaded sub-PTAT circuits with subthreshold transistors to reduce the power consumption without consuming large chip area.

Table 4.2 - Device size of the proposed circuit-2.

Transistor	W/L (µm/µm)	Device	W/L (µm/µm)
M1	4/10	MS4	2/10
M2	2*4/10	MS5	2/10
M3	4/10	MS6	2/10
M4	4/10	MA1	4*2/10
M5	1/18	MA2	2*4/4
M6	32*1/12	MA3	2*4/4
M7	1/12	MA4	4*2/10
M8	17*1/12	MA5	4*2/10
M9	1/12	MA6	6/8
MS1	4*4/1	MA8	6/8
MS2	2/8	MA9	4/8

Chapter 5

SIMULATION RESULTS

CIRCUIT-1

The proposed dual-output voltage reference circuit was designed in LTspiceXVII 0.18-µm CMOS. To evaluate the performance of the proposed voltage reference and validate the design procedure, a series of simulations was carried out with the aid of LTspice simulator 0.18-µm Mixed Signal/RF technology. Using the device's mismatch model, Monte Carlo simulation was run over a set of 500 samples on a typical process corner and at room temperature. The results are illustrated in Figure 5.1. The mean values of the dual-output voltages Vref1 and Vref2 were 281.28 mV & 180mV respectively.

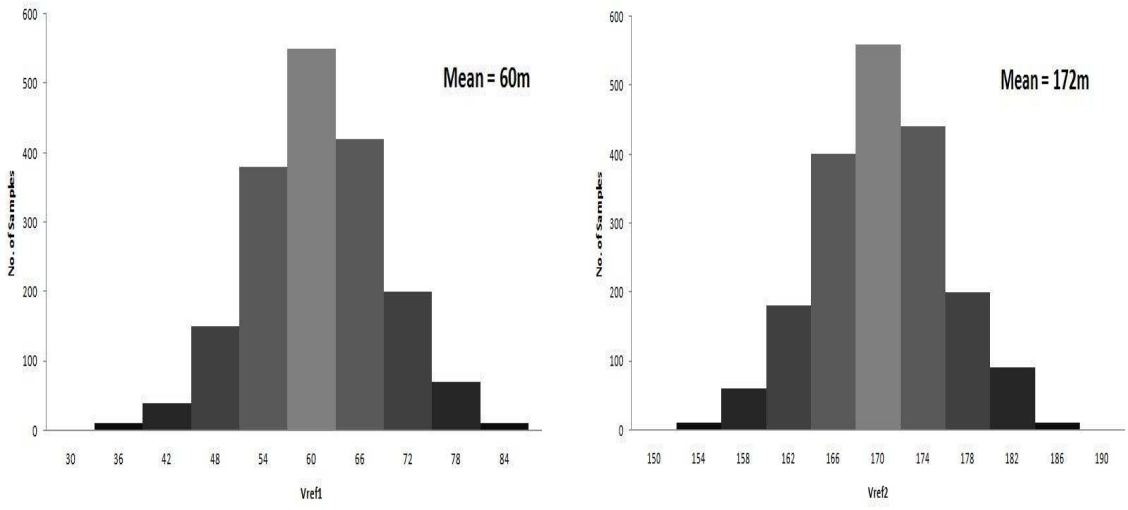
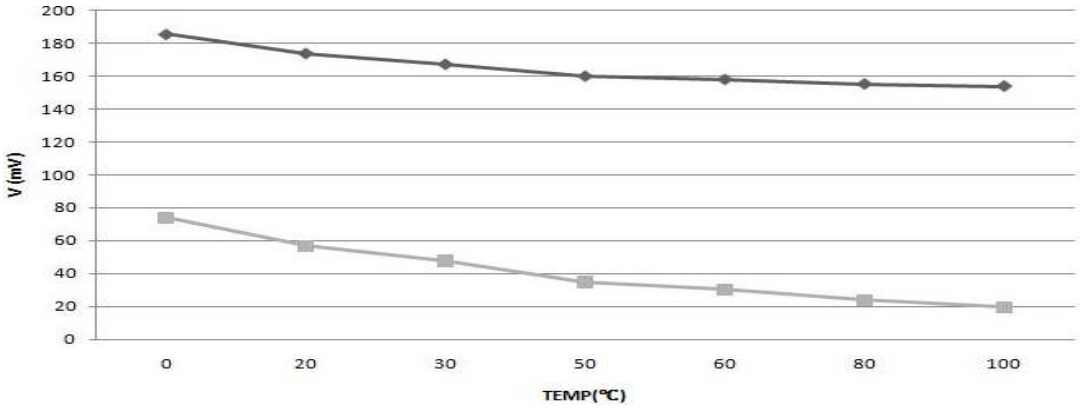


Figure 5.1: Monte Carlo simulation of output voltages for 2000 samples: (**a**) simulation *Vref1*; and (**b**) simulation *Vref2*.

A series of simulations was done to verify the performance of the

proposed voltage reference. Figures 5.2and 5.3show the simulation results in different process corners.



(a)

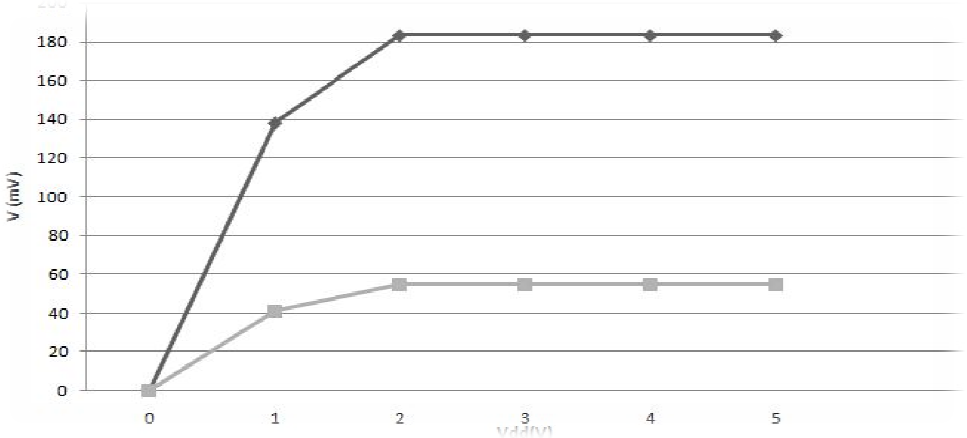
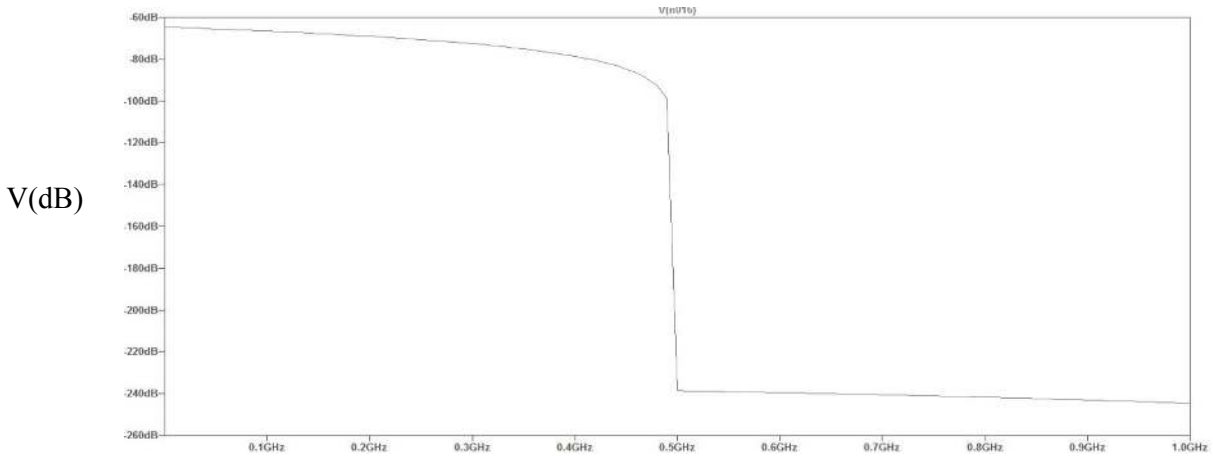
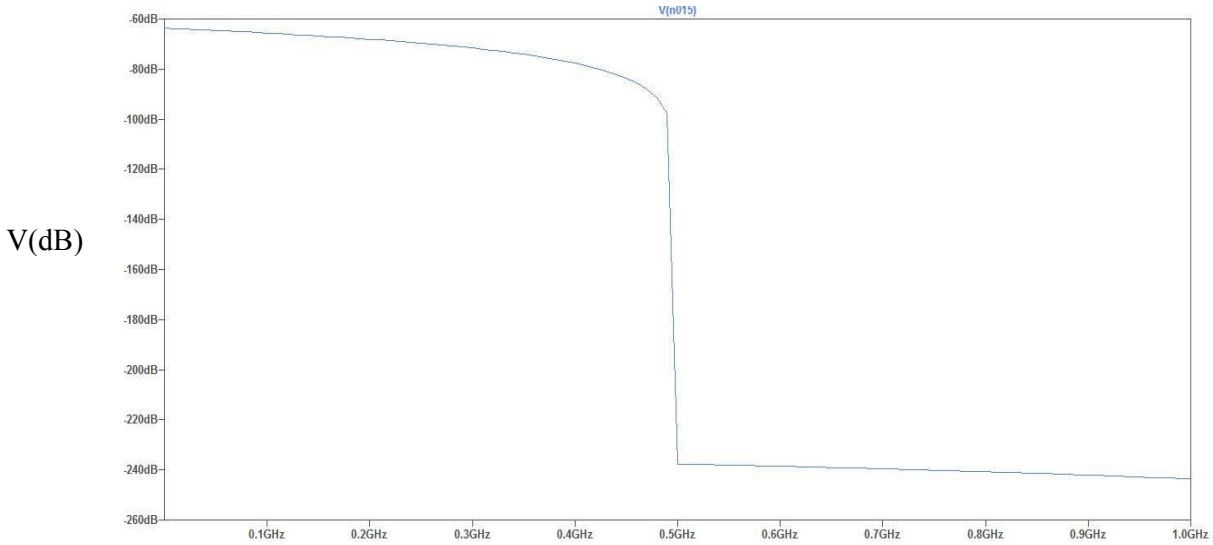


Figure 5.2: Simulation of *Vref1 and Vref2* on different process corners:
(**a**) simulation TC (**b**) simulation LS;



(a)



(b)

Figure 5.3: Simulation of *Vref1 and Vref2* on different process corners:
(**a**) simulation PSRR of Vref1 (**b**) simulation of PSRR of Vref2;

CIRCUIT-2

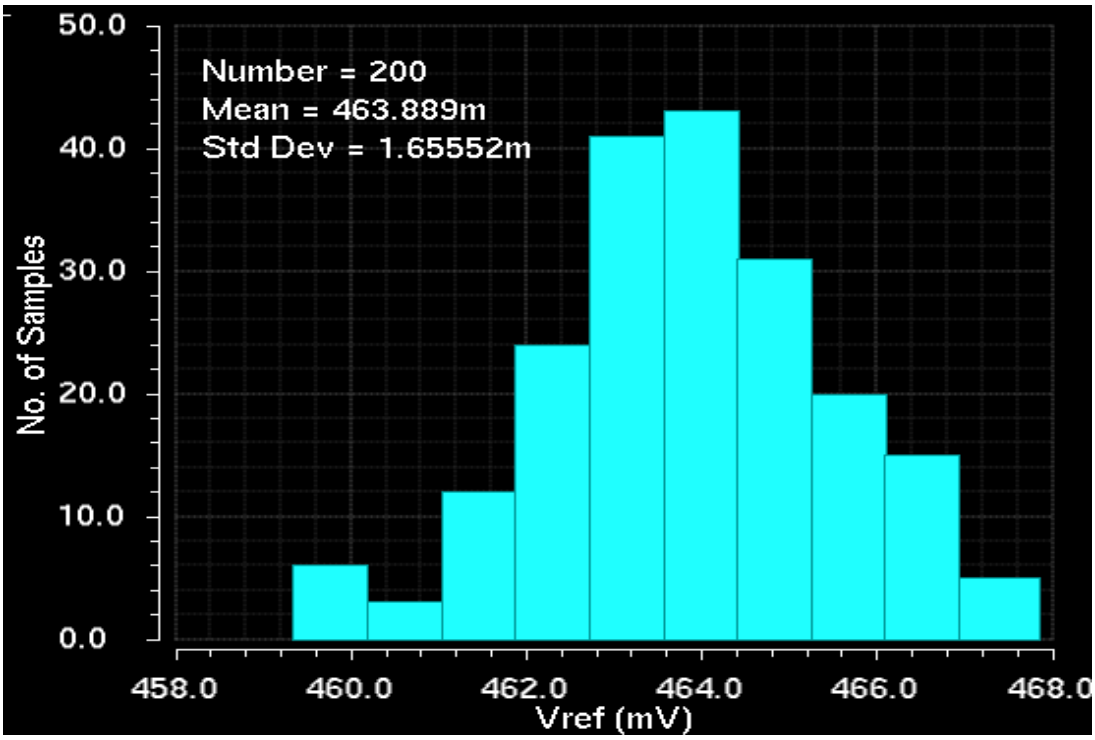


Figure 5.4: Monte Carlo simulation

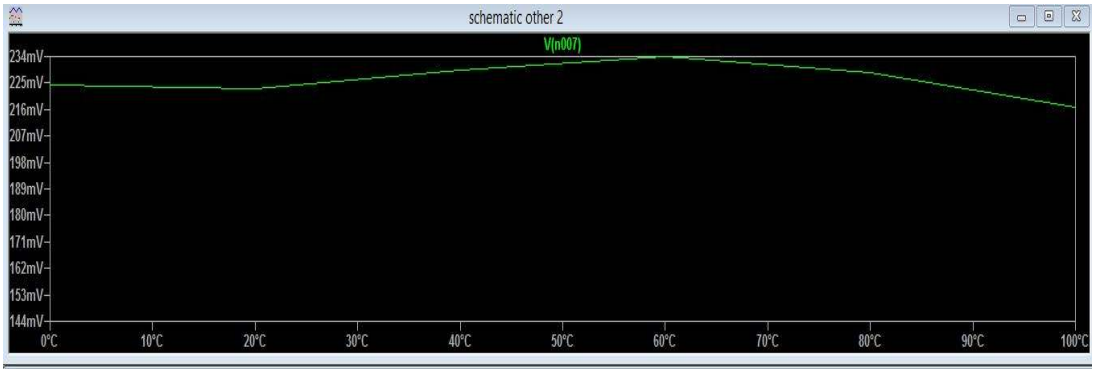


Figure 5.5 : Simulation of *TC*

Figure 5.6 - Simulation of *PSRR*

Chapter 6

SOFTWARE

LTspice is free Software computer software implementing a SPICE electronic circuit simulator, produced by semiconductor manufacturer Linear Technology, now part of Analog Devices. It is used in-house at Linear Technology for IC design, and the most widely distributed and used SPICE program in the industry. LTspice is not artificially crippled to limit its capabilities (no node limits, no component limits, no sub-circuit limits).

LTspice provides schematic capture to enter an electronic schematic for an electronic circuit, an enhanced SPICE type analog electronic circuit simulator, and a waveform viewer to show the results of the simulation. Circuit simulation analysis based on transient, noise, AC, DC, DC transfer function, DC operating point can be performed and plotted as well as Fourier analysis. Heat dissipation of components can be calculated and efficiency reports can also be generated. It has enhancements and specialized models to speed the simulation of switched-mode power supplies (SMPS) in DC-to-DC converters.

LTspice does not generate printed circuit board (PCB) layouts, but net-lists can be exported to layout programs. While LTspice does support simple logic gate simulation, it is not designed specifically for simulating logic circuits.

It is used by many users in fields including radio frequency electronics, power electronics, audio electronics, digital electronics, and other disciplines.

LTspice XVII

In 2016, LTspice XVII was released, and is currently the latest version. It is designed to run on 32-bit or 64-bit editions of Windows 7, 8, 8.1, 10, and macOS 10.9+

Summary of major changes from LTspice IV to LTspice XVII are:

- Add 64-bit executables.
- Add Unicode characters in schematics, net-lists, plot.
- Add device equations for IGBT, diode soft recovery, arbitrary state machine.
- Add user-defined symbol and library directory search path settings to the LTspice control panel.
- Add schematic thumbnail and preview support on Microsoft Windows.
- Add editors for most SPICE commands.
- Add multi-monitor support.

6.1 Commands for Simulation:

To draw V vs. Temp simulation

.step temp 0 100 20 .op

Type of sweep: Temperature

Nature of Sweep: Linear

Start value: 0℃

Stop value: 100℃

Increment: 20℃

.op: Dc operating point

To draw PSRR simulation

.ac lin 3 1 1000meg

Ac amplitude: 1v

Dc value: 1.25v

Analysis: Ac analysis

Type of Sweep: Linear

No of points: 3

Start freq: 1 End freq: 1000megHz

To draw LS simulation

.dc V1 0 5 1

Type of analysis: Dc analysis

Name of 1st source to sweep: V1

Type of sweep: linear

Start value: 0

Stop value: 5

Increment: 1

Chapter 7

APPLICATIONS AND ADVANTAGES

A bandgap voltage reference is a temperature independent voltage reference circuit widely used in integrated circuits. It produces a fixed (constant) voltage regardless of power supply variations, temperature changes and circuit loading from a device.

For, example, the accuracy of data converters depends on the precision of reference voltage, which makes the reference an important part of the system. Bandgap reference circuits are used to design the ICs of your phone, so that they remain temperature independent. The proposed Bandgap reference circuit is used for portable biomedical application. For eg.

Smart Health watches

Smart-watches allow users to perform tasks they normally do o their phones - read notifications, send simple messages, make phone calls , while also offering some of the exercise and health-tracking benefits of fitness tracker.

Wearable ECG monitor

The Move ECG is able to measure an electrocardiogram and send the reading to the user's doctor, as well as detect atrial fibrillation. It's also able to track pace, distance, and elevation, as well as automatic tracking for walking, running, swimming, and biking.

Wearable Blood Pressure Monitors

Heart-Guide is an oscillometric blood pressure monitor that can measure blood pressure and daily activity - like steps taken, distance traveled, and calories burned.

Biosensors

Biosensors are up and coming wearable medical devices that are radically different from wrist trackers and smart-watches. The Philips' wearable is a self-adhesive patch that allows patients to move around while collecting data on their movement, heart rate, respiratory rate, and temperature.

Chapter 8

CONCLUSIONS AND SCOPE FOR FUTURE WORK

The reference voltage Vref1 and Vref2 will be obtained through Monte carlo Simulation graph by taking samples around 400-500 and for each graph we will note down the value of Vref1 and Vref2 and at the end average of Vref1 and Vref2 will give expected output reference voltage with their variation coefficient.

The simulation results show that, at temperature ranging from 0to100℃, the TC's of output voltage s were 12.38ppm/℃ and 15.5ppm/℃, respectively. The mean LS was 0.05% under a supply voltage ranging from 0.9V to 3.1V at room temperature. The PSRRs of Vref1 and Vref2 at 1MHz were greater than−64 dB and−63 dB, respectively. The results of 500-point Monte Carlo simulation show that the output voltages 60mV and 172mV for circuit-1 and Vref=400mv for circuit-2. It was more suitable for low-power fields such as human body area networks, wearable medical devices and medical measurements, especially portable biomedical application.

Recommendation for future work

Any external parameters such as the effect of device mismatch on Output voltage need to be investigated on the real environment.

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APPENDIX A