Seventh Semester B.E. Degree Examination, July/August 2021
Advanced Computer Architecture

Time: 3 hrs.   Max. Marks:100

Note: *Answer any FIVE full questions.*

1   a. Define Computer Architecture. Explain seven ISA's of computer.   **(08 Marks)**
    b. Give a brief explanation about trends in power in integrated circuits and cost.   **(08 Marks)**
    c. Define the following terms: MTTR, MTTF, availability and FIT.   **(04 Marks)**

2   a. Discuss five basic stages of RISC instruction execution with neat block diagram.   **(08 Marks)**
    b. Define and list major hurdles of pipeline and illustrate data hazard with stall and without stall with example.   **(12 Marks)**

3   a. Explain in detail 3 different types of dependency.   **(10 Marks)**
    b. Discuss the methods used to reduce branch costs with prediction.   **(10 Marks)**

4   a. Explain the basic VLIW approach for exploiting instruction level parallelism using multiple issues.   **(08 Marks)**
    b. What are the key issues in implementing advanced speculation techniques? Explain in detail.   **(08 Marks)**
    c. Write a note on value predictors.   **(04 Marks)**

5   a. Explain the taxonomy of parallel architectures.   **(04 Marks)**
    b. Explain the basic structure of centralized shared memory architecture and distributed memory multiprocessor system.   **(10 Marks)**
    c. Define cache coherence and explain different possibilities when the memory system is coherend.   **(06 Marks)**

6   a. Explain the four memory hierarchy questions in detail.   **(08 Marks)**
    b. Discuss 3C's of cache miss.   **(04 Marks)**
    c. Discuss about the methods used to reduce miss penalty.   **(08 Marks)**

7   a. Explain the different methods used to increase the cache bandwidth.   **(10 Marks)**
    b. Discuss in detail compiler optimization to reduce miss rate.   **(10 Marks)**

8   a. Explain detecting and enhancing loop level parallelism for VLIW.   **(06 Marks)**
    b. Explain Intel-IA 64 architecture with neat diagram.   **(06 Marks)**
    c. Explain hardware support for exposing parallelism for VLIW and EPIC.   **(08 Marks)**

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