CBCS SCHEME

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17CS32

Third Semester B.E. Degree Examination, July/August 2021
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: *Answer any FIVE full questions.*

1 a. Explain the construction, working and characteristics of N-channel DE-MOSFET. **(10 Marks)**

b. List out the difference between JFET and MOSFET. **(05 Marks)**

c. Explain CMOS as an inverter. **(05 Marks)**

2 a. Explain the following performance parameters of op-amp :
(i) Bandwidth (ii) Slew rate (iii) CMRR **(06 Marks)**

b. With a neat circuit diagram and waveforms, explain the operation of astable multivibrator using 555 timer. **(08 Marks)**

c. With neat circuit diagram and waveform explain relaxation oscillator. **(06 Marks)**

3 a. What is logic Gate? Realize $Y = \overline{(A+B)} + \overline{C}$ using Nand gates only. **(05 Marks)**

b. Describe positive and Negative logic. List the equivalence between them. **(05 Marks)**

c. A digital system is to be designed in the months of year which is given input in bit form. The month of January is represented as '0000' and February as '0001' and so on. Output of the system is '1' corresponding to the input of the month containing 31 days, otherwise it is '0'. For this system of 4 variable (a, b, c, d) find the following :

(i) Give the truth table and Boolean expression in $\sum m$ and πM.

(ii) Simplify using K-Map.

(iii) Implement the simplified equation using Nand-Nand gates and NOR – NOR gates. **(10 Marks)**

4 a. Using Quine-McClusky method simplify the following Boolean equation:
$y = f(a,b,c,d) = \sum m(0,2,3,6,7,8,10,12,13)$ **(10 Marks)**

b. Define Hazard. Explain different types of Hazard. **(05 Marks)**

c. Explain the structure of verilog HDL. **(05 Marks)**

5 a. What is Multiplexer? Design 16-to-1 Mux using two 8-to-1 Mux and one 2-to-1 Mux. **(06 Marks)**

b. Implement Full adder using following data processing circuits : (i) 8-to-1 Mux (ii) 3-to-8 line decoder and multi-input OR gate. **(08 Marks)**

c. Draw PLA circuit and realize the following equations $x = f(a,b,c) = \sum m(1,4,6)$, $y = f(a,b,c) = \sum m(2,3)$ and $z = f(a,b,c) = \sum m(0,5,7)$. **(06 Marks)**

6 a. Realize $y = A'B + B'C' + ABC$ using 8-to-1 Mux. **(05 Marks)**

b. What is Magnitude comparator? Explain 1-bit comparator. Implement 1-bit comparator using 2-to-4 line decoder. **(08 Marks)**

c. With neat logic diagram, truth table and waveform explain positive edge-triggered JK flip-flop. **(07 Marks)**

7 a. With a neat logic diagram and truth table, explain the working of JK Master Slave flip-flop along with its implementation using Nand gates. **(10 Marks)**

b. Explain various representations of SR, D, JK flip-flop. **(10 Marks)**

8 a. Using negative edge triggered JK flip-flop draw logic diagram of 4-bit Serial In Serial Out (SISO) shift register. Explain how to shift binary number 1001 using state table and necessary waveform. **(10 Marks)**

b. Explain with neat logic diagram and state table a switched tail counter initialized with 0000 also explain how to decode the counter. **(08 Marks)**

c. How long will it take to shift an 8-bit number into serial? In parallel out shift register, if clock used is of 10 MHz. **(02 Marks)**

9 a. What is ripple counter? Explain 3-bit ripple counter with logic diagram truth table and waveforms. What is the clock frequency if the period of the waveform at Q_C is 24 μs. **(10 Marks)**

b. Design self correcting Mod-5 synchronous down counter for Q_C, Q_B, Q_A, using JK flip-flop. Assume all unused state leads to 100. **(10 Marks)**

10 a. What is Binary Ladder? Explain binary ladder with digital input of 1000. What is full-scale output voltage of 5-bit ladder if input levels are 0 = 0 V and 1 = +10V **(08 Marks)**

b. Explain 2-bit simultaneous A to D converter. **(08 Marks)**

c. Explain : (i) Steady state accuracy test. (ii) Monotonicity test. **(04 Marks)**

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