Scheme of Solution

Internal Assessment Test 2 – October 2019

Sub:	COMPUTER ORGANIZATION							Code:	18CS34
Date:	14/10/2019	Duration	90 mins	Max Marks:	50	Sem:	III	Branch:	**ISE**

Answer Any **FIVE FULL** Questions

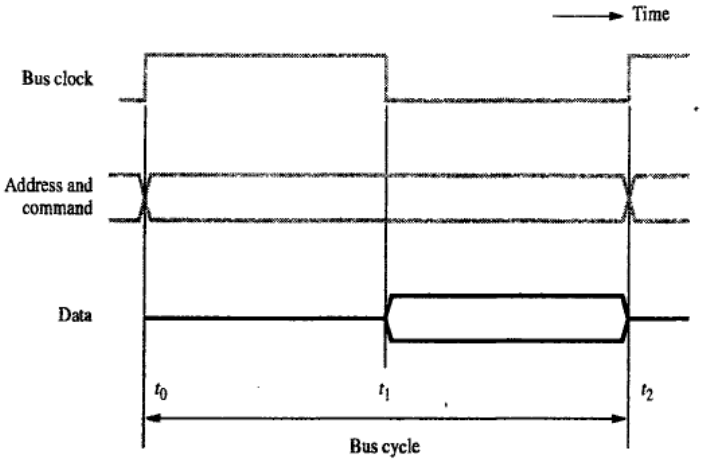
1(a) Discuss in detail about the following bus types with timing diagram

i) Synchronous Bus
ii) Asynchronous Bus

Synchronous Bus

All devices derive timing information from a common clock line
Equal time intervals – Bus cycle – High and Low signals

Example:



2 Marks

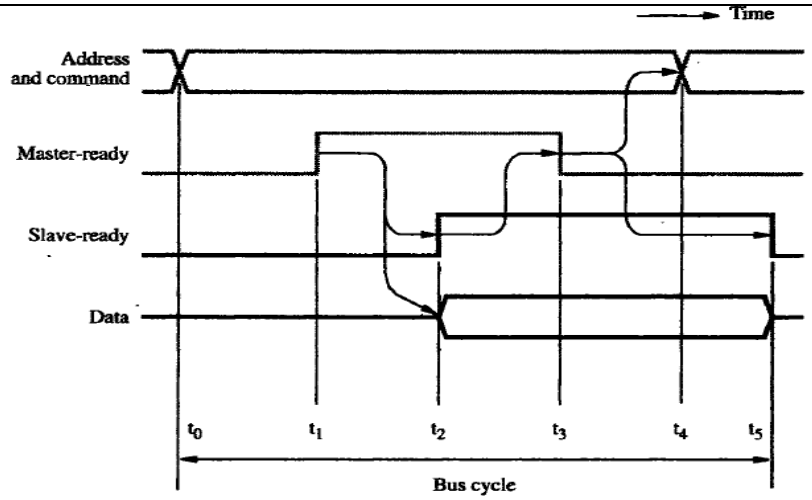
- Let consider the sequence of events during and input read operations
-At time t0 the master places the device address on address bus
-Read operation command given to control bus
-t0 to t1 allows the device to decode address and read operation to the slave
-after t1 slave places the requested input data on the data line after t1 to t2
-At the end of t2, the master 'Strobes' the data on the data lines
- Strobe – To capture the values of the data at a given instant and store them into buffer

3 Marks

Asynchronous Bus

- Alternate to control data transfer on the bus is based on Handshake Signals (Acknowledge) between Master and Slave
- Common clock is replace with master-ready and slave-ready signals

Example: Handshake control of data transfer during an input operation

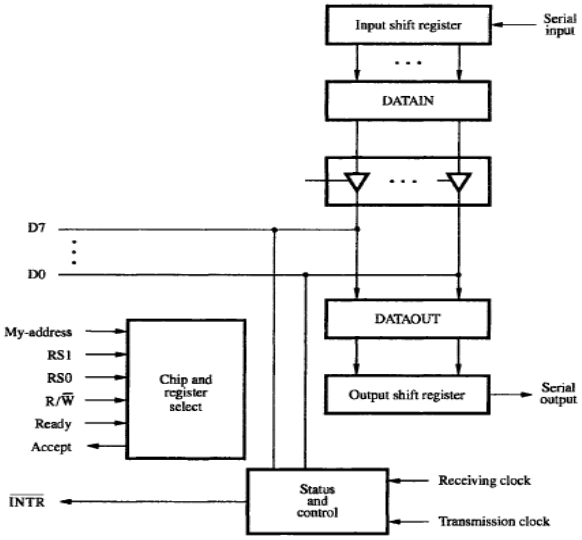


2 Marks

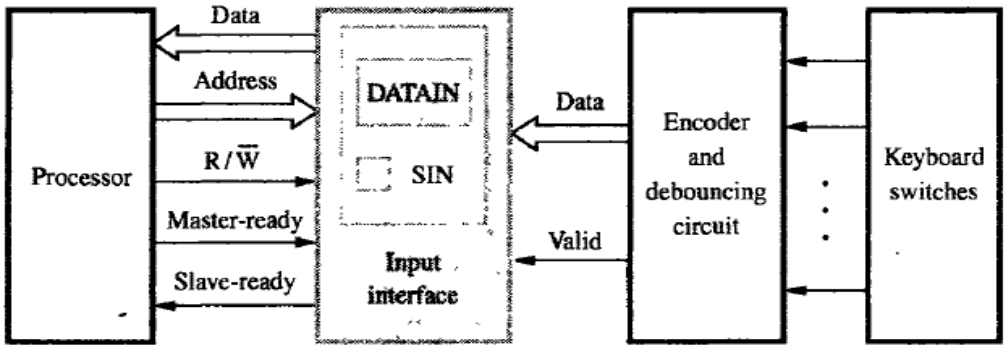
- t0 – The master places the address and command information on the bus
-t1- The master sets the mater-ready line to 1 to inform the data in I/O device and also slave-ready
- Skew – It occurs when two signals simultaneously transmitted from one source arrive at the destination at different times
- t2 – The selected slave decode the address and command information performs the required input operations in the data line
- t3 – The slave-ready signal arrives at the master, indicating that the input data are available on the bus.
- t4- the master removes the address and command information from the bus
- t5- When the device interface receives the 1 to 0 transition of the master-ready signal, it removes the data and the slave-ready signal from the bus. 3 Marks

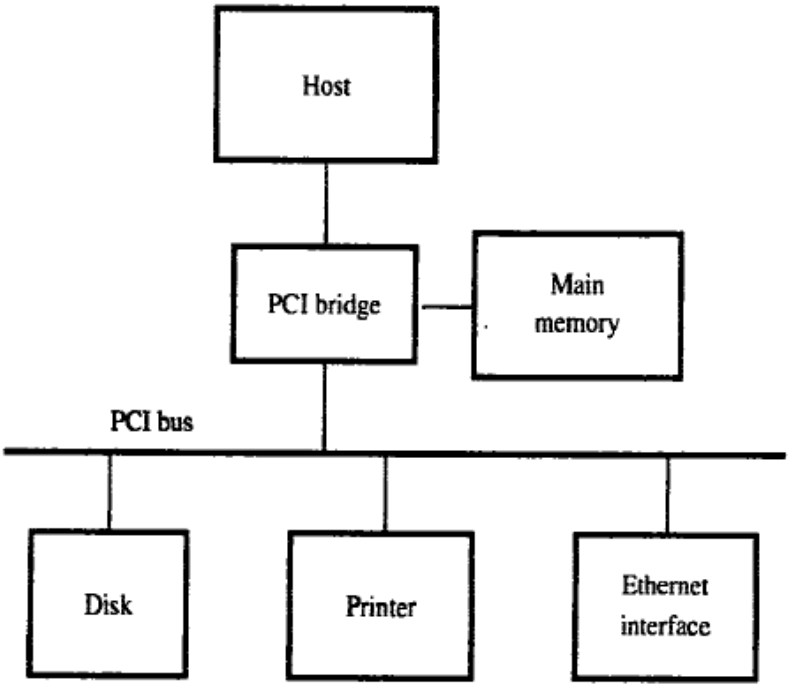
2(a) Provide suitable block diagram for serial interface and write its functionality.

When all 8 bits of the data have been received the contents of this shift register are loaded in parallel into the DATIN` register. Similarly, output data in the DATAOUT register are loaded into the output shift register, from which the bits are shifted out and send to the I/O device. 2 Marks



3 Marks

(b)	Draw and explain keyboard input interface with block diagram  2 Marks Keyboard bouncing need to be eliminated – Two ways – Simple de-bouncing circuit / Software approach (problem in longer waiting time) Key press – SIN = 1, processor reads the content of DATAIN then SIN=0 3 Marks
3(a)	Explain about PCI bus features, block diagram for host connection, Data transfer signals and Device configurations PCI bus features - It supports the functions found on a processor bus but in a standardized format that is independent of an particular processor - Device connected to the PCI bus appear to the processor as if they were connected directly to the processor bus. - Used in IBM PC's – Similar to 8-bit 80X86 processor – Later 16-bit bus on PC AT as ISA bus – 32-bit bus as in EISA bus. - It was developed as low cost, processor independent, high speed, plug and play - Data transfer – Used in burst mode of data transfer instead of single data - Supports read and write operation - Bus supports address space of memory, I/O and Configuration (plug-play) 2 Marks Draw a block diagram of PCI bus connected with host computer - Signal convention is like master and slave activity - Master holds address information on the bus until data transfer is completed - Slave store the address in its internal buffer - Address is needed on the bus for one clock cycle only, so it reduces cost of bus



3 Marks

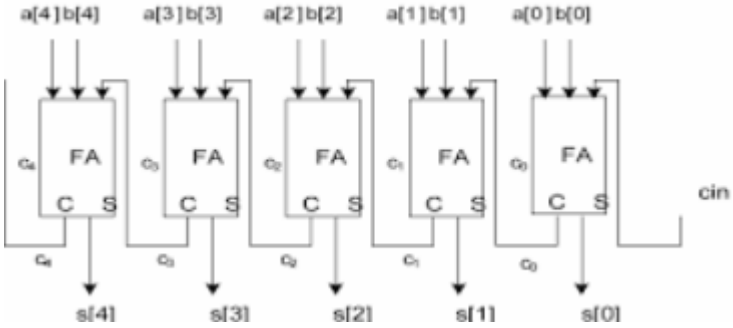
Data transfer signals

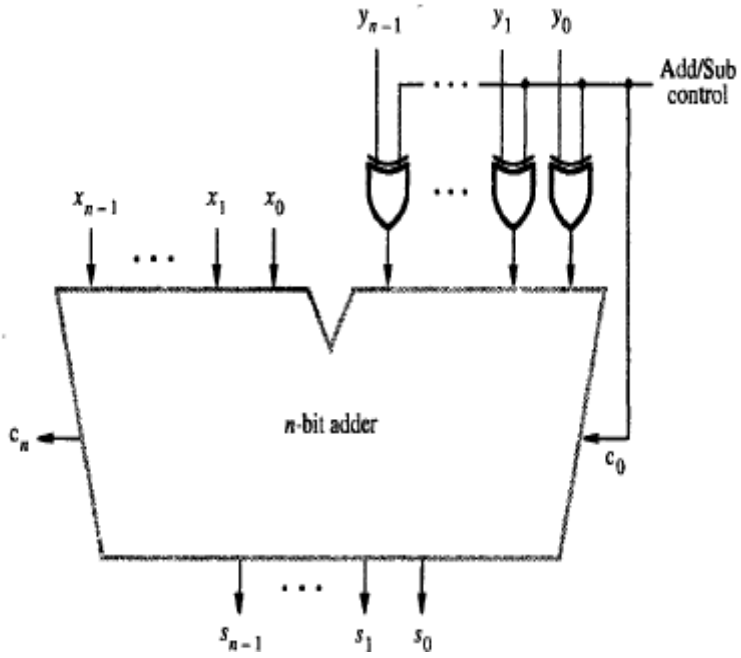
Name	Function
CLK	A 33-MHz or 66-MHz clock.
FRAME#	Sent by the initiator to indicate the duration of a transaction.
AD	32 address/data lines, which may be optionally increased to 64.
C/BE#	4 command/byte-enable lines (8 for a 64-bit bus).
IRDY#, TRDY#	Initiator-ready and Target-ready signals.
DEVSEL#	A response from the device indicating that it has recognized its address and is ready for a data transfer transaction.
IDSEL#	Initialization Device Select.

2 Marks

Device Configuration

- When I/O connected to a computer, several actions need to be configure
- Ex: Device, software, communication path, jumper, switches, speed etc..
- PCI simplifies all the above by configuration ROM
- ROM helps in power, reset, printer, keyboard (I/O), control, characteristics
- Each input signal called as Initialization Device Select (IDSEL#)

	- It connects 21- upper address lines (AD11 to AD31) - A device can be selected for a configuration operation by issuing a configuration command and an address in which the corresponding AS line is set to 1. Remaining 20 lines set to 0 - Lower address line (AD0 to AD10) used to specify the type of operation and to access the contents of the device configuration ROM - Configuration software scans all 21 locations in the configuration address space to identify which devices are present. - PCI contains 4 interrupt request lines, operating with either 5v or 3.3.v power supply - The user simply plugs in the interface board and turns on the power. The software does the rest. Thus, device is ready to use. 3 Marks
4(a)	Construct a block diagram for 5-bit ripple carry adder and brief its working principles.  3 Marks Explanation 2 Marks
(b)	Calculate the following using binary subtraction i) (-7) – (-5) ii) (+2) – (-3) i) -7 = 1001 (1001) -5 = 1011 (0101) - - - - - - - - - - -2 = 1110 1.5 Marks ii) +2 = 0010 (0010) -3 = 1101 (0011) - - - - - - - - - - -5 = 0101 1.5 Marks
5(a)	Implement a binary addition-subtraction logical network for the given data 10010 and 01101. Prove the results for addition and subtraction operation.



4 Marks

Proving

case 1: $x = 10010$ ($x_4 x_3 x_2 x_1 x_0$) $y = 01101$ ($y_4 y_3 y_2 y_1 y_0$) Add/sub Control $= 0$.

According to the above diagram if add/sub control = 0 means $C_0 = 0$.

The input coming to n bit adder is

$y = 01101$ XOR 00000 is $\begin{array}{r} 01101 \\ 00000 \\ \hline 01101 \end{array}$ $y' = y_4 y_3 y_2 y_1 y_0$

x and y' are added with carry as 0.

$$\begin{array}{r} 10010+ \\ 01101 \\ \hline 11111 \end{array}$$ will be the result of addition.

case 2: where Add/sub control = 1

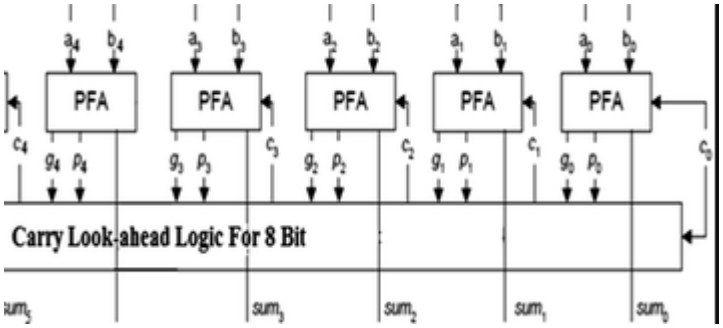
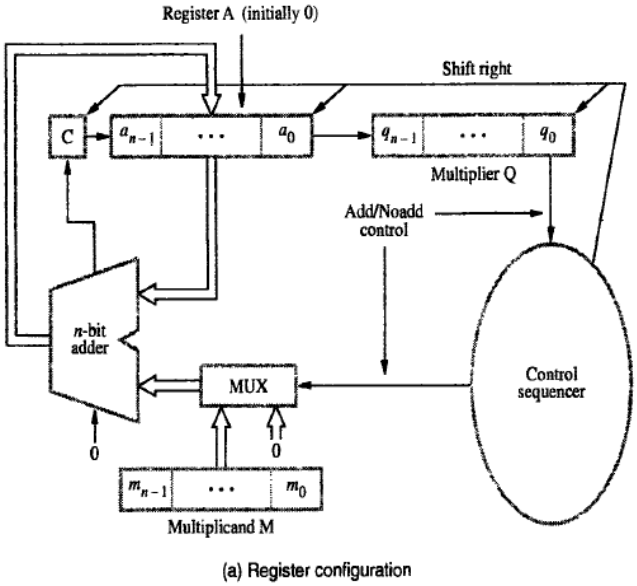
so $y' = 01101$ XOR 11111

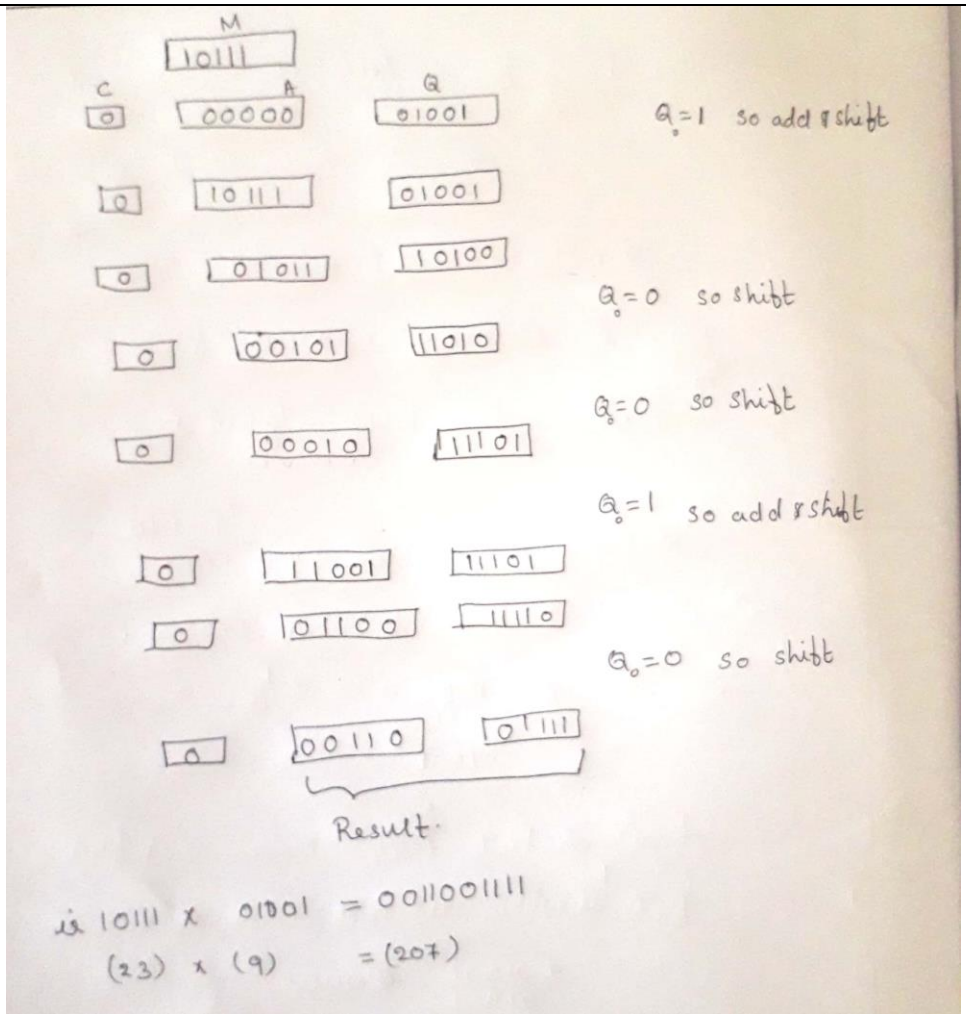
$$\begin{array}{r} 01101 \\ 11111 \\ \hline 10010 \end{array}$$ ($y_4 y_3 y_2 y_1 y_0$)

Add/sub control signal 1 means $C_0 = 1$ (initial carry is set).

The input coming to n bit adder is x, y' & carry $C_0 = 1$

$$\begin{array}{r} 10010 + \\ 10010 \\ \quad\ 1 \\ \hline 00101 \end{array}$$ with carry 1.

6(a)	Construct and explain a 5-bit carry lookahead adder along with proper equations and block diagram.  4 Marks Explanation 6 Marks
7(a)	Design a 5-bit register block diagram for sequential circuit binary multiplier. Prove the same with M=10111, Q=01001, C=0 and A=00000  (a) Register configuration



Prove

4 Marks

(a) Prove the following booth algorithm's functionality

i) Basic formula /Encoding scheme table for Booth algorithm

Multiplier		Version of multiplicand selected by bit i
Bit i	Bit $i-1$	
0	0	$0 \times M$
0	1	$+1 \times M$
1	0	$-1 \times M$
1	1	$0 \times M$

2 Marks

ii) Booth recoding for 0100010100

Ans: +1-1000-1+1-100

3 Marks

iii) Booth multiplication for + 12 and -14

Ans:

5 Marks