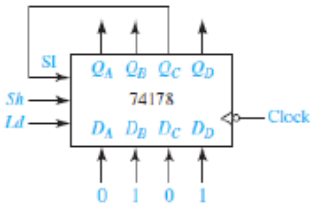
Scheme Of Evaluation

Internal Assessment Test 3 – Nov. 2019

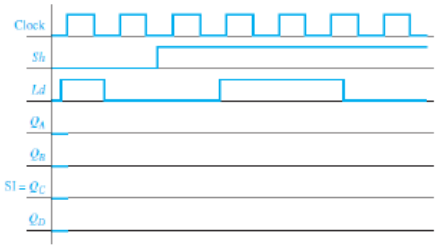
Sub:	Analog and Digital Electronics							**Code:**	18CS33
Date:	19/11/2019	Duration:	90mins	Max Marks:	50	**Sem:**	III	**Branch:**	ISE

Note: Answer Any Five Questions

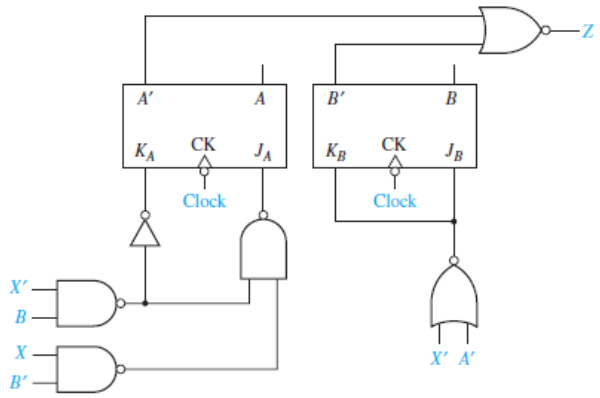
Question #		**Description**	**Marks Distribution**		**Max Marks**
1	a)	A 74178 shift register is described by the given table. All state changes occur on the 1-0 transition of the clock. The shift register is connected as shown. Complete the timing diagram.	1X4	4M	10 M



Sh	Ld	Q_A^+	Q_B^+	Q_C^+	Q_D^+
0	0	Q_A	Q_B	Q_C	Q_D
0	1	D_A	D_B	D_C	D_D
1	X	SI	Q_A	Q_B	Q_C



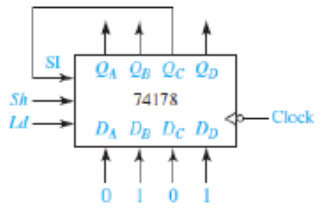
	b)	Design a parallel-in parallel-out left shift register which should shift left if *Sh* = 1, load if *Sh* = 0 and *Ld* = 1, and hold its state if *Sh* = *Ld* = 0. Draw the circuit using four D flip-flops and four 4-to-1 MUXes. Give the next-state equations for the flip-flops.	2 + 2+2	6M	
2 a)		An L-M flip-flop works as follows: If *LM* = 00, the next state of the flip-flop is 1. If *LM* = 01, the next state of the flip-flop is the same as the present state. If *LM* = 10, the next state of the flip-flop is the complement of the present state. If *LM* = 11, the next state of the flip-flop is 0. Complete the following table (use don't-cares when possible): Present State *Q* | Next State *Q*⁺ | *L* | *M* 0 | 0 0 | 1 1 | 0 1 | 1	1X4M	4M	10 M
2 b)		Using the in flip-flops which counts in the following sequence: *ABC* = 000, 100, 101, 111, 011, 001, 000, . . .		6M	
3		Design a 3-bit counter which counts in the sequence: 001, 011, 010, 110, 111, 101, 100, (repeat) 001, . . . (a) Use J-K flip-flops (b) Use S-R flip-flops In each case, what will happen if the counter is started in state 000?	5+5M	10M	10M

4	a)	Design a self-correcting mod-6 counter in which all unused states leads to state 000.	2.5X4M	10M	10 M
5	a)	Distinguish between synchronous and asynchronous counters.	3 x 2M	6M	10 M
	b)	Obtain the state graph for a serial adder. Is this a Moore machine or a Mealy machine?	3M+1M	4M	
6		For the following sequential circuit, find the next-state equation or map for each flip-flop. Is this a Mealy or Moore machine? Using these next-state equations or maps, construct a state table and state graph for the circuit.  	2M+1M+3.5M+3.5M	10M	10M
7	a)	Explain the working of a relaxation oscillator with necessary diagrams and waveforms.	2M+2M+2M	6M	10 M

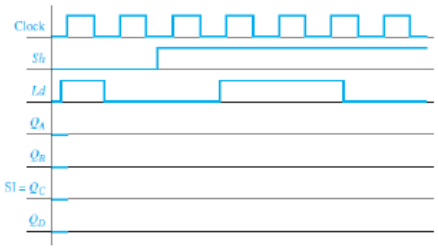
	b)	Design an astable multivibrator using 555 timer for a frequency of 2kHz and a duty cycle of (i) 25% (ii) 75%.	2M x 2	4M	
8	a)	What are the 2 types of analog filters? Distinguish between the 2.	2M+(2MX2)	6M	10 M
	b)	Explain the principle of operation of a photodiode with necessary diagrams.	2M+2M	4M	

Solution

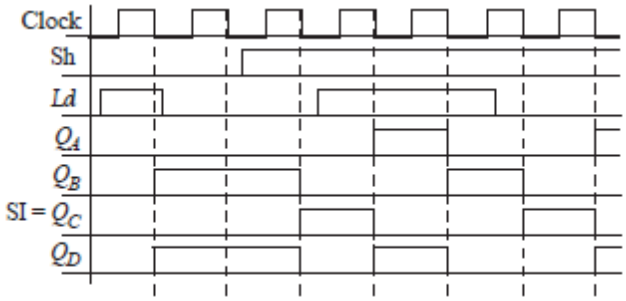
1 (a) A 74178 shift register is described by the given table. All state changes occur on the 1-0 transition of the clock. The shift register is connected as shown. Complete the timing diagram.



Sh	Ld	Q_A^+	Q_B^+	Q_C^+	Q_D^+
0	0	Q_A	Q_B	Q_C	Q_D
0	1	D_A	D_B	D_C	D_D
1	X	SI	Q_A	Q_B	Q_C



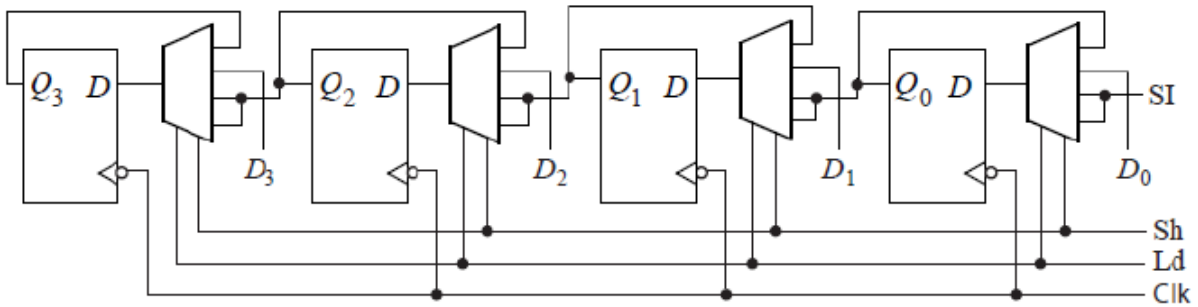
Answer:



(b) Design a parallel-in parallel-out left shift register which should shift left if $Sh = 1$, load if $Sh = 0$ and $Ld = 1$, and hold its state if $Sh = Ld = 0$. Draw the circuit using four D flip-flops and four 4-to-1 MUXes. Give the next-state equations for the flip-flops.

Answer:

When $ShLd = 00$, the MUX for flip-flop i selects Q_i to hold its state
When $ShLd = 01$, the MUX for flip-flop i selects D_i to load.
When $ShLd = 10$ or 11, the MUX for flip-flop i selects Q_i to shift left.

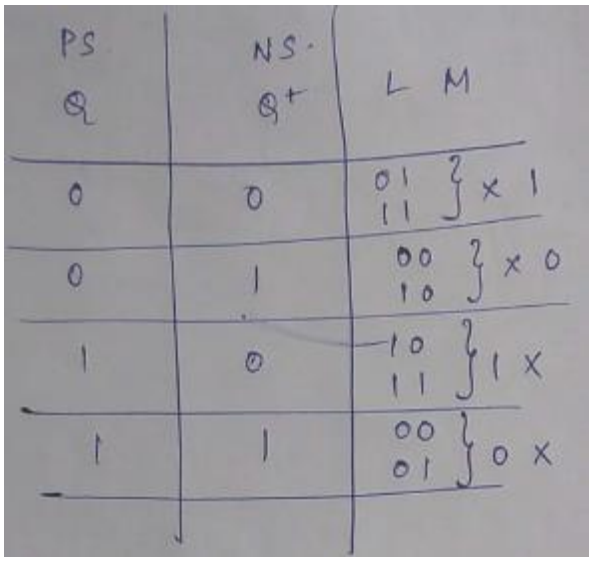


$Q_3^+ = Ld'Sh'Q_3 + LdSh'D_3 + ShQ_2$; $Q_2^+ = Ld'Sh'Q_2 + LdSh'D_2 + ShQ_1$; $Q_1^+ = Ld'Sh'Q_1 + LdSh'D_1 + ShQ_0$
$Q_0^+ = Ld'Sh'Q_0 + LdSh'D_0 + ShSI$

2 (a) An L-M flip-flop works as follows:
If $LM = 00$, the next state of the flip-flop is 1.
If $LM = 01$, the next state of the flip-flop is the same as the present state.
If $LM = 10$, the next state of the flip-flop is the complement of the present state.
If $LM = 11$, the next state of the flip-flop is 0.
Complete the following table (use don't-cares when possible):

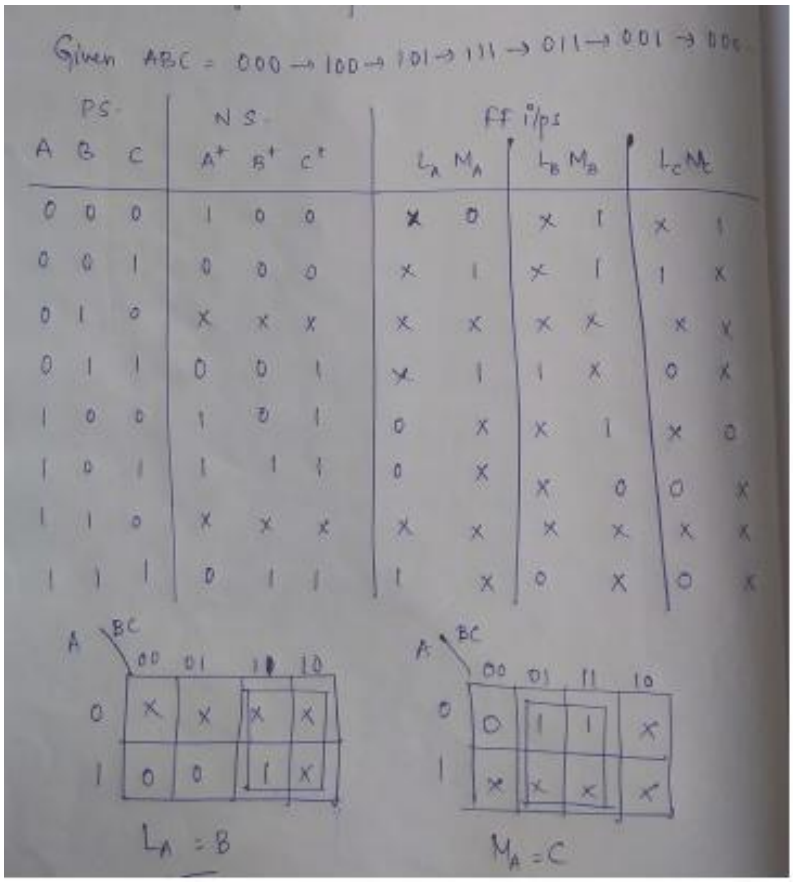
Present State Q	Next State Q^+	L	M
0	0		
0	1		
1	0		
1	1		

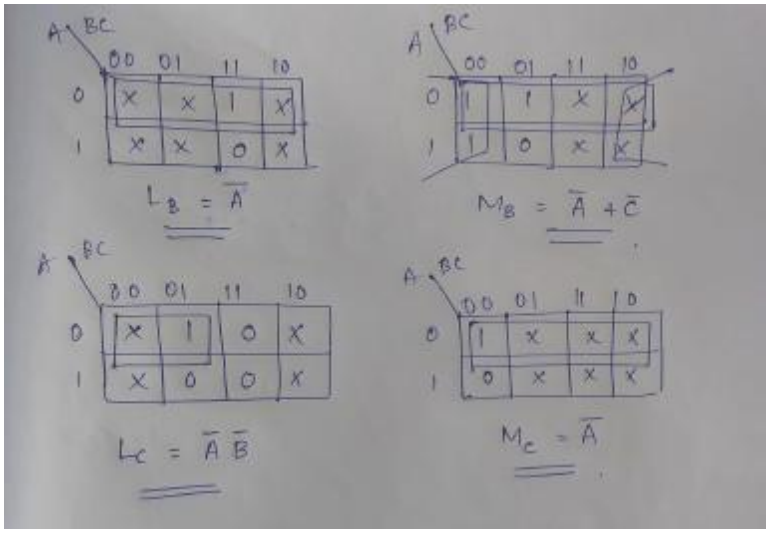
Answer:



(b) Using this table and Karnaugh maps, derive and minimize the input equations for a counter composed of three L-M flip-flops which counts in the following sequence:
ABC = 000, 100, 101, 111, 011, 001, 000, . . .

Answer:



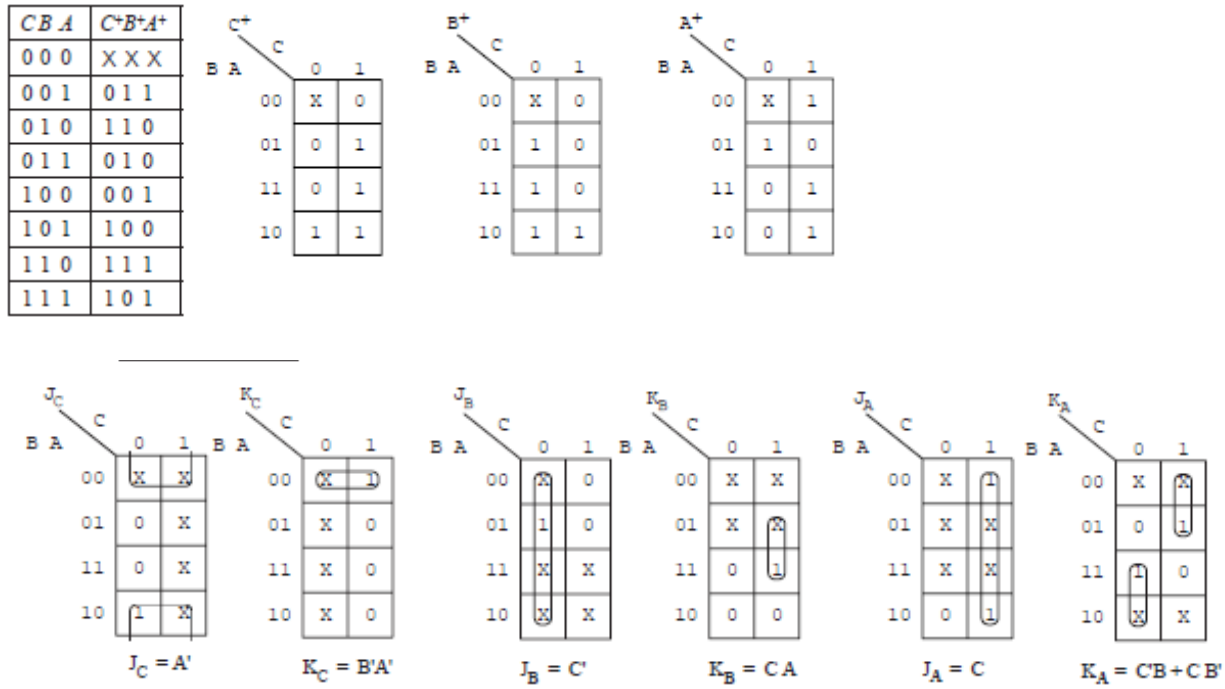


3 Design a 3-bit counter which counts in the sequence:
001, 011, 010, 110, 111, 101, 100, (repeat) 001, . . .
(a) Use J-K flip-flops
(b) Use S-R flip-flops
In each case, what will happen if the counter is started in state 000?

Answer:

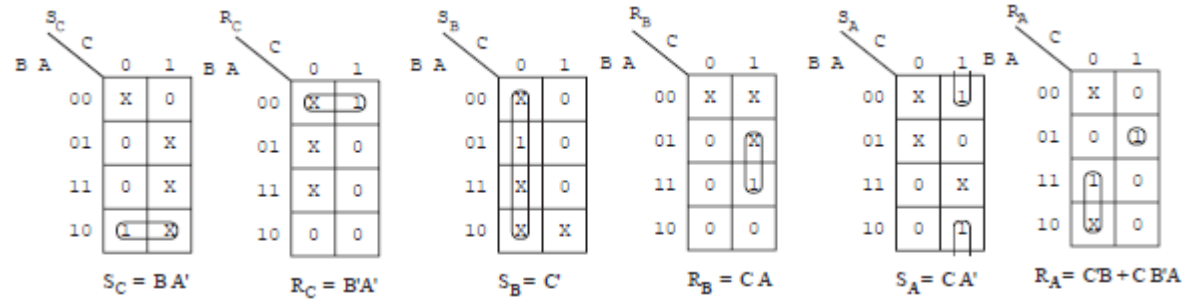
(a)

C B A	$C^+B^+A^+$
0 0 0	X X X
0 0 1	0 1 1
0 1 0	1 1 0
0 1 1	0 1 0
1 0 0	0 0 1
1 0 1	1 0 0
1 1 0	1 1 1
1 1 1	1 0 1



In state 000,
$J_C = A' = 1, K_C = B'A' = 1, C^+ = C' = 1$
$J_B = C' = 1, K_B = CA = 0, B^+ = 1$
$J_A = C = 0, K_A = CB' + C'B = 0, A^+ = A = 0$
So the next state is $C^+B^+A^+ = 110$

(b)



In state 000,

$S_C = BA' = 0, R_C = B'A' = 1, C^+ = 0$

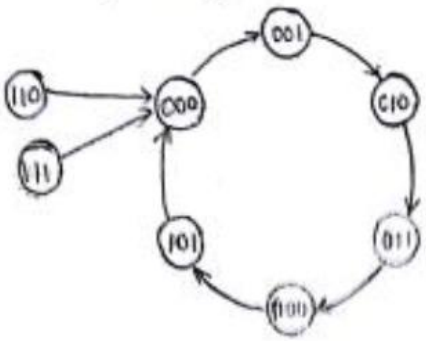
$S_B = C' = 1, R_B = CA = 0, B^+ = 1$

$S_A = CA' = 0, R_A = C'B + C'BA = 0, A^+ = A = 0$

So the next state is $C^+B^+A^+ = 010$

4 Design a self-correcting mod-6 counter in which all unused states leads to state 000.

Answer:



Present state			Next state			Flip-flop inputs		
A	B	C	A^+	B^+	C^+	D_A	D_B	D_C
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	0
0	1	0	0	1	1	0	1	1
0	1	1	1	0	0	1	0	0
1	0	0	1	0	1	1	0	1
1	0	1	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0

K-map simplification for flip-flop inputs :

For D_A

A \ BC	00	01	11	10
0	0	0	1	0
1	1	0	0	0

$D_A = A\bar{B}\bar{C} + \bar{A}BC$

For D_B

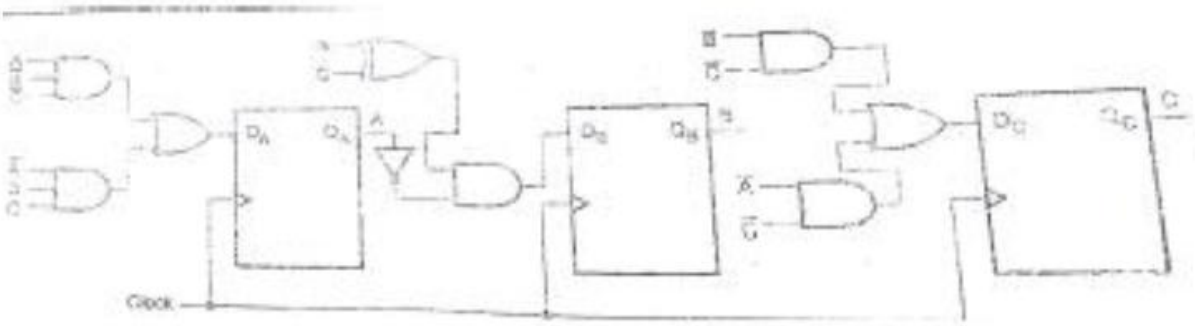
A \ BC	00	01	11	10
0	0	1	0	1
1	0	0	0	0

$D_B = \bar{A}\bar{B}C + \bar{A}B\bar{C}$
$= \bar{A}(\bar{B}C + B\bar{C})$
$= \bar{A}(B \oplus C)$

For D_C

A \ BC	00	01	11	10
0	1	0	0	1
1	1	0	0	0

$D_C = \bar{A}\bar{C} + \bar{B}\bar{C}$



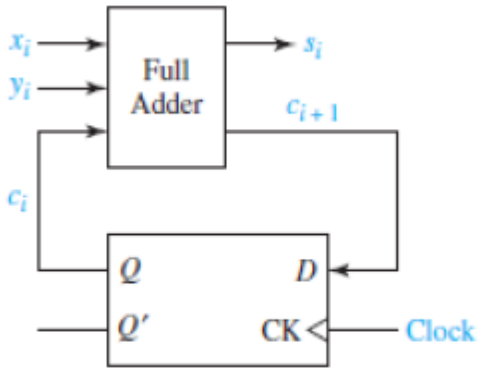
5 (a) Distinguish between synchronous and asynchronous counters.

Answer:

Synchronous	Asynchronous
* In synchronous counter, all flip-flops are triggered with same clock simultaneously.	* In Asynchronous, different flipflops are triggered with different clock not simultaneously.
* It is faster than asynchronous in operation	* It is slower in terms of operation
* It does not produce any decoding errors	* These counter produces decoding errors
* It is also called as serial counter	* It is also called as parallel counter
* Synchronous counter designing as well implementation are complex due to increasing of no of states	* Asynchronous counter designing as well as implementation is very easy.
* eg:- Ring counter	* eg:- Ripple up & ripple down counter

(b) Obtain the state graph for a serial adder. Is this a Moore machine or a Mealy machine?

Answer:

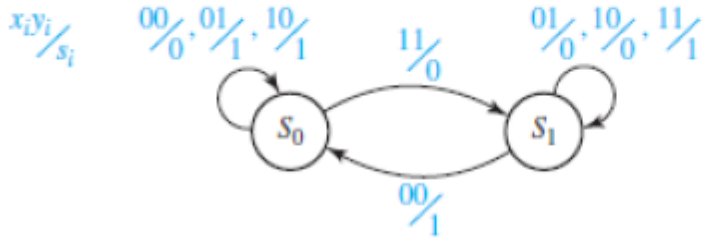


(a) With D flip-flop

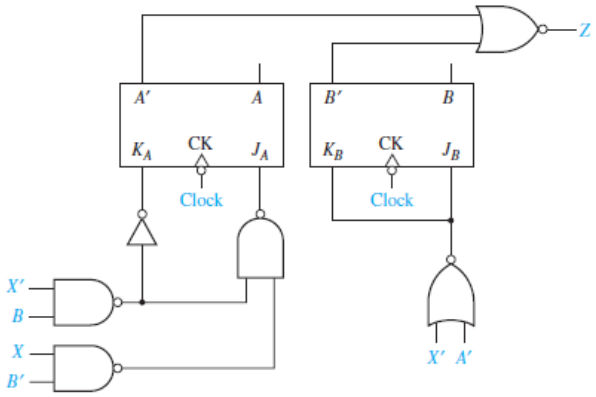
x_i	y_i	c_i	c_{i+1}	s_i
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

(b) Truth table

The serial adder is a Mealy machine with inputs x_i and y_i and output s_i. Using the truth table, we can construct a state graph for the serial adder. The two states represent a carry (c_i) of 0 and 1, respectively. From the table, c_i is the present state of the sequential circuit, and c_{i+1} is the next state. If we start in S_0 (no carry), and $x_i\,y_i = 11$, the output is $s_i = 0$ and the next state is S_1. This is indicated by the arrow going from state S_0 to S_1.



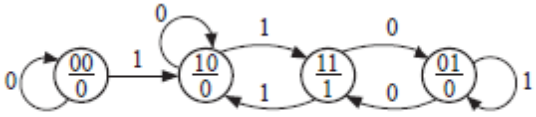
6 For the following sequential circuit, find the next-state equation or map for each flip-flop. Is this a Mealy or Moore machine? Using these next-state equations or maps, construct a state table and state graph for the circuit.



Answer:

$A^+ = AK_A' + A'J_A = A(B' + X) + A'(BX' + B'X)$
$B^+ = B'J_B + BK_B' = AB'X + B(A' + X')$
$Z = AB$

Present State AB	Next State (A^+B^+) $X=0$	$X=1$	Z
00	00	10	0
01	11	01	0
11	01	10	1
10	10	11	0



7 (a) Explain the working of a relaxation oscillator with necessary diagrams and waveforms.

Answer:

Relaxation oscillator is an non-linear electronic oscillator circuit that generates a continuous or respective non sinusoidal output signal in the form of rectangular wave, triangular wave or a sawtooth wave. The time period of non sinusoidal output depends on the charging time of the capacitor connected in the oscillator circuit. The relaxation oscillator basically contains a feedback loop that has a switching device in the form of transistor, relays, operational amplifiers, comparators, or a tunnel diode that charges a capacitor respectively through a resistance till it reaches a threshold level then discharges it again. Figure 7-71 shows the basic circuit of an op-amp based relaxation oscillator circuit.

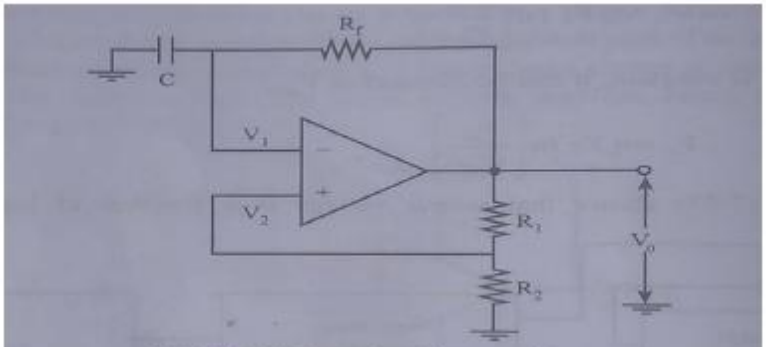


FIGURE 7-71: Relaxation oscillator

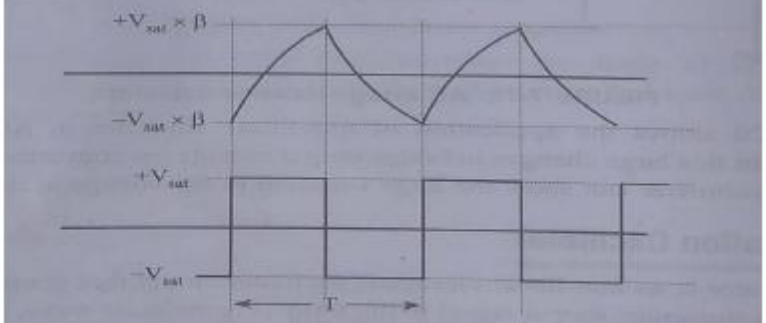


FIGURE 7-72: Waveforms of Relaxation oscillator

The circuit looks like a comparator and feedback resistor R_1 and R_2 form an inverting schmitt trigger. When the output voltage V_0 is at $+V_{sat}$ the feedback voltage which is known as upper threshold voltage V_{UT} and is given by,

$$V_{UT} = \frac{R_1.(+V_{sat})}{R_1 + R_2} \qquad (7\text{-}68)$$

Similarly when the output voltage is at $-V_{sat}$ the feedback voltage is known as lower threshold voltage V_{LT} and is given by,

$$V_{LT} = \frac{R_1(-V_{sat})}{R_1 + R_2} \qquad (7\text{-}69)$$

$$T = 2R_f C \ln\left[\frac{2R_1 + R_2}{R_2}\right]$$

equation (7-79) given the total time required for one oscillation.

(b) Design an astable multivibrator using 555 timer for a frequency of 2kHz and a duty cycle of (i) 25% (ii) 75%.

Answer:

Given: $f = 2\,\text{kHz}$ and $D = 0.25$

a) W.K.T $f = \dfrac{1.45}{(R_A + 2R_B)C} = 2\times10^3$

We know that

and $D = 0.25 = \dfrac{R_A + R_B}{R_A + 2R_B}$ (1)

Assuming $C = 0.1\ \mu\text{F}$

$$f = 2\times10^3 = \frac{1.45}{(R_A + 2R_B)\times0.1\times10^{-6}}$$

$$R_A + 2R_B = \frac{1.45}{0.1\times10^{-6}\times2\times10^3}$$

$R_A + 2R_B = 14.5\,\text{k}\Omega$ $7.25\,\text{k}\Omega$ (2)

On substituting in (1)

$$0.25 = \frac{R_A + R_B}{14.5\times10^3} \Rightarrow R_A + R_B = 3.65\,\text{k}$$ $1.8125\,\text{k}$ (3)

Solving (2) and (3)

$R_B = 10.875\,\text{k}\Omega$ $5.4375\,\text{k}\Omega$

and $R_A = 7.25\,\text{k}\Omega$ $3.625\,\text{k}\Omega$

b) for $f = 2\,\text{kHz}$ and $D = 75\%$

$$f = \frac{1.45}{(R_A + 2R_B)C}$$

$$D = 0.75 = \frac{R_A + R_B}{R_A + 2R_B}$$

Let us Assume $C = 0.1\ \mu\text{F}$

$$f = 2\times10^3 = \frac{1.45}{(R_A + 2R_B)C}$$

$$2\times10^3 = \frac{1.45}{(R_A + 2R_B)\times0.1\times10^{-6}}$$

$$R_A + 2R_B = \frac{1.45}{0.1\times10^{-6}\times2\times10^3} = 7.25\,\text{k}\Omega \quad (4)$$

Now $D = 0.75 = \dfrac{R_A + R_B}{R_A + 2R_B}$ (5)

Substituting (4) in (5)

0.75 ~~0.5~~ $= \dfrac{R_A + R_B}{7.25\times10^3}$

$R_A + R_B = 5.437\,\text{k}\Omega$

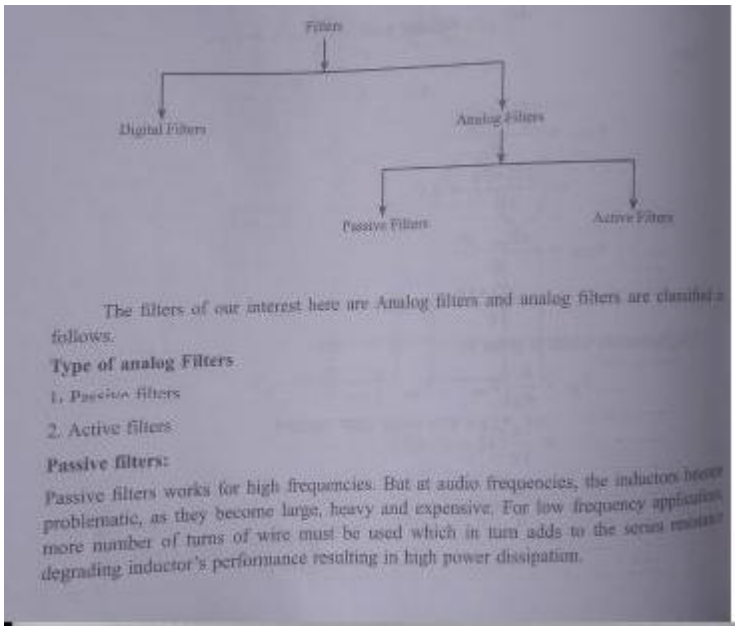
Solving (4) and (6) we get

$R_B = 1.82\,\text{k}\Omega$

$R_A = 3.61\,\text{k}\Omega$

8 (a) What are the 2 types of analog filters? Distinguish between the 2.

Answer:



The filters of our interest here are Analog filters and analog filters are classified as follows.

Type of analog Filters

1. Passive filters
2. Active filters

Passive filters:

Passive filters works for high frequencies. But at audio frequencies, the inductors become problematic, as they become large, heavy and expensive. For low frequency applications more number of turns of wire must be used which in turn adds to the series resistance degrading inductor's performance resulting in high power dissipation.

Active filters:

Active filters use op-amp as the active element, resistors and capacitors as passive elements. By enclosing a capacitor in the feedback loop, inductor less active filters can be obtained.

Now let us list down the differences between Active filters and Passive filters

TABLE 7-1: Comparison between active filter and passive filters

S.No	Active filters	Passive filters
1	Filters with components such as operational amplifiers, transistors or other active elements are known as active filters.	Filters with only components like R, L and C are known as passive filters
2	Active filters require an external power supply for operation. Capable of providing power gain.	Passive filters do not need an external power source for operation. Incapable of providing power gain.
3	Due to feedback loops used for regulating the active components may contribute to oscillation and noise.	Passive filters have a better stability and can withstand large currents.
4	Active filters have frequency limitations due to active elements.	Passive filters have no frequency limitation.
5	Active filter circuits are more compact and less heavy and operate with high speed	Due to presence of inductors, Passive filters are bulky/heavy in nature, they consume more power and operate with low speed
6	Can be fabricated in IC form and mass production making it cheaper.	Difficult to fabricate in IC form and usually designed using discrete components.

(b) Explain the principle of operation of photodiode with necessary diagrams.

Answer:

A photodiode is a light detector semiconductor device that converts light energy into electric current or voltage depending on the mode of operation.

Working Principle:

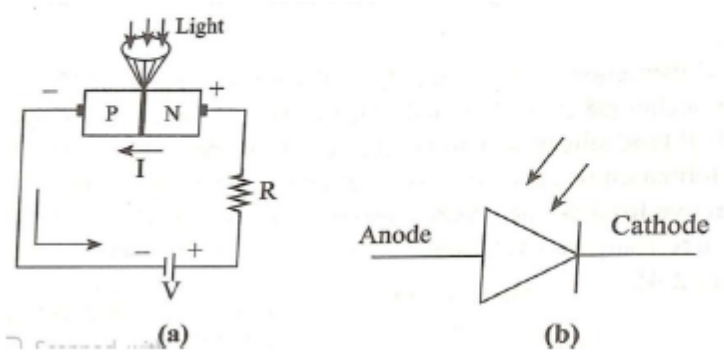


Figure (b) shows the symbol of photodiode.

The junction of photodiode is illuminated by a light source, that is, photons strike the junction surface. These photons impart their energy in the form of light to the junction. Due to this, the electrons present in the valence band get excited and move to the conduction band. This leaves positively charged holes in the valence band, thereby producing electron-hole pairs in the depletion layer. From these electron-hole pairs, electrons get attracted and move towards the positive potential on the cathode and the holes get attracted and move towards the negative potential on the anode. This constitutes a flow of current in a direction opposite to the direction of electron-flow. This current is termed as photocurrent. Thus photodiode converts light energy into electrical energy.