Modified.

CBCS SCHEME

USN

17EE35

Third Semester B.E. Degree Examination, Dec.2018/Jan.2019

Digital System Design

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Define canonical minterm form and canonical maxterm form. **(05 Marks)**

b. Compare between prime implicant and essential prime implecant. Indentify all the prime implecants and essential prime implecants of the following functions using k-map : $f(a, b, c, d) = \pi_M (0, 2, 3, 8, 9, 10, 12, 14)$. **(07 Marks)**

c. Simplify the following boolean function using k-map, and implement by logic gates. $f(A, B, C, D, E) = \sum_m (3, 7, 10, 11, 12, 13, 14, 15, 17, 19, 21, 23, 25, 27, 28, 29, 31) + \sum_d (2, 6, 26, 30)$ **(08 Marks)**

OR

2 a. Convert the given boolean function into minterm canonical form. $f(a, b, c) = (\bar{a} + b)(b + \bar{c})$. **(05 Marks)**

b. Simplify the following boolean fucntion using k-map $f(P, Q, R, S) = \sum_m (0, 2, 4, 5, 6, 8, 10, 15) + \sum_d (7, 13, 14)$. **(07 Marks)**

c. Using Quine – McCluskey method, obtain a minimal SOP expression for $f(a, b, c, d) = \sum_m (2, 3, 4, 5, 13, 15) + \sum_d (8, 9, 10, 11)$. **(08 Marks)**

Module-2

3 a. Design two bit magnitude comparator and draw the logic diagram. **(10 Marks)**

b. Write a short note on encoders. **(05 Marks)**

c. Design full adder using two numbers of 4:1 MUX. **(05 Marks)**

OR

4 a. Explain look ahead carry adder. **(10 Marks)**

b. Implement following multiple output function using IC74138 and external gates. **(05 Marks)** $F_1 (A, B, C) = \sum_m (1, 4, 5, 7)$ and $F_2 (A, B, C) = \pi_m (2, 3, 6, 7)$.

c. Design 16:1 multiplexer using 8:1 MUX. **(05 Marks)**

Module-3

5 a. Explain the working of master slave JK flip-flops with functional table and timing diagram. Show how race around condition is overcome. **(08 Marks)**

b. Obtain characteristic equation of SR flip-flop. **(05 Marks)**

c. Explain working of 3-bit binary ripple counter with the suitable logic and timing diagram. **(07 Marks)**

OR

6 a. Convert JK flip-flop to D flip flop. **(05 Marks)**

b. Explain the 4 modes of operation of shift register with suitable logic diagram and truth table. **(08 Marks)**

c. Design MOD – 6 synchronous counter using D flip-flop. **(07 Marks)**

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-4

7 a. Analyze the following sequential circuit given in Fig Q7(a) and obtain excitation, transition and state table. Also write the state diagram.

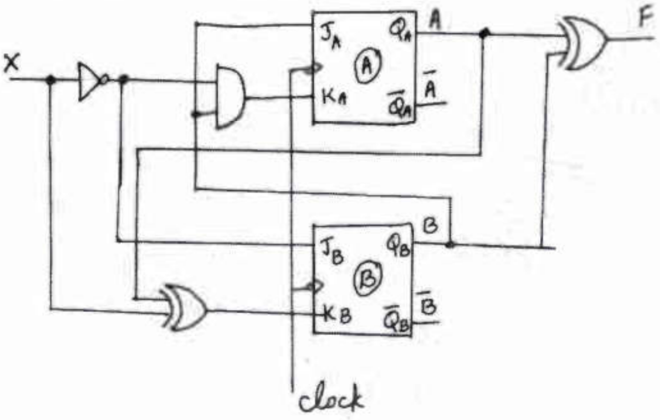

Fig Q7(a) **(12 Marks)**

b. Design a synchronous counter with the sequence 0, 1, 3, 7, 6, 4, 0 . . . . using JK flip-flop. **(08 Marks)**

OR

8 a. Design a clocked sequential circuit that operates according to the state diagram shown in Fig Q8 (a) implement the circuit using D flip flop.

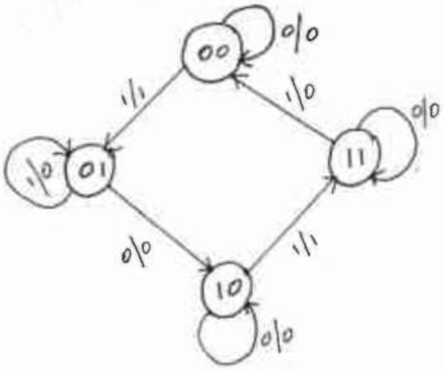

Fig Q8(a) **(12 Marks)**

b. With the help of block diagram explain Mealy and Moore model in a sequential circuit analysis. Give the example circuits. **(08 Marks)**

Module-5

9 a. Write the comparison between VHDL and verilog. **(08 Marks)**

b. Explain the various data types available in VHDL. **(06 Marks)**

c. Write HDL code of a 2 × 1 multiplexer – VHDL. **(06 Marks)**

OR

10 a. Write a data flow description for a full adder with active high enable in both VHDL and verilog. **(08 Marks)**

b. Explain shift and rotate operators in HDL with an example. **(08 Marks)**

c. Explain the structure of verilog module. **(04 Marks)**

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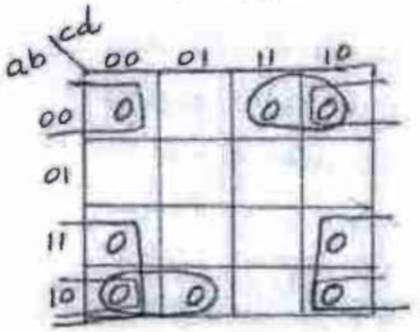
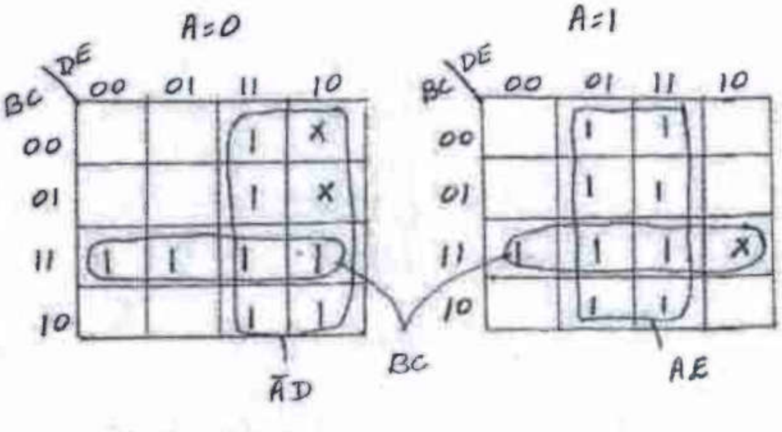
Scheme & Solution

Signature of Scrutinizer 14/11/18

Subject Title: Digital System Design **Subject Code:** 17EE35

Question Number	Solution	Marks Allocated
1 (a)	Definition with example expression for canonical minterm form Canonical maxterm form	-5M-
(b)	Comparision between prime implicant and essential prime implicant	-2M-
	$f = \pi_M (0, 2, 3, 8, 9, 10, 12, 14)$  Prime implicants & essential prime implicants: $(a+b+\bar{c})(\bar{a}+b+c)$ $(\bar{a}+d)(b+d)$	-5M-
(c)	 	-4M-
	$f = \bar{A}D + BC + AE$ -	-2M-
	logic diagram -	2M

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Question Number | **Solution** | **Marks Allocated**

(2) a.

$$f(a,b,c) = (\bar{a}+b)(b+\bar{c})$$
$$= abc + ab\bar{c} + \bar{a}bc + \bar{a}b\bar{c} + \bar{a}\bar{b}\bar{c}$$
$$= \Sigma m(0,2,3,6,7)$$

-5M-

(b)

PQ \ RS	00	01	11	10
00	1			1
01	1	1	x	1
11		x	1	x
10	1			1

answers:

(1) $\bar{P}.Q+QS.+\bar{Q}\bar{S}$

OR

(2) $\bar{P}Q+QR+\bar{Q}\bar{S}$

OR

(3) $\bar{P}\bar{S}+QS+\bar{Q}\bar{S}$

-5+2M-

(c) Quine Mccluskey method.

①

minterm	binary
m_2	0010
m_4	0100
m_8	1000
m_3	0011
m_5	0101
m_9	1001
m_{10}	1010
m_{11}	1011
m_{13}	1101
m_{15}	1111

②

minterm	binary
(2,3) ✓	001-
(2,10) ✓	-010
(4,5)	010-
(8,10) ✓	10-0
(8,9) ✓	100-
(3,11) ✓	-011
(5,13)	-101
(9,13) ✓	1-01
(9,11) ✓	10-1
(10,11) ✓	101-
(13,15) ✓	11-1
(11,15) ✓	1-11

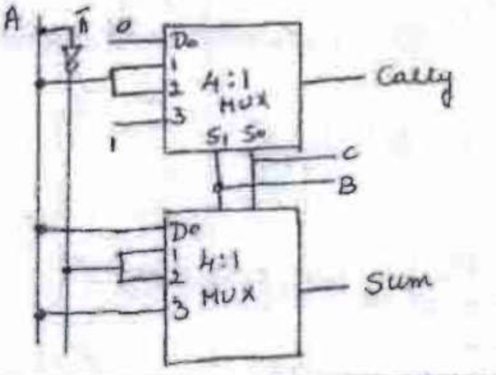
minterm	binary
(2,3,10,11)	-01-
(8,9,10,11)	10--
(9,11,13,15)	1--1

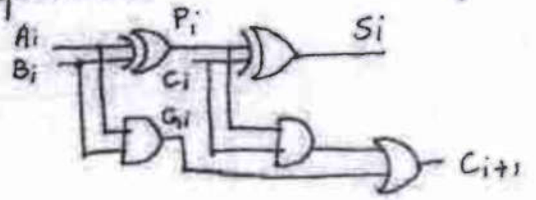
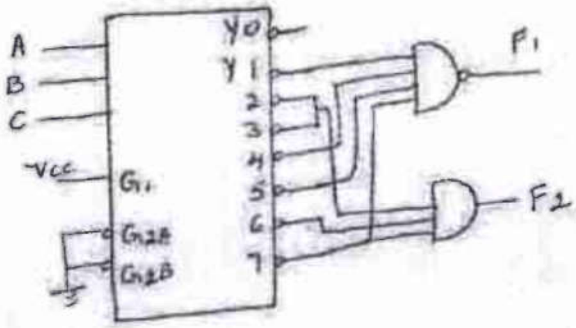
Prime implicants

$\bar{a}b\bar{c}$	(4,5)
$b\bar{c}d$	(5,13)
$\bar{b}c$	(2,3,10,11)
$a\bar{b}$	(8,9,10,11)
ad	(9,11,13,15)

-5M-

Subject Title: Digital System Design **Subject Code:** 17EE35

<table>
<tr><th>Question Number</th><th>Solution</th><th>Marks Allocated</th></tr>
<tr><td></td><td>Prime implicant table</td><td>-2M-</td></tr>
<tr><td></td><td>$y=\bar{b}c+\bar{a}b\bar{c}+ad$</td><td>-1M-</td></tr>
<tr><td></td><td>Module 2</td><td></td></tr>
<tr><td>3
(a)</td><td>2-bit comparator truth table</td><td>-2M-</td></tr>
<tr><td></td><td>K-map simplification</td><td>-6M-</td></tr>
<tr><td></td><td>$(A>B)=A_0\bar{B}_1\bar{B}_0+A_1\bar{B}_1+A_1A_0\bar{B}_0$
$(A=B)=(A_0\odot B_0)(A_1\odot B_1)$
$(A<B)=\bar{A}_1\bar{A}_0B_0+\bar{A}_0B_1B_0+\bar{A}_1B_1$
} each - 2M.</td><td></td></tr>
<tr><td></td><td>logic diagram - (2M)</td><td></td></tr>
<tr><td>(b)</td><td>Definition for encoder -</td><td>-1M-</td></tr>
<tr><td></td><td>Block diagram -</td><td>-2M-</td></tr>
<tr><td></td><td>Explanation -</td><td>-2M-</td></tr>
<tr><td>(c)</td><td>Full adder
Sum = $\Sigma m(1,2,4,7)$, Carry = $\Sigma m(3,5,6,7)$</td><td>-1M-</td></tr>
<tr><td></td><td>
Sum
<table>
<tr><td></td><td>D0</td><td>D1</td><td>D2</td><td>D3</td></tr>
<tr><td>Ā</td><td>0</td><td>①</td><td>②</td><td>3</td></tr>
<tr><td>A</td><td>④</td><td>5</td><td>6</td><td>⑦</td></tr>
<tr><td></td><td>A</td><td>Ā</td><td>Ā</td><td>A</td></tr>
</table>
Carry
<table>
<tr><td></td><td>D0</td><td>D1</td><td>D2</td><td>D3</td></tr>
<tr><td>Ā</td><td>0</td><td>1</td><td>2</td><td>③</td></tr>
<tr><td>A</td><td>4</td><td>⑤</td><td>⑥</td><td>⑦</td></tr>
<tr><td></td><td>0</td><td>A</td><td>A</td><td>1</td></tr>
</table>
</td><td>-2M-</td></tr>
<tr><td></td><td>
</td><td>-2M-</td></tr>
</table>

Question Number	Solution	Marks Allocated
4 (a)	Explanation with the logic circuit  $P_i = A_i \oplus B_i$ $G_i = A_i B_i$	-3M-
	logic expressions $C_1 = G_0 + P_0 C_0$ $C_2 = G_1 + P_1 C_1$ $C_3 = G_2 + P_2 C_2$ $C_4 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 C_1$	- 3M -
	logic diagram of look ahead carry generator	- 4M -
(b)		- 5M -
(c)	logic diagram 16:1 MUX using 8:1 MUX	- 5M -
	MODULE-3	
5 (a)	logic diagram of Master slave JK flip flop.	- 2M -
	functional table / truth table	- 2M -
	Timing diagram	- 2M -
	Explanation with race around condition	- 2M .
(b)	SR flip flop truth table	- 2M -
	K-map $\begin{array}{ccccc} S \backslash RQ_n & 00 & 01 & 11 & 10 \\ 0 & 0 & 1 & 0 & 0 \\ 1 & 1 & 1 & x & x \end{array}$ $Q_{n+1} = S + \bar{R} Q_n$	- 2M -
	block diagram	- 1M -

Subject Title: Digital system Design　　Subject Code: 17EE35

Question Number	Solution	Marks Allocated

6.(c) logic diagram 3-bit ripple counter — -2M-

truth table — -1M-

Explanation — -2M-

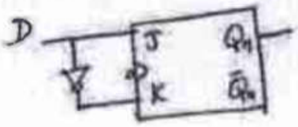
Timing diagram — -2M-

6(a) Conversion table

JK Flip flop to D flip flop.

D	Q_n	Q_{n+1}	J	K
0	0	0	0	x
0	1	0	x	1
1	0	1	1	x
1	1	1	x	0

$J = D$, $K = \bar{D}$ — 2+2+1



(b) 4 modes of operation

(1) SISO

(2) SIPO

(3) PISO

(4) PIPO

2 Marks each. — 2M x 4

explain with the logic diagram

(c) $2^n \geq N$, $N = 6$, $n = 3$ flip flops required.

Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	0	0	0
1	1	0	x	x	x
1	1	1	x	x	x

→ 2M

$D = Q_{n+1}$

simplification using K-map.

$D_A = Q_A \bar{Q}_C + Q_B Q_C$, $D_B = \bar{Q}_A \bar{Q}_B Q_C + Q_B \bar{Q}_C$, $D_C = \bar{Q}_C$ — -3M-

logic diagram — -2M-

Q.No. | Marks

Module-4

7 (a)

$F = A \oplus B$

$J_A = B,\ K_A = \bar{x} B$

$J_B = \bar{x},\ K_B = x \oplus A$. — -2M-

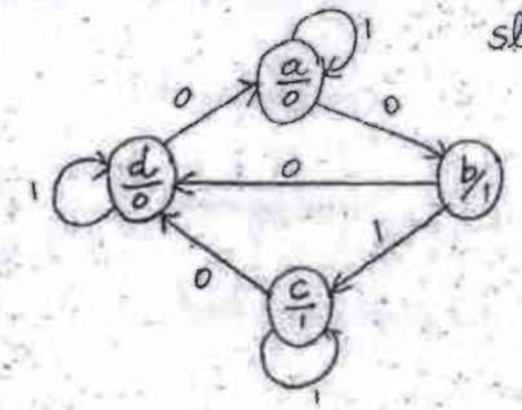
$Q_A^+ = B\bar{A} + (x+\bar{B})A$

$Q_B^+ = \bar{x}\bar{B} + \overline{x \oplus A} \cdot B$ — -3M-

Transition table.

Present state	Next state		output
	x = 0	x = 1	F
A B	A^+B^+	A^+B^+	
a	b	a	0
b	d	c	1
c	d	c	1
d	a	d	0

-5M-



State diagram -2M-

(b) 3-flip flops required

Excitation table → -3M-

K-map simplification : $J_A = B$ $K_A = \bar{B}$, $J_B = C$, $K_B = \bar{C}$, $J_C = \bar{A}$, $K_C = A$ } → 3M

logic diagram → -2M-

Q.No. | Marks

(8) (a) state table

Present state	Next state		output	
	x=0	x=1	x=0	x=1
AB	$A^+ B^+$	$A^+ B^+$	y	y
0 0	0 0	0 1	0	1
0 1	1 0	0 1	0	0
1 0	1 0	1 1	0	1
1 1	1 1	0 0	0	0

-4M-

K-map simplification

$D_A = \bar{x}B + A\bar{B}$, $Y = x\bar{B}$

$D_B = \bar{x}AB + x\bar{A} + x\bar{B}$

-4M-

Sequential circuit diagram - -2M-

(b) Mealy model explanation with block diagram & example logic circuit diagram -4M-

Moore model explanation with block diagram & example logic circuit diagram -4M-

Module-5

9 (a) Comparision between VHDL & Verilog.

Explain by Considering application, data type, easy of learning, libraries, operators, procedures, case sensitivity

Comment : → each carries (1M) -8M-

(b) VHDL data types

Scalar type
Composite type
Access type
File type
other types

give examples -6M-

(c) VHDL 2x1 multiplexer

```
library ieee;
use ieee.std_logic_1164all;
entity mux2x1 is
port (D0, D1, S, Enbar : in std_logic;
    Y : out std_logic);
end mux2x1;
architecture MUX of mux 2x1 is
signal I1, I2, I3, I4: std_logic;
begin
I1 <= not s after 10ns;
I2 <= not Enbar after 10ns;
I3 <= D0 and I1 and I2 after 10ns;
I4 <= D1 and S and I2 after 10ns;
Y <= I3 or I4 after 10ns;
  end MUX;
```

		o/p
S	Enbar	Y
x	1	0
0	0	D0
1	0	D1

Alternate methods such as structural Description, process Description, behavioral description case. can also be considered. 6M

10 (a) <u>VHDL data flow</u>

```
entity full_add is
port (A, B, Cin, En : in bit;
      Sum, Cout : out bit);
end full_add;
architecture adder of full add is
begin
  Sum <= (A XOR B XOR Cin) and En;
  Cout <= ((A and B) or (Cin and A) or (Cin and B)) & En;
end adder:
```

-4M

<u>Verilog data_flow</u>

```
module full_add (A.B.Cin, En, Sum, Cout);
input A, B, Cin, En;
output Sum, Cout;
assign Sum = ((A^B)^Cin) & En;
assign Cout = ((A & B) | (Cin &A) | (Cin & B)) & En;
end module.
```

-4M.

(b) Shift & rotate operators with examples -4+4 M-

Structure of verilog module Explanation.

```
module <module name> <port list>;
<declares>
<module items>
```

4M

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