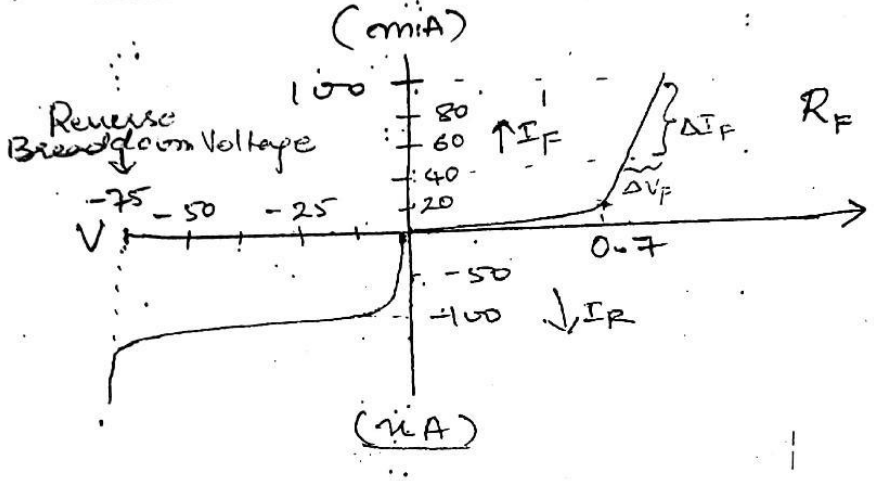
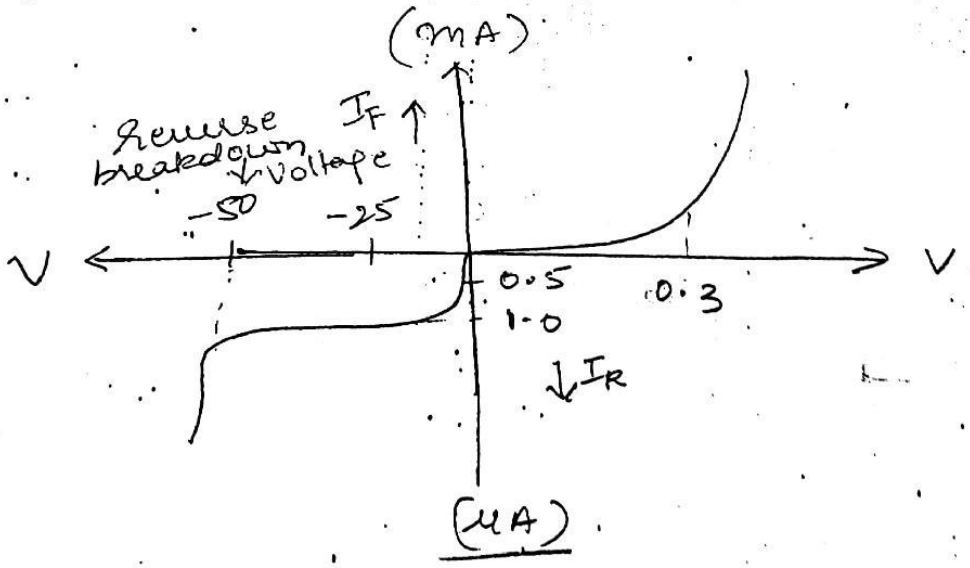
Characteristics & Parameters



$$R_F = \frac{V_F}{I_F}$$

Silicon diode

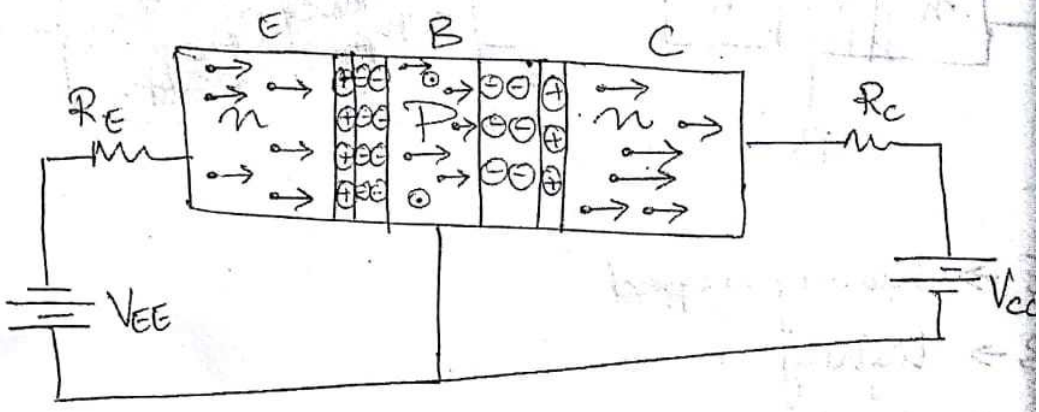


$$R_R = \frac{V_R}{I_R}$$

Ge diode

Ans 2(b) 2(b) **Transistor Operation (npn)**

Consider an npn transistor in active region. (E-B j^n is fwd biased & C-B j^n is rev bias in Common base mode.



→ The fwd bias EB j^n causes the electrons f n-type emitter to flow towards the base. This constitutes emitter current I_E.

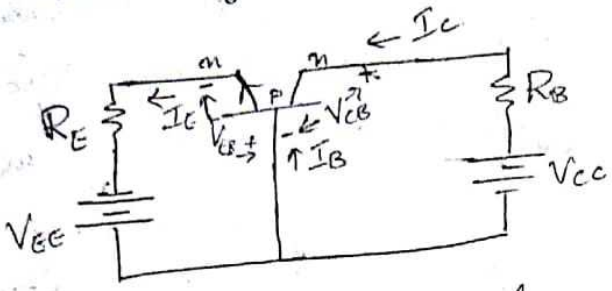
→ As these electrons flow through the p-type b they tend to combine with holes in p-regio (base). Since Base is thin & lightly dope the free electrons have only a short distance to go to reach the collector. Hence a few Electrons injected into base from emitt get recombined with holes in base constit I_B current & remaining large no of ele cross the Base region & move towards the terminal of external source the collector region. This constitutes Collector current. Hence

$$I_E = I_C + I_B$$

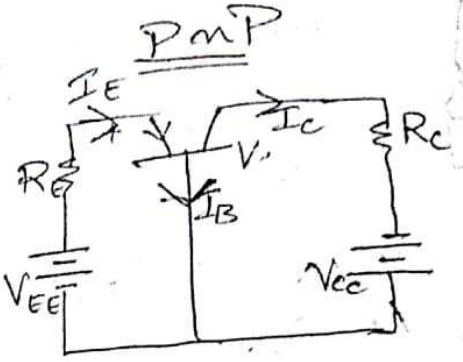
Ans: 1(c)

Common Base characteristics

Consider nPn transistor in CB mode & active region.



PnP

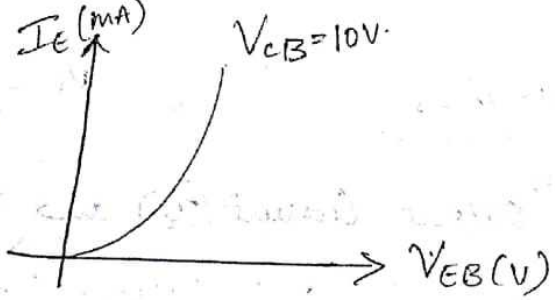


E-B jn → fwd biased

C-B jn → Rev biased

Input characteristics

It is the graph of input current (I_E) & input Voltage (V_{EB}) keeping output voltage (V_{CB}) constant.



1) Since E-B jn is fwd biased, I_E increases Exponentially with small increase in V_{EB}.

∴ Input resistance

$$R_i = \left.\frac{\Delta V_{EB}}{\Delta I_E}\right|_{V_{CB}=\text{Const}}$$

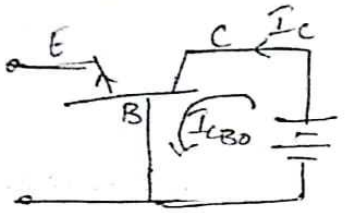
∴ R_i is low (fwd biased).

Que-1(c)

~~Diode acts as a ~~ device

1) In Active region, E-B jn is fwd biased & C-B jn is Rev biased. Hence I_C is approximately equal to I_E & transistor works as amplifier.

2) In cut-off region, $I_E = 0$, the Collector current $I_C = I_{CBO}$. In cut-off E-B jn & C-B jn is reverse biased.



3) In saturation region, E-B & C-B jn are fwd biased & hence the collector current (I_C) increases as shown in the graph.

4) Output resistance

$$R_o = \left.\frac{\Delta V_{CB}}{\Delta I_C}\right|_{I_E = \text{Const}}$$

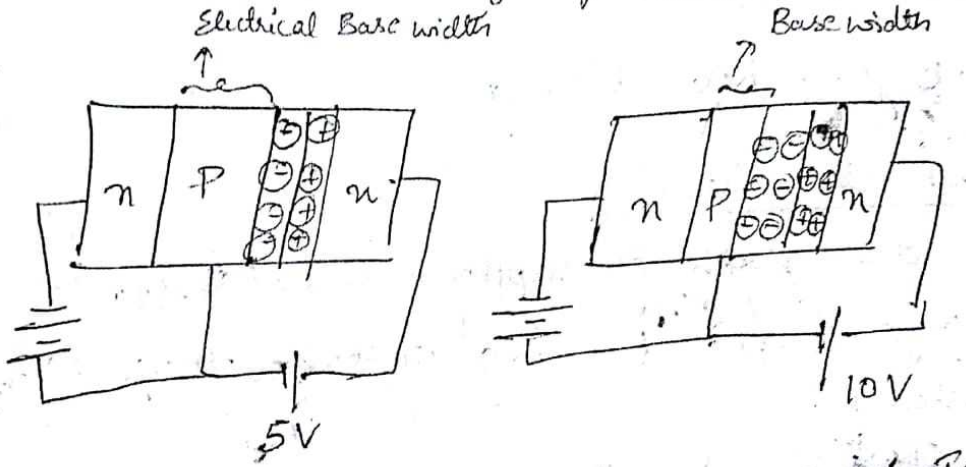
R_o is high (∵ Rev biased)

5) Notice in the graph that $I_C \simeq I_E$ ∴ BJT ∴ a Current Controlled device

6) As V_{CB} increases above $V_{CB(max)}$ shown in graph below C-B jn depletion region increases such that it penetrates into base & makes a contact with E-B depletion region. This is called punch through effect or reach through

Ans 1(c)

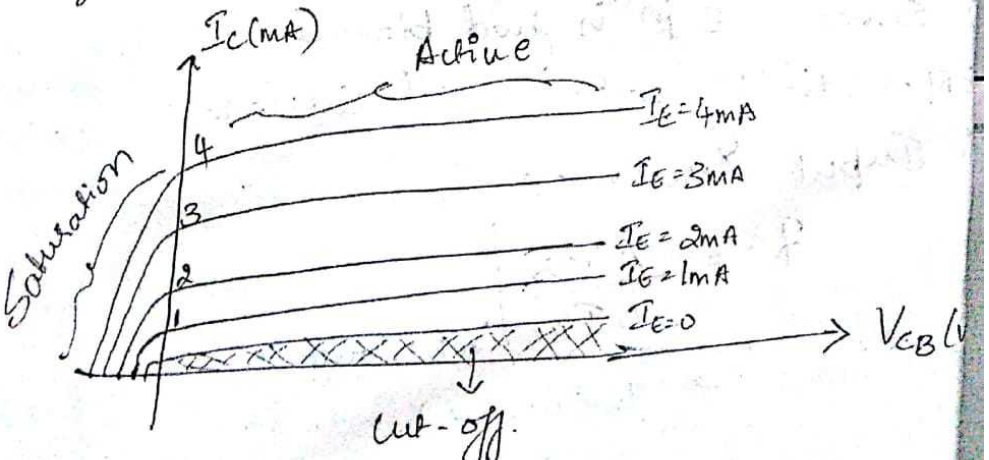
2) As V_{CB} increases, width of C-B j^n increase
∴ Base width decreases, leading to more charge particles per unit area. Thus concentration of the charge gradient increases in base region & causes more diffusion of electrons from n-type emitter to base. Thereby increasing Emitter current slightly. This effect is Early Effect or Base width modulation



Current gain $\beta = \frac{I_C}{I_E}$

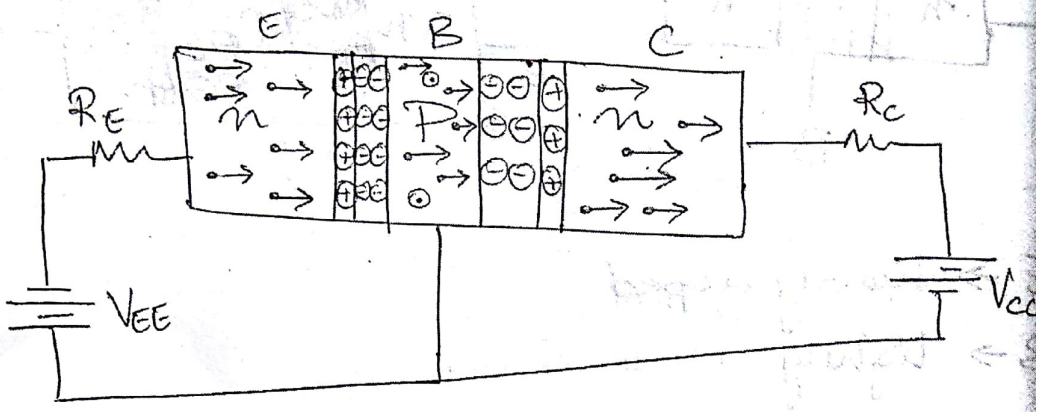
Output characteristics

It is a graph of Output Current (I_C) and O/P voltage (V_{CB}) at Constant input current I_E.



Ans 2(b) 2(b) **Transistor Operation (npn)**

Consider an npn transistor in active region. (E-B jⁿ is fwd biased & C-B jⁿ is rev bias in Common base mode.



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$$I_E = I_C + I_B$$

18 (66) Relation b/w α & β

$$\beta = \frac{I_C}{I_B}, \qquad \alpha = I_C/I_E$$

we know $I_E = I_C + I_B \Rightarrow I_B = I_E - I_C$

$$\beta = \frac{I_C}{I_E - I_C}$$

÷ by I_E, both nume & deno

$$\beta = \frac{I_C/I_E}{1 - I_C/I_E} = \frac{\alpha}{1-\alpha}$$

$$\boxed{\beta = \frac{\alpha}{1-\alpha}}$$

÷ nume & deno by $1+\beta$

$$\frac{\beta}{1+\beta} = \frac{\frac{\alpha}{1-\alpha}}{1+\beta}$$

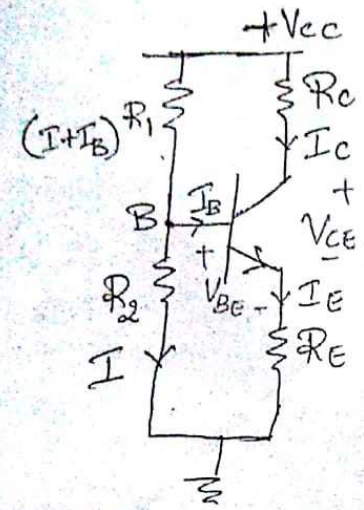
$$= \frac{\frac{\alpha}{1-\alpha}}{1+\frac{\alpha}{1-\alpha}} = \frac{\frac{\alpha}{1-\alpha}}{\frac{1-\alpha+\alpha}{1-\alpha}}$$

$$\boxed{\frac{\beta}{1+\beta} = \alpha}$$

Module-2

Ans-3(a) Voltage Divider Bias

(also called Self Bias ckt)



In this ckt, Biasing is provided by 3 resistors R_1, R_2 & R_E. The resistors R_1 & R_2 acts as a potential divider giving a fixed voltage at point B.

Consider a case where I_C changes due to change in β. Let us consider that I_C increases with increase in β. Since ($I_C \simeq I_E$) I_E also increases thus voltage drop across R_E increases i.e V_E increases.

we know that $V_{BE} = V_B - V_E$

As V_E increases, V_{BE} decreases. Due to reduction in V_{BE}, I_B base current reduces & hence I_C also reduces. This reduction

in I_C compensates for original increase in I_C.

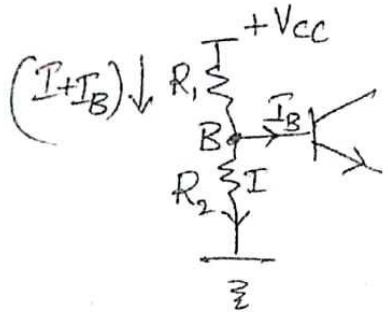
Case: $\beta\uparrow$, $I_C\uparrow$

Since $I_C \simeq I_E$, $I_E\uparrow$, $\downarrow V_{BE} = V_B - V_E\uparrow$, $I_B\downarrow$,

Since $I_C = \beta I_B$, $I_C\downarrow$

Compensates.

Consider the Base section



$$V_B = \frac{V_{CC} \times R_2}{R_1 + R_2}$$

The current I is very much larger than I_B, hence neglecting I_B, we have V_B as

Consider collector section, applying KVL

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

→ this ckt offers the Best Stability to operating point.

→ Solve numericals ~~A~~ X

→ Current Series feedback

Ideal OP-Amp Characteristics

a) Infinite Voltage gain ($A_{OL} = \infty$)

Open loop gain of an op-Amp is denoted as A_{OL} & is infinite for an ideal op-Amp.

b) Infinite input impedance ($R_{in} = \infty$)

The input impedance R_{in} is infinite for an ideal op-Amp. Hence no current flows into the input terminals of the op-Amp.

c) Zero output impedance ($R_o = 0$)

Output impedance (R_o) of an op-Amp is zero. Hence output voltage is same irrespective of value of load ~~resistance~~ resistance connected.

d) Zero offset voltage ($V_{ios} = 0$)

Offset voltage (V_{ios}) is some extra voltage, we add or subtract at the input section to make the output zero in case when $V_1 = V_2$. Ideally V_{ios} has to be zero.

e) Infinite B.W ($B.W = \infty$)

An ideal op-Amp has infinite B.W. Hence op-Amp can operate over a wide range of frequencies i.e from 0 to ∞. Hence op-Amp can amplify d.c Signals (zero frequency) & a.c Signals.

f) Infinite CMRR ($\rho = \infty$)

It is ratio of differential gain & Common mode gain. It is ideally ∞,

$$CMRR = \frac{A_d}{A_c} = \infty.$$

Hence $A_c = 0$ i.e Common mode gain is zero.

g) Infinite Slew Rate ($S=\infty$)

Infinite Slew Rate indicates that output changes simultaneously with the changes in the input ~~signal~~ voltage.

Thus Slew rate is defined as maximum rate of change of output voltage with time. & unit is V/μs

$$\text{Slew Rate} = S = \left.\frac{dV_o}{dt}\right|_{max}$$

h) Power Supply Rejection Ratio ($PSRR=0$)

PSRR is ratio of change in input offset voltage due to change in supply voltage producing it, keeping other power supply voltage constant.

$$PSRR = \left.\frac{\Delta V_{IOS}}{\Delta V_{CC}}\right|_{V_{EE}}$$

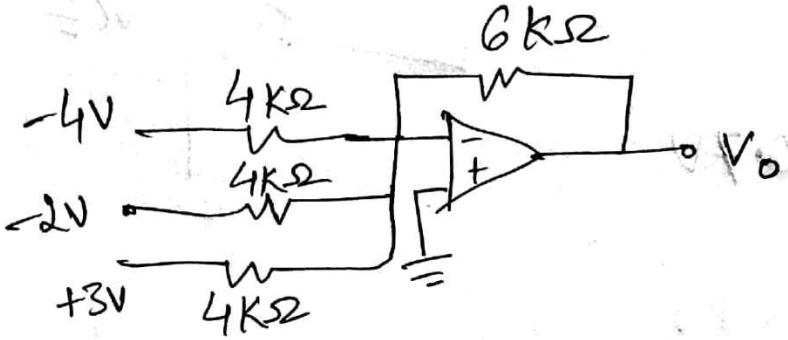
or

$$PSRR = \left.\frac{\Delta V_{IOS}}{\Delta V_{EE}}\right|_{V_{CC}}$$

Module-2

Ans. 3

(C)



$$V_o = -\frac{R_F}{R_1}V_1 - \frac{R_F}{R_2}V_2 - \frac{R_F}{R_3}V_3$$

$$= -\frac{6K}{4K}(-4) - \frac{6K}{4K} \times (-2) - \frac{(6K)}{(4K)} \times 3$$

$$= 6 + 3 - \frac{9}{2} = 9 - \frac{9}{2} = \frac{9}{2} = 4.5V$$

Ans-3(a)

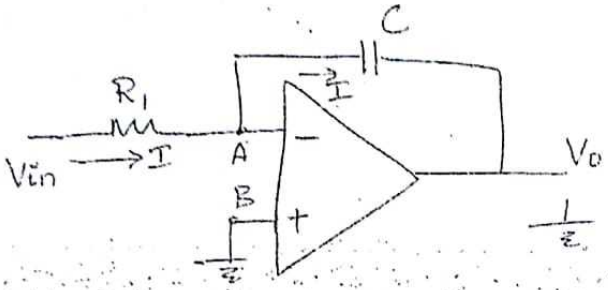
if $R_f = R_1 = R_2$

$\therefore V_o = -V_1 + V_2$.

$\Rightarrow V_o = V_2 - V_1$

★ Solve Numericals from text.

Integrator



By virtual ground concept,

$V_A = V_B = 0$

As input current of op-Amp is zero, the entire current I flowing through R_1, also flows through C.

From fig

$$I = \frac{V_{in} - V_A}{R_1} = \frac{V_{in}}{R_1} \quad -(1)$$

From o/p side,

$$I = C \frac{d(V_A - V_o)}{dt}$$

$$I = -C \frac{dV_o}{dt} \quad -(2)$$

Eq (1) & (2)

$$\frac{V_{in}}{R_1} = -C\frac{dV_o}{dt}$$

Integrating both sides

$$\int_0^t \frac{V_{in}}{R_1} = -\int_0^t C\frac{dV_o}{dt}$$

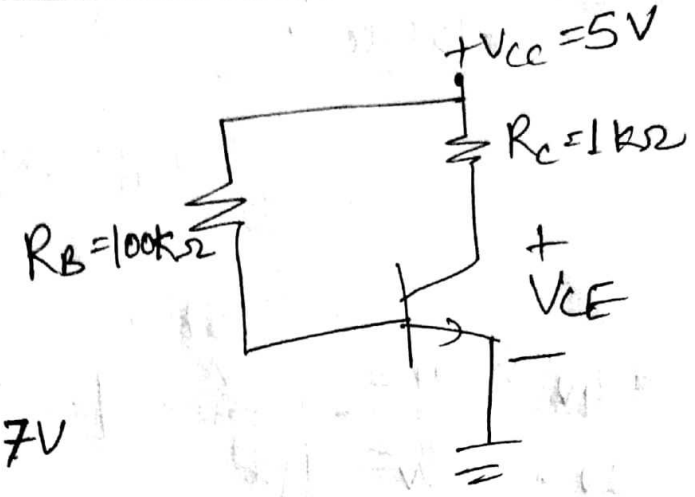
$$V_o = -\frac{1}{R_1 C}\int_0^t V_{in}\cdot dt$$

This o/p is integration of input. hence called integrator
where RC is called time constant of integrator

→ Integration of Step waveform is Ramp waveform
→ " " Square " " Triangular "
" " Sine " " neg Cosine

Ans 4

(a)



Given

$V_{BE} = 0.7V$

$\beta = 50$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{5 - 0.7}{100 \times 10^3} = 43\mu A.$$

$$I_C = \beta I_B = 50 \times 43 \times 10^{-6} = 2.15mA$$

$$V_{CE} = V_{CC} - I_C R_C = 5 - 2.15 \times 10^{-3} \times 10^3$$
$$= 2.85V$$

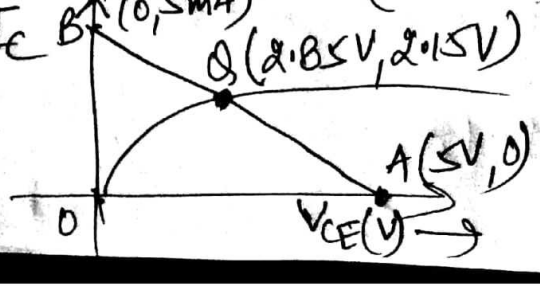
Q Point (2.85V, 2.15mA)

DC Load line

(a) $V_{CE} = V_{CC}$ at $I_C = 0$ so $A(V_{CC}, 0)$

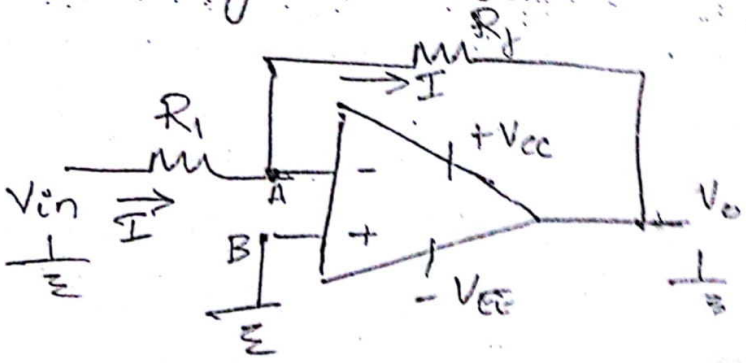
$A(5V, 0)$

(b) $I_C = \frac{V_{CC}}{R_C}$ at $V_{CE} = 0$ so, $B(0, 5mA)$



Ideal Inverting Amplifier

An amplifier that provides 180° phase shift between input & output is called an inverting amplifier. Hence the input is given to the inverting terminal.



Note: (No Current Enters the input terminal of Op-Amp due to its high input impedance)

By concept of virtual ground.

$$V_A = V_B = 0\,V.$$

$$I = \frac{V_{in} - V_A}{R_1} \qquad \text{Since } V_A = 0$$

$$I = \frac{V_{in}}{R_1} \quad — (1)$$

From output side, direction of current I is given

$$I = \frac{V_A - V_o}{R_f}$$

$$I = \frac{-V_o}{R_f} \quad — (2)$$

Equate (1) & (2)

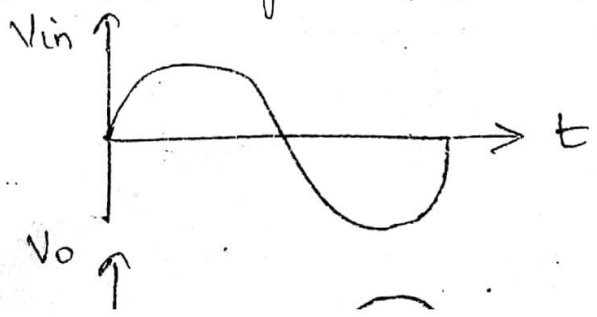
$$\frac{V_{in}}{R_1} = -\frac{V_o}{R_f}$$

$$\Rightarrow \boxed{\frac{V_o}{V_{in}} = -\frac{R_f}{R_1}}$$ gain of inverting amplifier

-ve sign indicates that O/P is inverted with respect to I/P. Hence it is inverting amplifier.

★: Solve Numericals from text book

~~Non-Sine~~



★: Learn up key points from

Module-3

Ans: 5 (a)

(i) $(11001.011)_2 \longrightarrow (\ )_{10}$

$2^4\ 2^3\ 2^2\ 2^1\ 2^0\ .\ 2^{-1}\ 2^{-2}\ 2^{-3}$

$2^4 + 2^3 + 1 + \frac{1}{2^2} + \frac{1}{2^3} = 16 + 8 + 1 + \frac{1}{4} + \frac{1}{8}$

$= 25 + \frac{2+1}{8} = 25 + \frac{3}{8}$

$= (25.375)_{10}$

(ii) $(186.75)_{10} \longrightarrow (\ )_2$

2	186	0
2	93	1
2	46	0
2	23	1
2	11	1
2	5	1
2	2	0
	1	

$.75 \times 2 = 1.50$ 1

$.5 \times 2 = 1.0$ 1

$(10111010.11)_2$

(iii) $(64.73)_8 \longrightarrow (\ )_{16}$

$(110\ 100\ .\ 111\ 011)_2$

$(34.EC)_{16}$ Ans

(iv) $(ABCD)_{16} \longrightarrow (\quad)_2$

$(1010\ 1011\ 1100\ 1101)_2$ Ans

(b) Subtract using 2's complement

(i)

(i) $(111001)_2 - (101011)_2$

$(111001)_2$
$-(101011)_2 \xrightarrow{2's} (010101)_2$

111001
010101
(1) 001110

carry ignore

Ans $\rightarrow (001110)_2$

(ii) $(1111)_2 - (1011)_2$

$(1111)_2$
$-(1011)_2 \xrightarrow{2's\ comp} 0101$

1111
0101
Ignore (1) 0100

$(0100)_2$ Ans

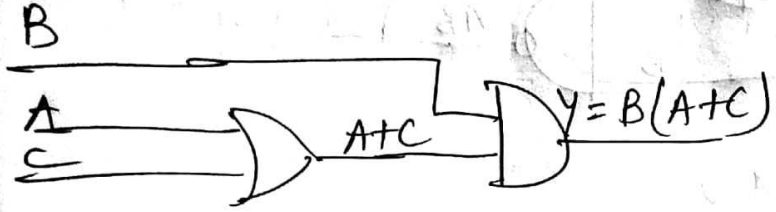
Ans-5

(C) $Y = ABC + AB\bar{C} + \bar{A}BC$

$= AB(C+\bar{C}) + \bar{A}BC = AB + \bar{A}BC$

$= B(A+\bar{A})(A+C)$

$= B(A+C)$



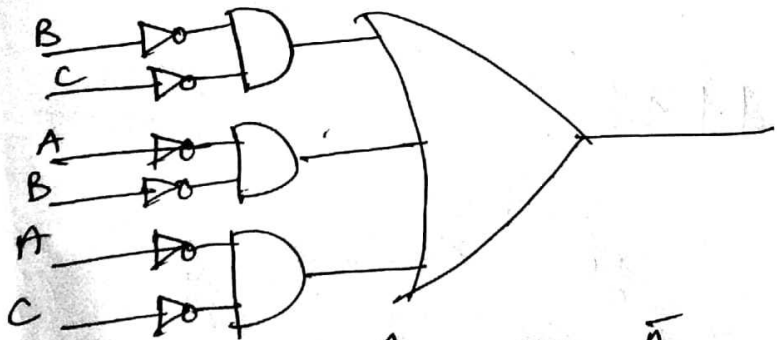
OR

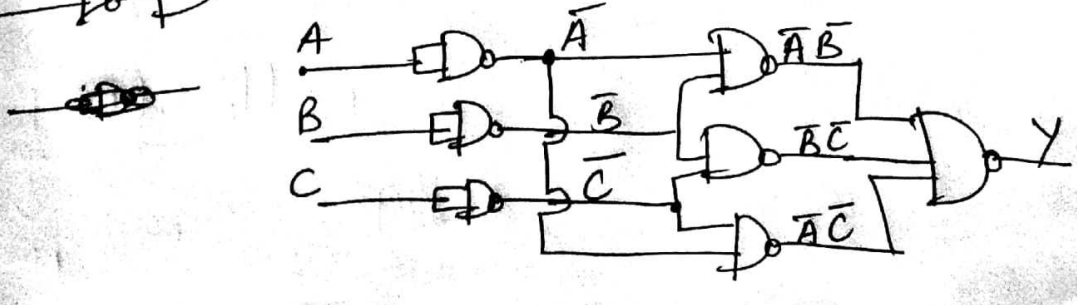
Ans-6

(C) $Y = A\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B} + \bar{A}\bar{C}$

$= \bar{B}\bar{C}(A+\bar{A}) + \bar{A}\bar{B} + \bar{A}\bar{C}$

$Y = \bar{B}\bar{C} + \bar{A}\bar{B} + \bar{A}\bar{C}$ = ~~$B\bar{B}C + A\bar{B}C + \bar{A}BC$~~





Q5(b) Q5(d)

De Morgan's Theorem :-

Theorem I

$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

NAND = Bubbled OR

* The LHS of this theorem represents a NAND gate with input A and B whereas the right hand side (RHS) of the theorem represents an OR gate with inverted input
This OR gate is called as Bubbled OR.

or

* The Complement of the Product of two or more variables is equal to the Sum of the Complement of the variable individually.

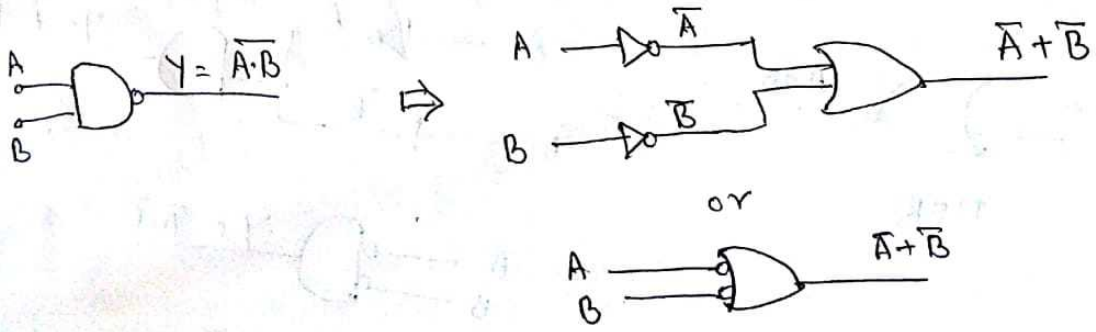


Table showing Verification of the 1st Theorem

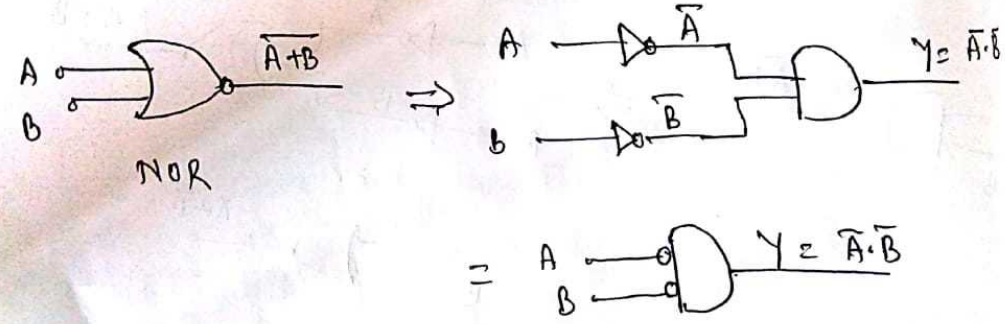
A	B	$\overline{A \cdot B}$	$\overline{A}$	$\overline{B}$	$\overline{A}+\overline{B}$
0	0	1	1	1	1
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	0	0	0

Theorem 2

$$\overline{A+B} = \overline{A} \cdot \overline{B}$$

NOR = Bubbled AND

* The LHS of this theorem represents a NOR gate with input A and B, whereas the RHS represents an AND gate with Inverted inputs.
* This AND gate is called as Bubbled AND.



$=$

Bubbled AND.

Or

* The Complement of the Sum of two variables is Equal to the Product of the Complement of the variable Individually.

Table Showing Verification of 2nd Theorem

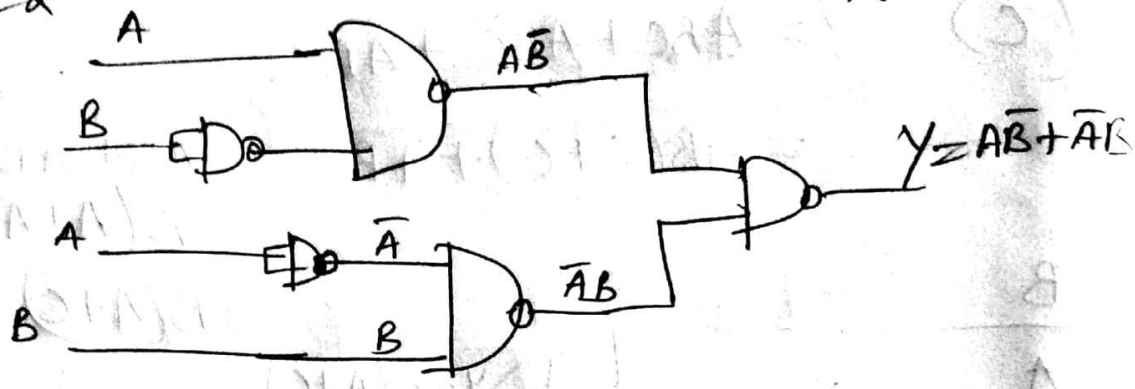
A	B	$\overline{A+B}$	$\overline{A}$	$\overline{B}$	$\overline{A} \cdot \overline{B}$
0	0	1	1	1	1
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	0

$Y = \bar{A}B + \bar{B}A = A \oplus B$

↙ XOR

Ans. 6

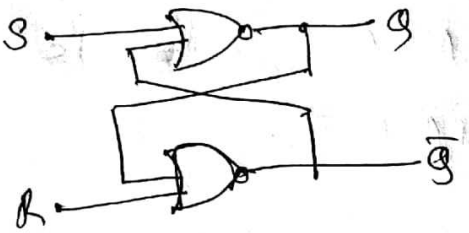
(b)

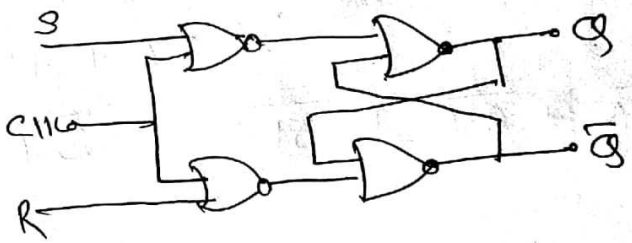


7(a)

Latch		Flip flop
(i) Latch is level triggered	–	Flip flop is edge Triggered.
(ii) O/p changes with change in input	–	O/p changes only at the +ve or -ve edge of the clock
(iii) It is made up of basic gates and there is no Control signal	–	It has control signal called as clock.
(iv) Ex – SR Latch	–	Ex – SR flip flop J-K flip flop

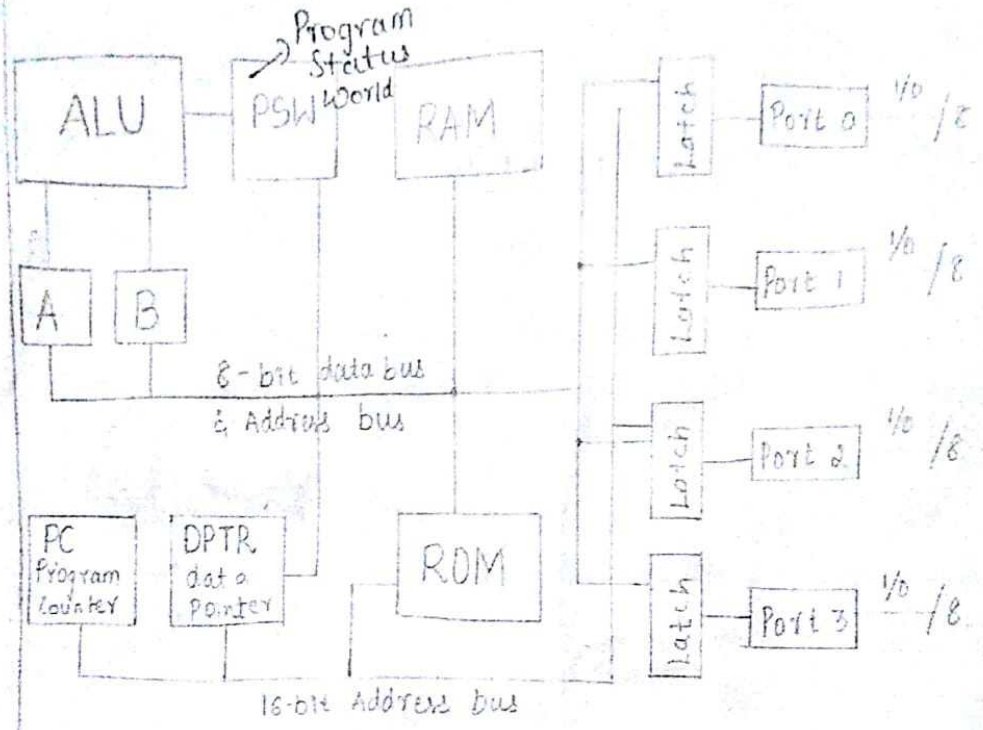
(v)





MICROCONTROLLER

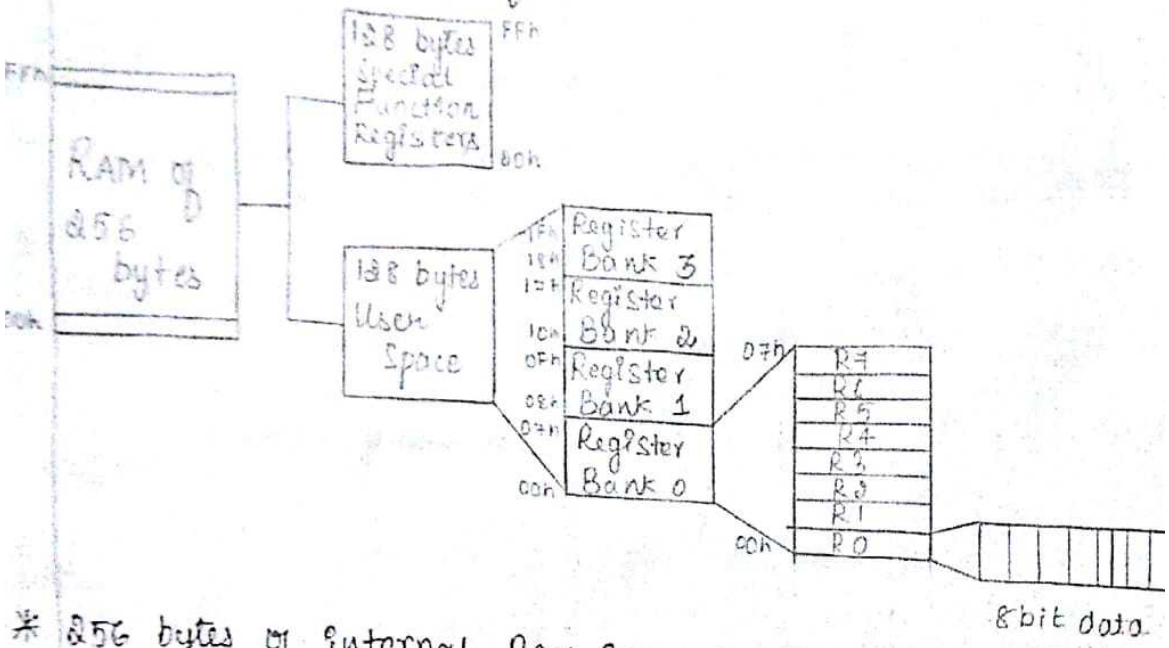
⇒ Architecture of 8051 :-



* 8051 has an 8 bit ALU.
* It has 8 bit - data bus & 16 bit - Address bus.
* ALU is directly associated with two 8 bit registers namely A & B.
* 8051 has 3 kilobytes of ROM memory.
* ROM stores all the optcodes (operational codes) require for microcontroller to understand what an instruction is supposed to do (To understand instruction).
* PC holdes the Address of next instruction to be Executed
* Data pointer is a 16 bit register used to access interna RAM & ROM Space (or) External RAM & ROM Space.

* 8051 has 4 I/O ports namely Port 0, Port 1, Port 2 & Port 3. Each I/O port has 8 I/O pins.
* 8051 has 256 bytes of RAM Space.
* Program Status word (PSW) is an 8-bit register which contains flags like Carry flag, parity flag etc, this register gets updated automatically after An ALU Operation.

Internal Structure of RAM :-



* 256 bytes of internal RAM space is divided as 2 halves namely 128 bytes of Special function register Space & 128 bytes of User Space
* User Space is divided into 4 register banks namely Register Bank 0, Register Bank 1, Register Bank 2, Register Bank 3
* Each register bank has 8 registers namely R0, R1, R2, R3, R4, R5, R6, R7.
* Each register Contains 8 bit data

S-R Latch using NOR Gate :-

Fig. 1 shows NOR latch. S and R are the inputs that are called as set (S) and R (Reset) inputs.

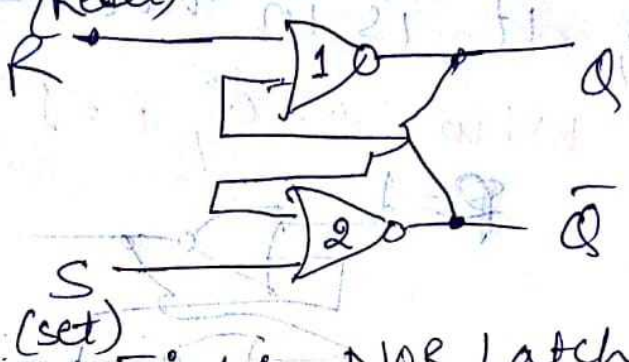


Fig 1 :- NOR Latch

→ Two outputs ie Q and $\bar{Q}$ is shown Q is the normal output and $\bar{Q}_n$ is its complemented form.

Truth Table

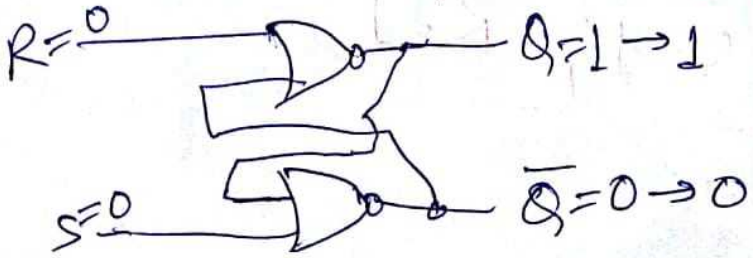
S	R	Q_{n+1}	$\bar{Q}_{n+1}$	State
0	0	1 / 0 (Q_n)	0 / 1 ($\bar{Q}_n$)	Hold
0	1	0	1	Reset
1	0	1	0	Set
1	1	0	0	NA or Invalid

Q_n → Previous state

Q_{n+1} → Present state

Working or Operation

Case-I When S=0, R=0 (After $Q_n = 1$, $\bar{Q}_n = 0$)



So, here $Q_{n+1} = 1$

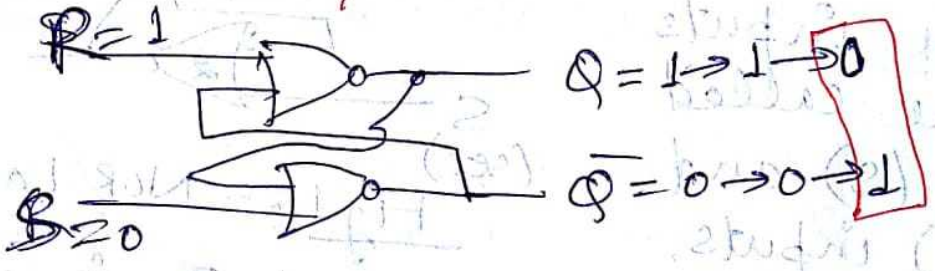
$\overline{Q_{n+1}} = 0$

i.e. $Q_{n+1} = Q_n = 1$

$\overline{Q_{n+1}} = \overline{Q_n} = 0$

So, it is in hold state.

Case-2 When $S=0$, $R=1$

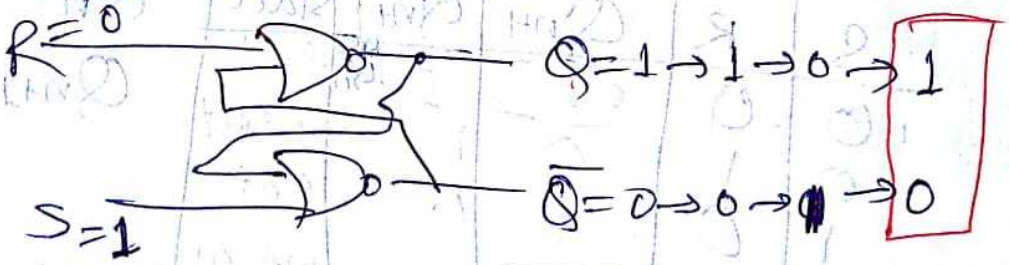


So, $Q_{n+1} = 0$

$\overline{Q_{n+1}} = 1$

So, this is Reset state.

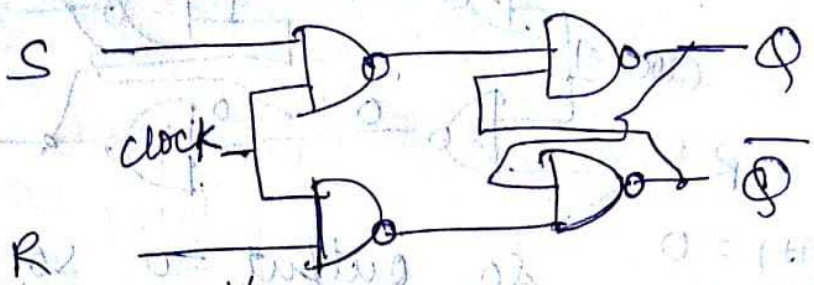
Case-3 When $S=1$, $R=0$



So, $Q_{n+1} = 1$ $\overline{Q_{n+1}} = 0$

So, output is in set state.

S-R Flip-Flop using NAND :- (8)

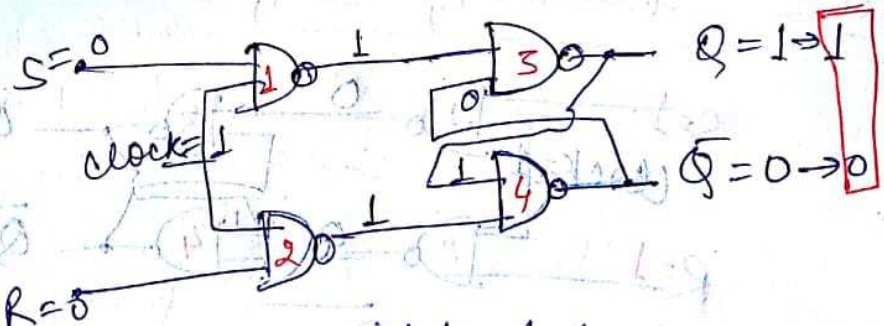


Truth Table (For ~~Both NOR and~~ Nand (S-R) Flip Flop)

clock	S	R	Q_{n+1}	$\overline{Q_{n+1}}$	State	
0	X	X	Q_n	$\overline{Q_n}$	hold	(No change)
1	0	0	1 (Q_n)	0 ($\overline{Q_n}$)	hold	(when $Q_n=1$, $\overline{Q_n}=0$)
1	0	1	0	1	Reset	
1	1	0	1	0	Set	
1	1	1	1	1	Invalid or Not allowed (N.A)	

Working or Operation :-

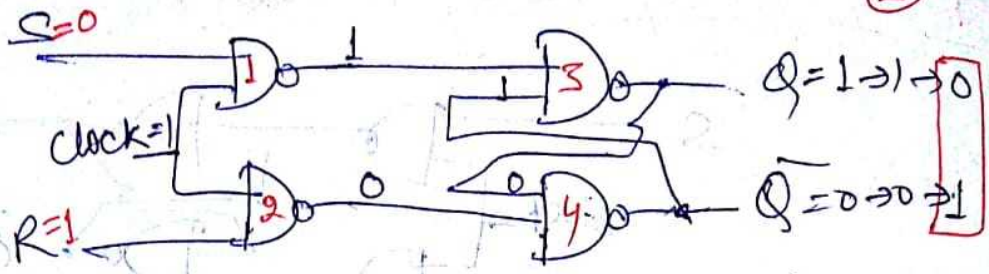
Case-1 ~~Clock~~ clock = 1, S = 0, R = 0 (Let $Q_n=1$, $\overline{Q_n}=0$)



So,
$Q_{n+1} = Q_n = 1$
$\overline{Q_{n+1}} = \overline{Q_n} = 0$

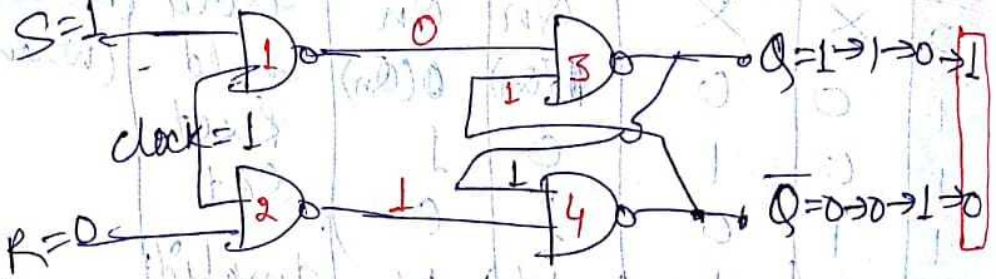
So, this state is hold state.

Case-2 clock = 1, S = 0, R = 1



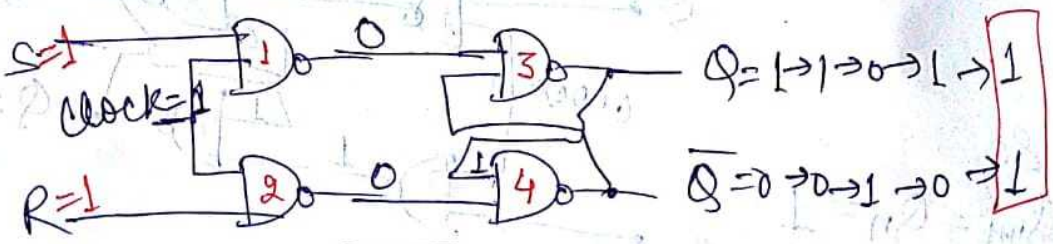
So, $Q_{n+1} = 0$
$\overline{Q_{n+1}} = 1$ So, output = 0 so, Reset state.

Case-3 clock=1, S=1, R=0



So, $Q_{n+1} = 1$
$\overline{Q_{n+1}} = 0$ So output = 1, so Set state.

Case-4 clock=1, S=1, R=1

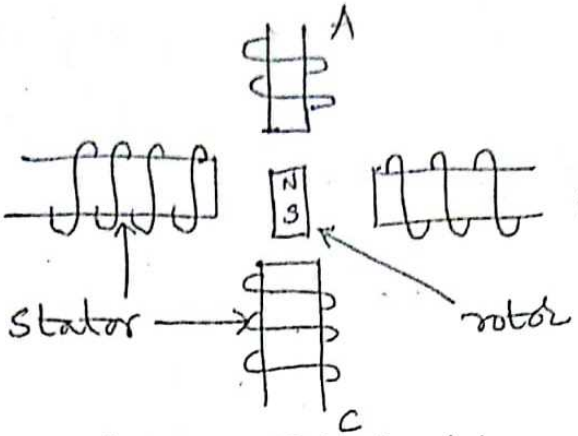


Since $Q_{n+1} \neq \overline{Q_{n+1}}$
And here $Q_{n+1} = 1$
$\overline{Q_{n+1}} = 1$

So, Invalid state or NA (Not allowed state)

8C 15/05/2018

* Stepper Motor



Important

Wave drive

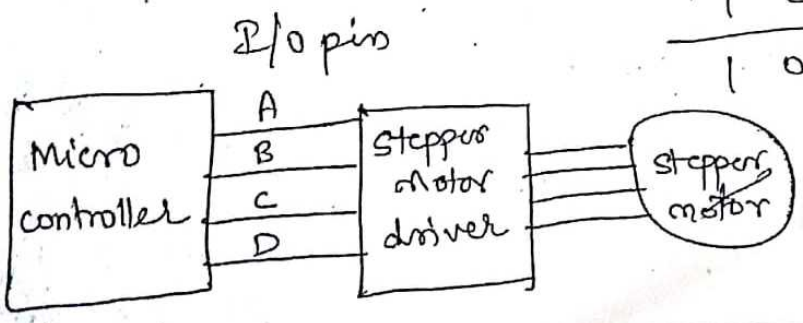
A	B	C	D
1	0	0	0
0	1	0	0
0	0	1	0
0	0	0	1
1	0	0	0

Full step drive

A	B	C	D
1	1	0	0
0	1	1	0
0	0	1	1
1	0	0	1
1	1	0	0

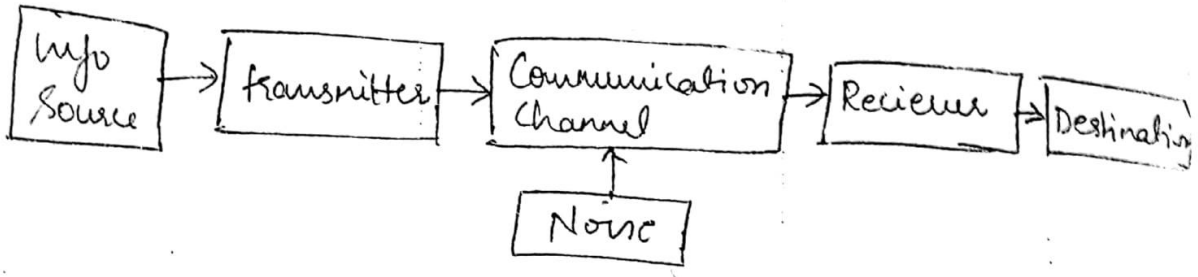
Half step drive

A	B	C	D
1	0	0	0
1	1	0	0
0	1	0	0
0	1	1	0
0	0	1	0
0	0	1	1
0	0	0	1
1	0	0	1
1	0	0	0



Communication Systems

Basic Block diagram



Information may contain humans voice, picture, code, data, music etc

Transmitter is a collection of electronic circuits to convert the information source into a suitable signal for transmission over a given Communication Channel. The messages have to be processed before transmission & converted into electrical signals

Communication channel → Line Communication
→ Radio "

Line Communication use pair of wires that carry signals from one end to another. Communication is also done by using Co-axial cables or fiber optic cable. hence use of Physical wires or Conductors b/w transmitter & reciever is refered to as Line Communicatio

Radio Communication : is a wireless Communication, Requiring no Physical wires b/w transmitter & Reciever

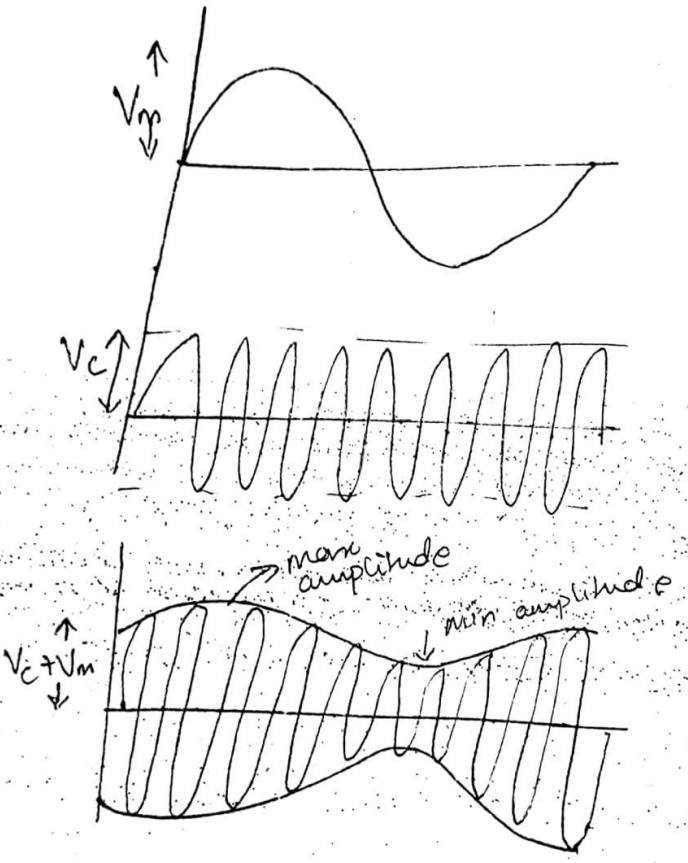
free space or air. hence it requires two antennas, one at transmitter & another at reciever end. The transmitter transmits the signal using transmitter antenna into free space. The reciever picks up the signal by means of recieving antenna.

Noise :- Noise is undesirable electrical energy that enters the Communication System. Noise can be natural or man-made. Natural ~~co~~ noise is produced in nature eg lighting during rainy season. Man made noise is the noise produced by electric ignition System of car etc

Reciever :- is a collection of electronic ckts to convert the signal back to the orginal information.

Amplitude Modulation

Amplitude of a carrier signal is varied in accordance with message signal (modulating signal keeping frequency & phase constant.



Equation of an AM signal

Instaneous value of modulating signal

$v_m = V_m \sin \omega_m t$

V_m = Max amplitude

v_m = instaneous amplitude

ω_m = angular frequency = $2\pi f_m$

f_m = frequency of modulating signal

instaneous value of carrier signal is

$v_c = V_c \sin \omega_c t$

V_c = max amplitude

v_c = instaneous amplitude

ω_c = angular frequency = $2\pi f_c$

f_c = frequency of carrier signal

$V_{AM} = V_c + v_m = V_c + V_m \sin \omega_m t$

Modulation Index: is ratio of modulating signal voltage to carrier signal voltage

$$m = \frac{V_m}{V_c}$$

Modulation index → 0 to 1.

Percentage modulation: $m \times 100 =$

Frequency Spectrum of the AM wave

→ $v_{AM} = V_{AM} \sin \omega_c t$

$$v_{AM} = (V_c + V_m \sin \omega_m t) \sin \omega_c t$$

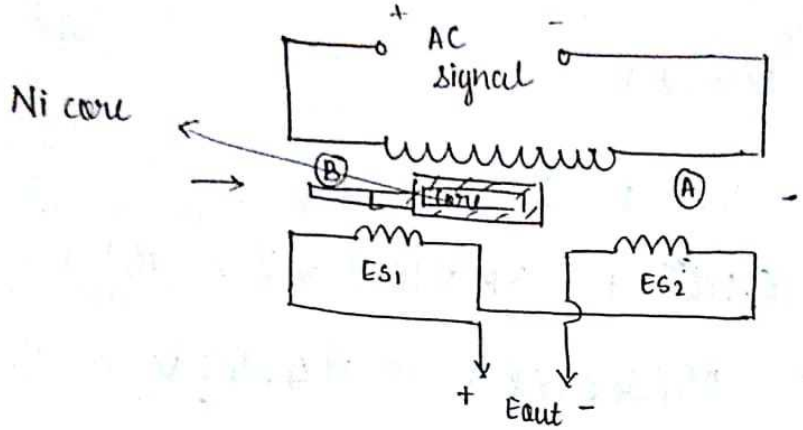
since $m = \frac{V_m}{V_c}$

$$v_{AM} = \left(V_c + mV_c \sin \omega_m t\right) \sin \omega_c t$$

$$= V_c \sin \omega_c t + \frac{mV_c}{} \sin \omega_m t \sin \omega_c t$$

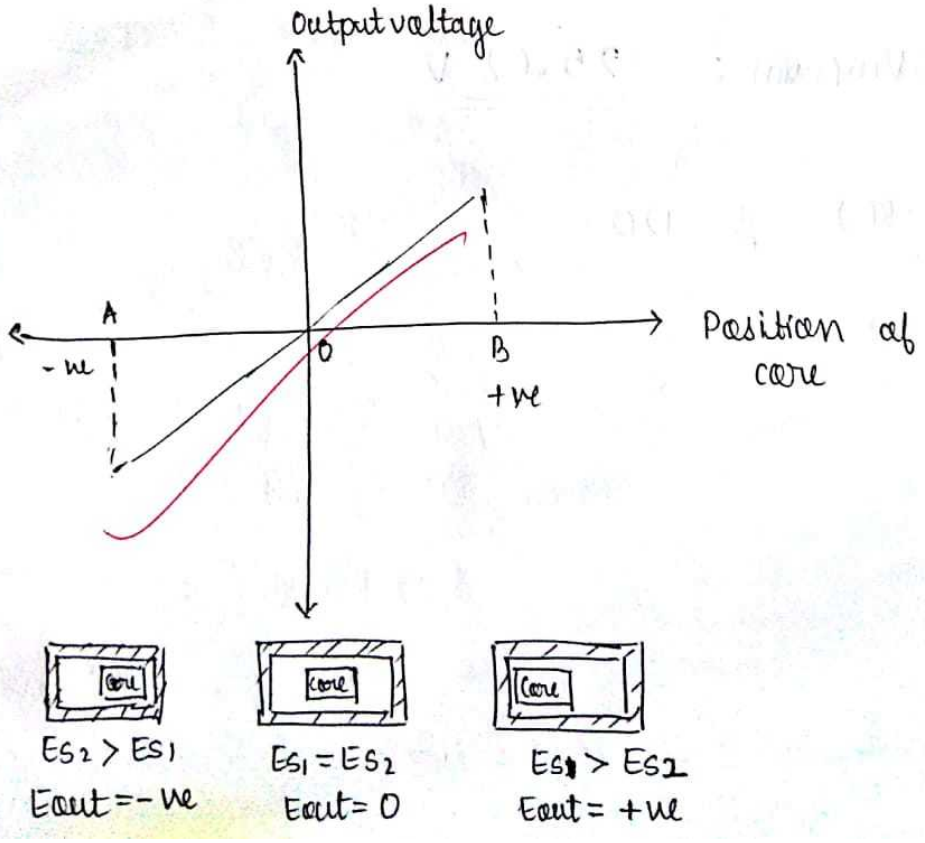
9(c)

1. LVDT (Linear Variable Differential transducer.



LVDT has a primary coil connect to the AC source. It has two secondary coils which have the same number of turns E_{S1} & E_{S2}. When the core is moved btw the primary & secondary coils, electric field is induced. The $E_{out} = E_{S1} - E_{S2}$.

10

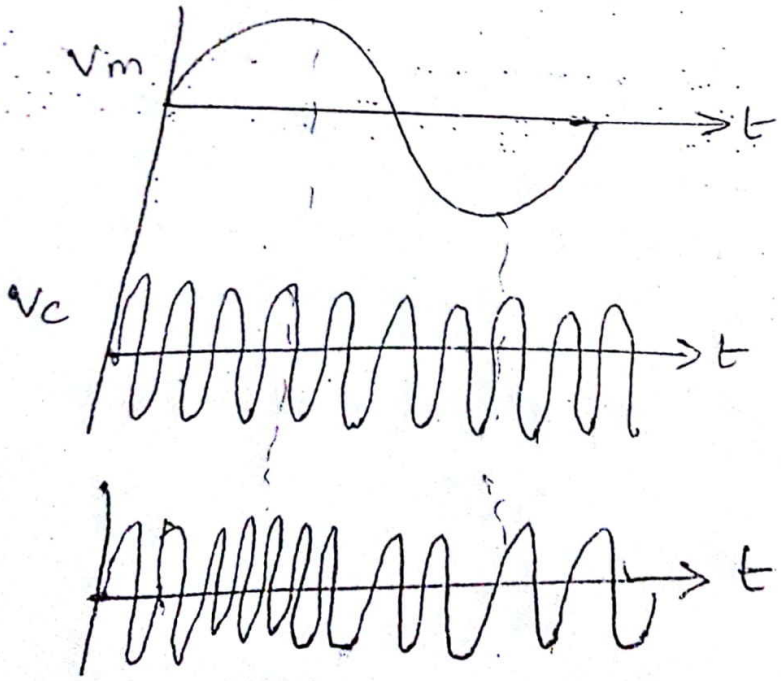


10(a)

	FM	AM
(i)	$V = A\sin(\omega_c t + m_f \sin\omega_m t)$	$V = V_c (1 + m\sin\omega_m t)\sin\omega_c t$
(ii)	Modulation index value is either one or more than one	Modulation index is always 0 to 1
(iii)	Bandwidth of FM is proportional to modulation index	B.W of AM signal is twice the modulating frequency. $B.W = 2f_m$
(iv)	Transmitted Power is independent of modulation index	Power is dependent on modulation index $P_t = P_c\left(1 + \frac{m^2}{2}\right)$

Frequency Modulation

In frequency modulation, the instaneous frequenc
of the carrier wave is varied in accordance with
the signal to be modulated keeping amplitud
constant.



instaneous frequency of an FM wave is given as

$$f = f_c (1 + K V_m \cos \omega_m t)$$

$f_c \rightarrow$ unmodulated carrier frequency

$V_m \cos \omega_m t \rightarrow$ instaneous modulating voltage

Maximum deviation δ is given by

$$\boxed{\delta = K V_m f_c}$$

Instantaneous amplitude of the FM is given

$$V_{FM} = A \sin[F(\omega_c, \omega_m)]$$

$F(\omega_c, \omega_m) \rightarrow$ function of ω_c & ω_m

$$= A \sin\theta \quad \text{where } \theta = F(\omega_c, \omega_m)$$

we know that

$$\theta = \int \omega \cdot dt = \int \omega_c (1 + K V_m \cos \omega_m t) \cdot dt$$

$$= \omega_c \left(t + \frac{K V_m \sin \omega_m t}{\omega_m}\right)$$

$$= \omega_c t + \frac{K V_m \omega_c \sin \omega_m t}{\omega_m}$$

$$= \omega_c t + \frac{K V_m f_c \sin \omega_m t}{f_m}$$

$$= \omega_c t + \frac{\delta}{f_m} \sin \omega_m t$$

modulation index $m = \frac{\delta}{f_m}$

$$= \omega_c t + m \sin \omega_m t$$

$$\boxed{V_{FM} = A \sin(\omega_c t + m \sin \omega_m t)}$$

Thermistor :-

→ It is a contraction of term 'Thermal Resistors'.

→ It is a two terminal semiconductor slab whose resistance decreases with temperature i.e Negative temperature Coefficient [NTC].

→ Materials used are oxides of Cobalt, Ni, Cu, Fe, Uranium and Manganese.

Principle of operation

The Resistance of Thermistor is given as

$$R = R_0 \exp\left[\beta\left(\frac{1}{T} - \frac{1}{T_0}\right)\right] \quad \text{—— (1)}$$

where R_0 = Resistance at $T_0(K)$

R = Resistance at $T(K)$ ⑥

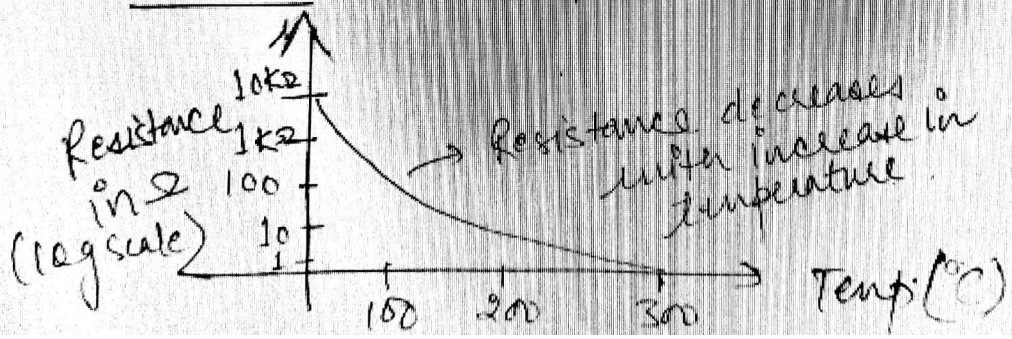
β = constant determined experimentally.

→ For large values of T, eq^n ① is approx as,

$$\left[R = R_0 \exp\left(\frac{B}{T}\right) \right]$$

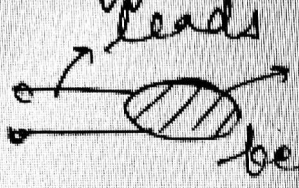
→ Symbol is → 

→ Resistance vs temp. characteristics of thermistor

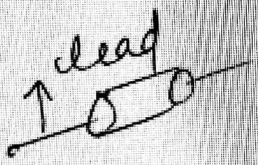


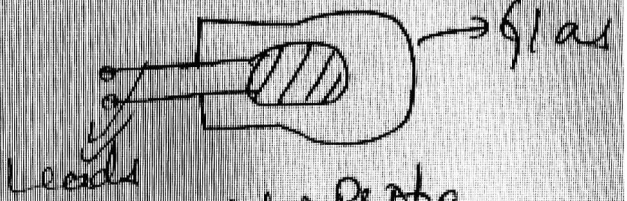
100 200 300

→ Different types of Thermistors are :—



(a) Bead Type





(b) Probe.