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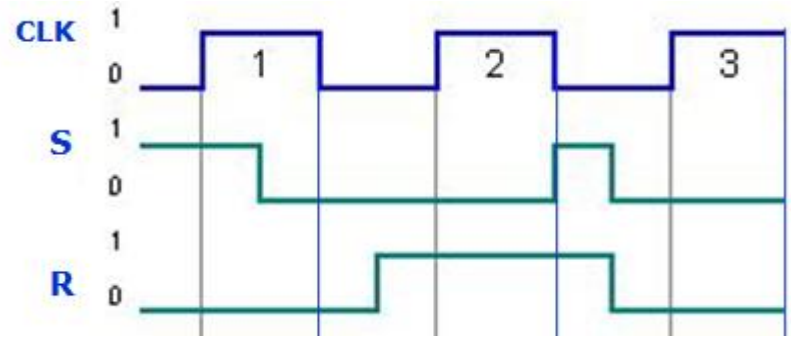
Internal Assesment Test - II

Sub:	**DIGITAL SYSTEM DESIGN**							Code:	18EE35
Date:	15/10/2019	Duration:	90 mins	Max Marks:	50	Sem:	3rd	Branch:	EEE

Answer Any **FIVE FULL** Questions

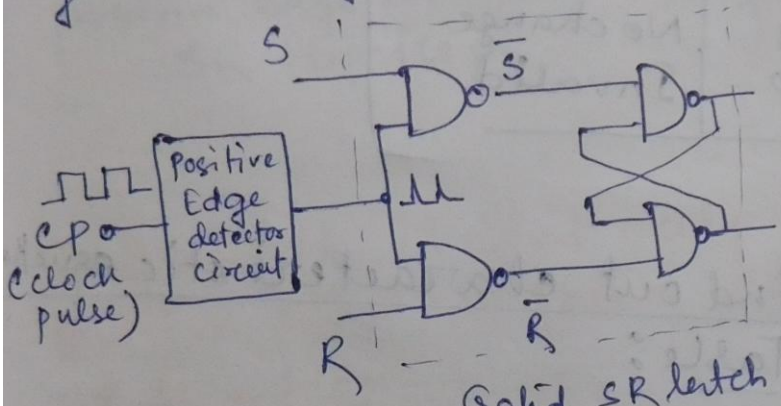
		Marks	OBE	
			CO	RBT
1	(a) Describe the working principle of SR Flip-flop with its truth table. (b) Distinguish between Flip-flop and Latch.	7+3=10	CO3	L2
2	(a) With a neat logic diagram describe the working of D flip-flop with truth table and derive the Characteristics Equation. (b) Distinguish between combinational circuit and sequential circuit.	6+4=10	CO3	L2
3	Explain the working of Master slave JK Flip-flop with waveforms and functional table (truth table) and show how the race around is overcome.	10	CO3	L4
4	(a) Analyze the role of SR Flip-flop in switch debouncer circuit. (b) Compare between Synchronous and Asynchronous sequential circuit with valid points.	7+3=10	CO3	L4
5	(a) Illustrate the significance of triggering in flip-flop and mention various methods for triggering. (b) Complete the output waveform for the following combination of SR Flip flop. Consider initial condition as 0. 	5+5=10	CO3	L3
6	Explain the operation of T Flip-flop with truth table. Derive the Characteristics table, Characteristics Equation and Excitation table for T flip flop.	10	CO3	L4

Answers:

1. a) Describe the working principle of SR Flip-flop with its truth table.

the logic symbol of ...

Ans: Logic Diagram of SR flip-flop using NAND gates are given below.



Gated SR latch

TT (Truth Table)

clk	S	R	Q_n
0	X	X	Q (No change)
↑	0	0	Q (No change)
↑	0	1	0 (RESET)
↑	1	0	1 (SET)
↑	1	1	X (Invalid)

Operation/working:

Case (I): When, cp = 0 means, no clock pulse is applied, then input will not effect the circuit so memory (Q) element will be shown at the o/p (Q_n = next state) means 'no change' i.e 1st row of Truth Table.

Case (II): When, S = R = 0 and cp = 1 means clk pulse is applied then again like SR gated latch at o/p it will show No change i.e $Q_n = 0$. This indicates 2nd row of Truth Table.

Case (III): When, S = 0, R = 1 & clock pulse is applied then at o/p RESET ($Q_n = 0$) condition will be reflected. This indicates the 3rd row of TT.

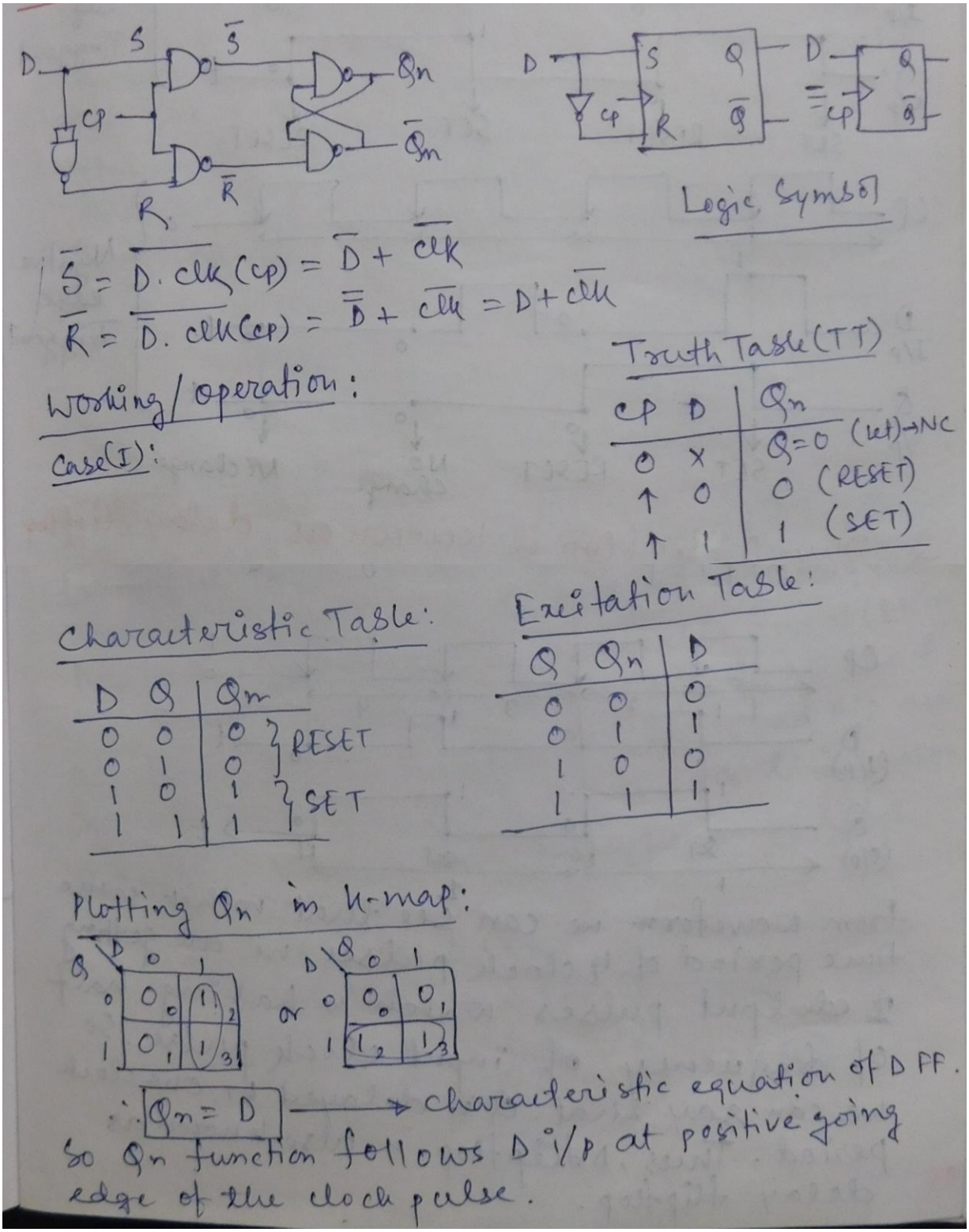
Case (IV): When, S = 1, R = 0 & clock pulse is applied then at o/p it will show 'SET' ($Q_n = 1$) condition. This indicates the 4rth row of TT.

Case (V): When, S = R = 1 & clock pulse is applied then at o/p it will show undefined or invalid which indicates 5th row of TT.

(b) Distinguish between Flip-flop and Latch.

Latch	flip-flop
(I) It does not require clock signals.	(I) A flip-flop have clock signal.
(II) A latch is an asynchronous device.	(II) A flip-flop is a synchronous device.
(III) Latches are transparent device i.e when they are enabled, the o/p changes immediately if the i/p changes.	(III) Here the change in o/p is determined by the transition of clock signal from low to high or high to low.
(IV) It is level sensitive device.	(IV) It is level as well as edge sensitive device.
(V) These are simpler to design as there is no clock signal.	(V) These are more complex to design as they have clock signal and it has to be routed carefully
(VI) The operation of the latch is faster as they don't have to wait for any clock signal.	(VI) Flip-flops are comparatively slower than latch due to clock signal.
(VI) The power requirement of a latch is less.	(VI) Power requirement of a flip-flop is more
(VII) A latch works based on the enable signal.	(VII) A flip-flop works based on the clock signal.

2. (a) With a neat logic diagram describe the working of D flip-flop with truth table and derive the Characteristics Equation.



(b) Distinguish between combinational circuit and sequential circuit.

Combinational Circuits	Sequential Circuits
(I) In these circuits, the output variables are at all times dependent on the combination of i/p variables.	(I) In these circuits, the output variables depend not only on the present input variables but they also depend upon the past history of these input variables.
(II) Memory unit is not required in these circuits.	(II) Memory unit is required to store the past of i/put variables in these circuits
(III) These are faster in speed because the delay between input and output is due to propagation delay of gates.	(III) These are slower than the combinational circuits.
(IV) These circuits are easy to design.	(IV) These circuits are harder to design.
(V) Example: Parallel Adder	(V) Example: Serial Adder.

3. Explain the working of Master slave JK Flip-flop with waveforms and functional table (truth table) and show how the race around is overcome.

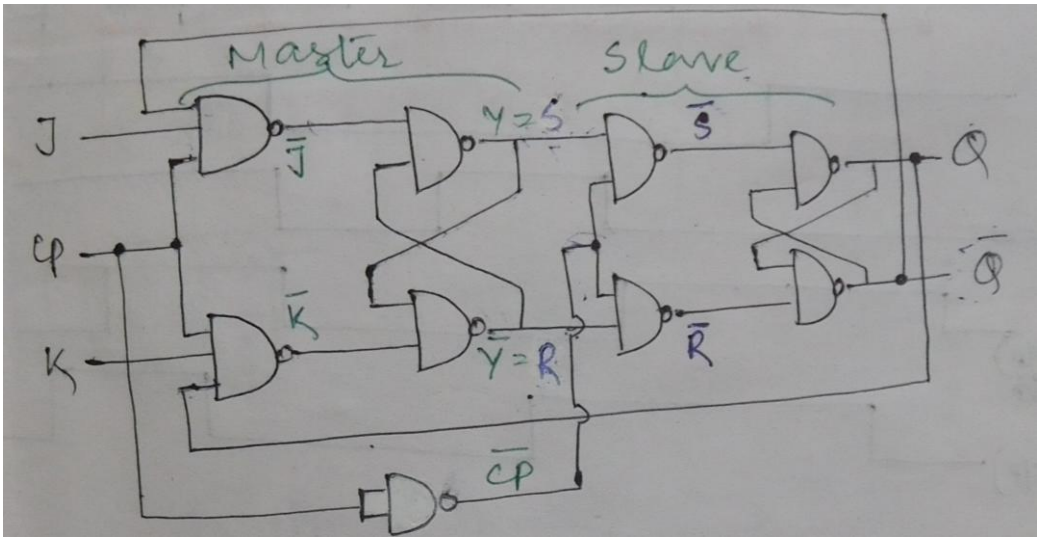


fig. shows the JK master slave flip-flop. which consists of 2 flip-flops named as one is Master another is slave. slave always follows master. Both the flip-flops are positive level triggered but an inverter is connected to the clock input of the slave flip-flop which forces it to triggers at the negative level. Therefore, the information present at the J and K inputs is transmitted to the o/p of master flip-flop on the positive clock pulse and it is held there until the negative clock pulse occurs, after which it is allowed to pass through to the output of the slave FF means slave flip-flop uses the SR input at the negative clock pulse to determine its o/p state Q and $\overline{Q}$.

Case(I): When, J=K=0, the o/p of master remains same at the +ve clock. Thus the o/p of slave also remains same at the -ve clock.

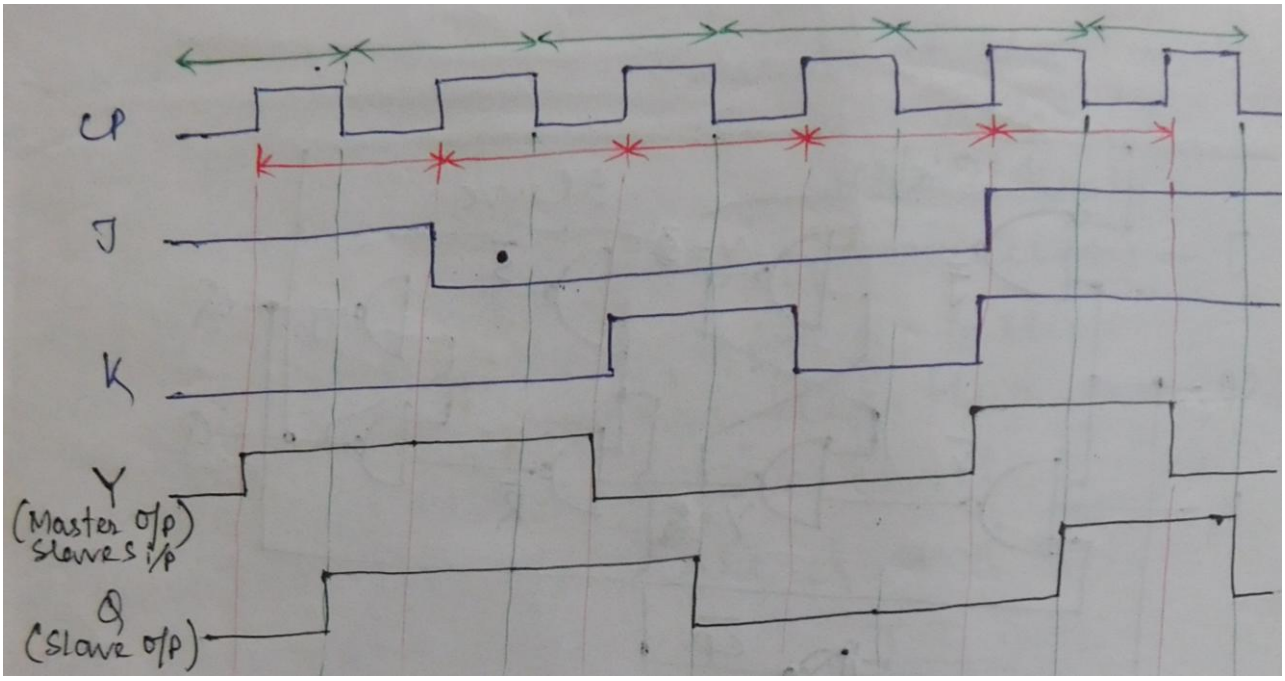
Case(II): When, J=0 & K=1, the master resets on the +ve clock. The high $\overline{Y}$ o/p of master goes to the R i/p of the slave. So, at -ve clock slave resets, again copying the action of the master.

case(III): When, J=1 & K=0, the master sets on the positive clock. The high Y o/p of master drives the S i/p of the slave, so at -ve clock slave sets, copying the action of master.

case(IV): When, J=K=1, master toggles on the positive clock and slave then copies the o/p of master on the negative clock.

TT

	CLK	J	K	Q_n
(I)	⊓⊔	0	0	Q (NC)
(II)	⊓⊔	0	1	0 (RESET)
(III)	⊓⊔	1	0	1 (SET)
(IV)	⊓⊔	1	1	$\overline{Q}$ (Toggle)



In JK flip-flop as we know, at J=K=1 condition, a continuous toggling is happening at the output side which is known as "race around condition". This condition can be avoided by using three methods as

i) Keeping propagation delay higher than clock period.
ii) Using of edge triggered clock pulses for the operation.
iii) Using Master Slave flip-flop.

However, from the above timing diagram it is clearly seen that at J=K=1 condition, there is no chance of toggling at the output as master flip-flop works at positive level triggered clock pulse and slave flip-flop works at negative clock pulse simeltaneously. So by using the master slave flip-flop we can avoid this race around condition at J=K=1 condition.

4. (a) Analyze the role of SR Flip-flop in switch debouncer circuit.

Ans. In a digital system, usually push button keys are used as a interfacing key. When these push button keys are pressed, then it bounces a few times, means closing and opening of the contact are randomly changed before providing a steady reading. So reading taken during this bouncing period may be faulty. This problem is known as key debounce which is undesirable and it must be avoided.

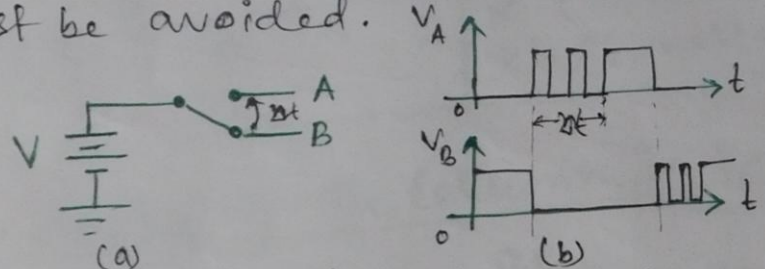


fig 1 Effect of key debounce.

One way to avoid key debounce problem is to use SR latch. The circuit which is used to avoid keybounce with SR latch is called a switch debouncer. Here, Fig.1(a), shows a switch which is connected to B terminal so, B is 1 and A is 0. When it moves from B to A then during Δt time period it will bounces and a toggle condition is occured. So two pull down resistors are connected across the i/p terminal of SR latch as shown in fig.2. When key is at position A then S=1 and Q=1 mean V. When transition happens between A to B then

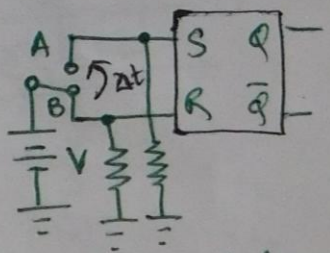


Fig 2. Switch debouncer

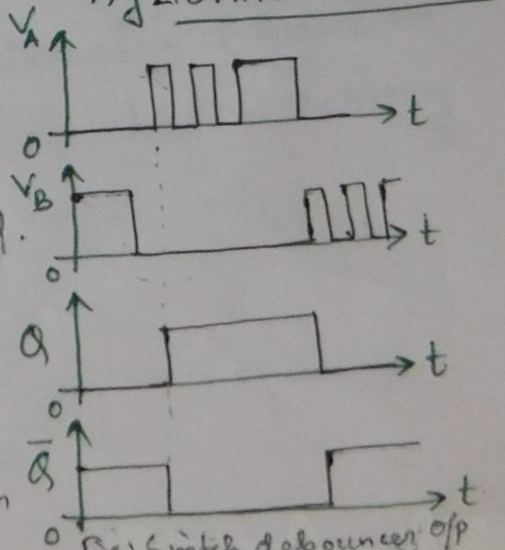


Fig: Switch debouncer o/p

it will take some time (let n sec.). During that time position A and B both are in high impedance state (means no current will flow). Due to these resistors (pull down) these high impedances are pulled down to zero. So whenever the contact point is in between A and B then i/p of SR latch will be zero which will maintain the steady state o/p of the latch.

(b) Compare between Synchronous and Asynchronous sequential circuit with valid points.

Synchronous Circuits	Asynchronous Circuits
(I) In these circuits, memory elements are clocked flipflops.	(I) In these circuits, memory elements are either unclocked flip flops or time delay elements.
(II) Here, the change in input signals can affect memory element upon activation of clock signal	(II) Here, the change in input signals can affect memory element at any instant of time.
(III) The maximum operating speed of clock depends on time delays involved.	(III) Because of absense of clock, these circuits can operate faster than synchronous circuits.
(IV) Easier to design.	(IV) More difficult to design.

5. (a) Illustrate the significance of triggering in flip-flop and mention various methods for triggering.

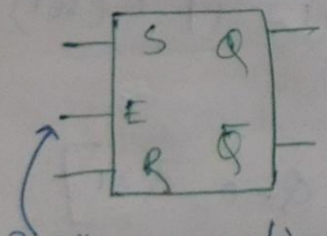
Ans: The o/p of a flipflop can be changed by bringing a small change in the input signal. This small change can be brought with the help of clock pulse or commonly known as a trigger pulse. When such a trigger pulse is applied to the i/p, the o/p changes accordingly and thus the flip-flop is said to be triggered.

Types of triggering method: There are two types of triggering method. These are →

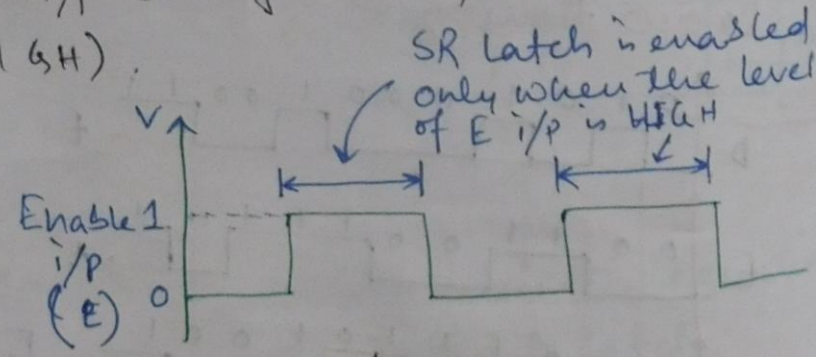
(I) Level Triggering.
(II) Edge Triggering.

① Level Triggering: Here the output state is allowed to change according to inputs when active level (either positive or negative) is maintained at the enable i/p. There are two types of level triggered latches:

(a) Positive level triggered: The o/p of latche responds to the i/p changes only when its enable input is 1 (HIGH).

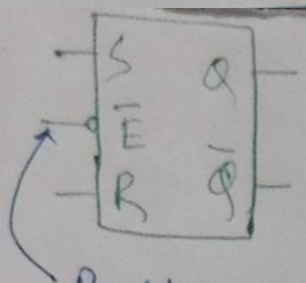


Positive level trigger Logic Symbol



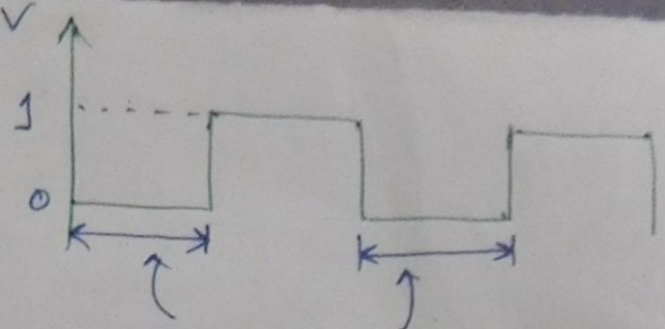
Positive level Triggering

(b) Negative level Triggered: Here the o/p of latch responds to the i/p changes only when its enable i/p is 0 (Low).



Bubble represents negative level triggering.

Logic Symbol

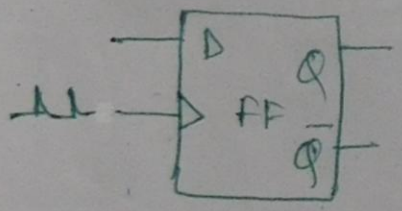


SR Latch is enabled only when the level of E input is Low.

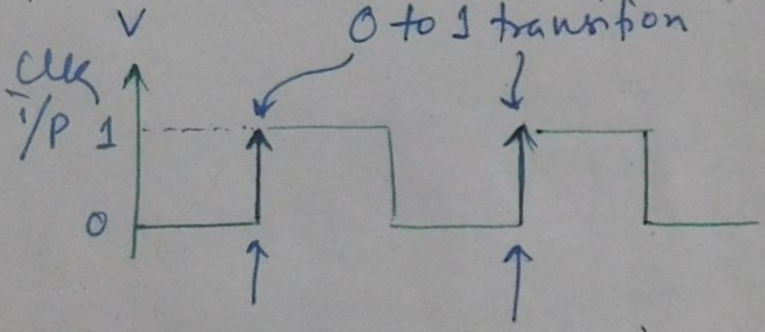
Negative level triggering

(II) Edge Triggering: Here, the output respon to the changes in the input only at the positive or negative edge of the clock pulse at the clock input. There are two types of edge triggering. These are →

(a) Positive Edge Triggering: Here, o/p responds to the changes in the i/p only at the positive edge of the clock pulse at the clock input.

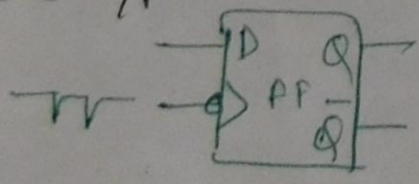


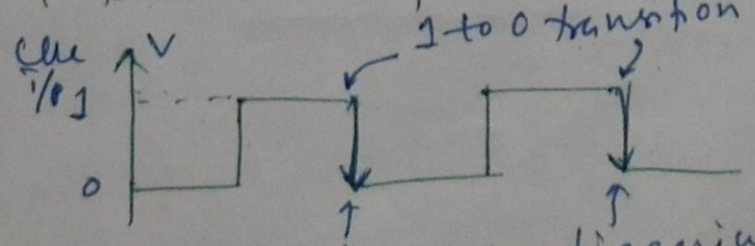
Positive edge triggered D FF



Positive edge triggering

(b) Negative Edge Triggering: Here, o/p responds to the changes in the i/p only at the negative edge of the clock pulse at the clock i/p.

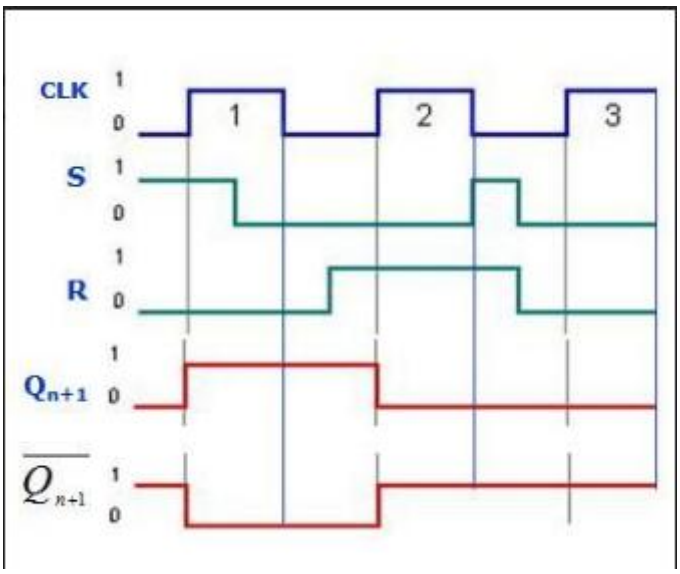




Negative Edge triggered D FF

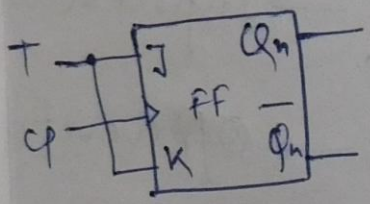
Negative Edge triggering

(b) Complete the output waveform for the following combination of SR Flip flop. Consider initial condition as 0.



6. Explain the operation of T Flip-flop with truth table. Derive the Characteristics table, Characteristics Equation and Excitation table for T flip flop.

Ans: T flip-flop is known as "Toggle flip-flop. It is like JK flip-flop. It is basically a single input version of JK flip-flop. This is a modified version of JK flip-flop that can be obtained by connecting both inputs J and K together. This flip-flop has only one input along with the clock input.



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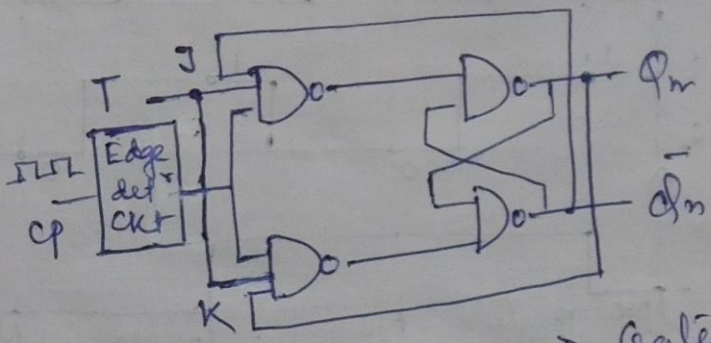

Fig: T flip-flop using NAND Gates.

Working / Operation:

Case (I): When, T = 0 then J = K = 0 and hence there is no change in the output. This is satisfying 1st row of TT.

Case (II): When, T = 1, then J = K = 1 and hence output toggles which is satisfying 2nd row of TT.

Truth Table (TT)

clk	T	Q_n (next state)
↑	0	No change (Q)
↑	1	$\bar{Q}$
0	×	No change

⇒

Characteristic Table

	(PS)	(NS)
T	Q	Q_n
0	0	0 (No change)
0	1	1 (No change)
1	0	1 (Toggle)
1	1	0 (Toggle)

Excitation Table

Q	Q_n	T
0	0	0
0	1	1
1	0	1
1	1	0

from characteristic Table:

$$Q_n = Q\bar{T} + \bar{Q}T$$

↑ characteristic equ^n of T FF

Q \ T	0	1
0	0 (0)	1 (1)
1	1 (2)	0 (3)