CMR INSTITUTE OF TECHNOLOGY

Solutons of Internal Assesment Test - III				
Sub:	**DIGITAL SYSTEM DESIGN**		Code:	18EE35
Sem:	3rd (A Section)	Branch:	EEE	
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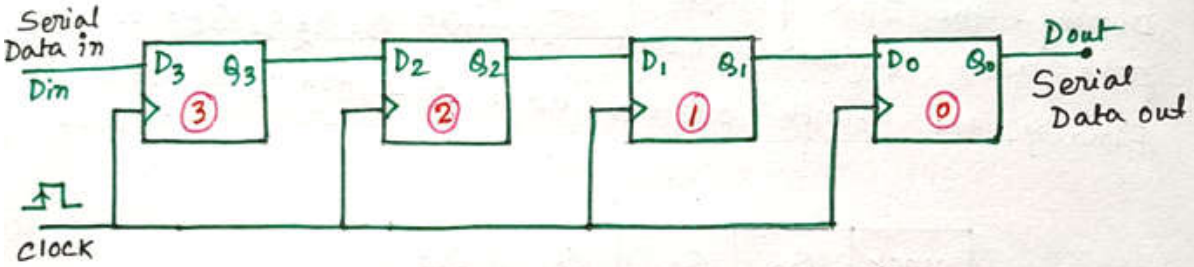
1. Draw the logic diagram for the following modes of Shift Register:

SISO, SIPO, PISO, PIPO

Solution:

→ (i) SISO :-



→ For SISO, the data bits are serially entered one by one into the D flip-flop.

→ SISO is constructed by using positive edge triggered D Flip flops.

→ Output of each flip flop is connected to the input of next flipflop.

→ Each Flip-flop is connected with a common synchronizing clock pulse.

→ Upon occurance of each positive edge of the clock, the content of each flip flop is shifted one bit position to the right.

Eg. Let us consider, initial register is cleared.

So, $Q_3 Q_2 Q_1 Q_0 = 0000$.

Now, Let us serially data 1111 is applied. When data 1111 is applied serially, i.e left most 1 is applied as Din. At the arrival of 1st positive edge of clock:-

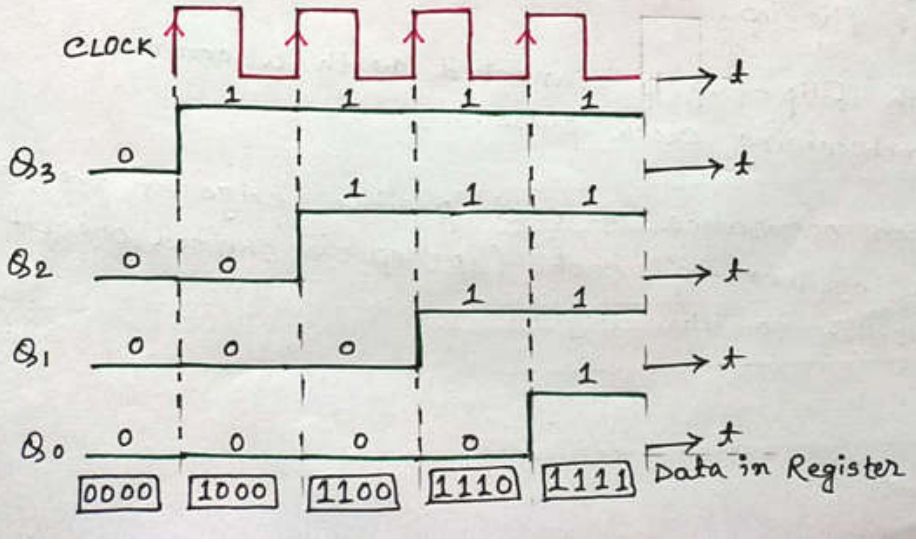
$\therefore$ Din = 1, $Q_3 Q_2 Q_1 Q_0 = 1000$

During, the 2nd positive edge of clock, the Q_2 Flipflop sets and Register content becomes. $Q_3 Q_2 Q_1 Q_0 = 1100$.

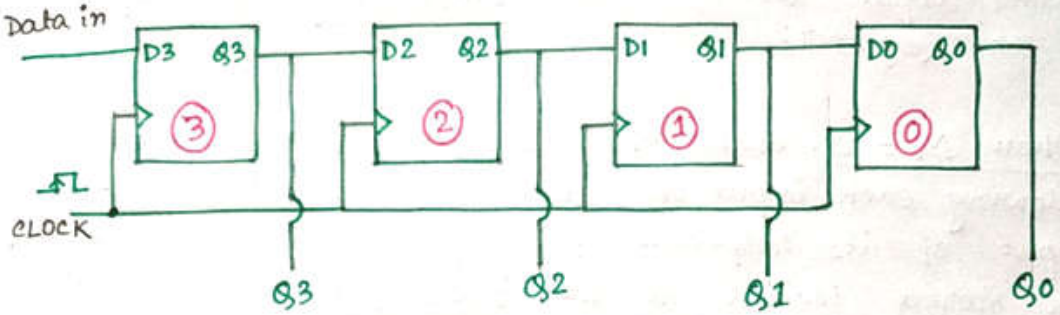
During, the 3rd positive edge of clock, the Q_1 Flipflop sets and Register content becomes $Q_3 Q_2 Q_1 Q_0 = 1110$.

Finally, the fourth positive edge of clock gives $Q_3 Q_2 Q_1 Q_0 = 1111$

CLOCK	Q_3	Q_2	Q_1	Q_0
–	0	0	0	0
1↑	1	0	0	0
2↑	1	1	0	0
3↑	1	1	1	0
4↑	1	1	1	1

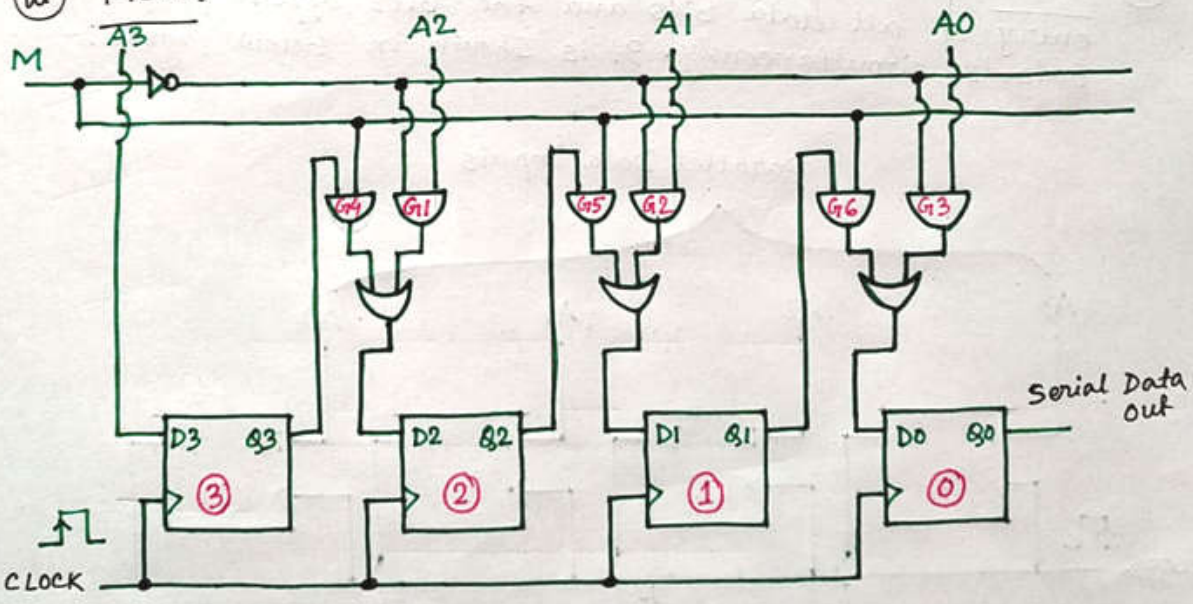


(ii) SIPO :-



In this case, the data bits are entered into the Register in the same manner as discussed for the case of SISO. But the outputs are collected in parallel. Once the data are stored, each bit appears on its respective output line and all the bits are available simultaneously.

(iii) PISO :-



In this type, the bits are entered in parallel. The above figure shows a 4 bit parallel in serial out shift register.

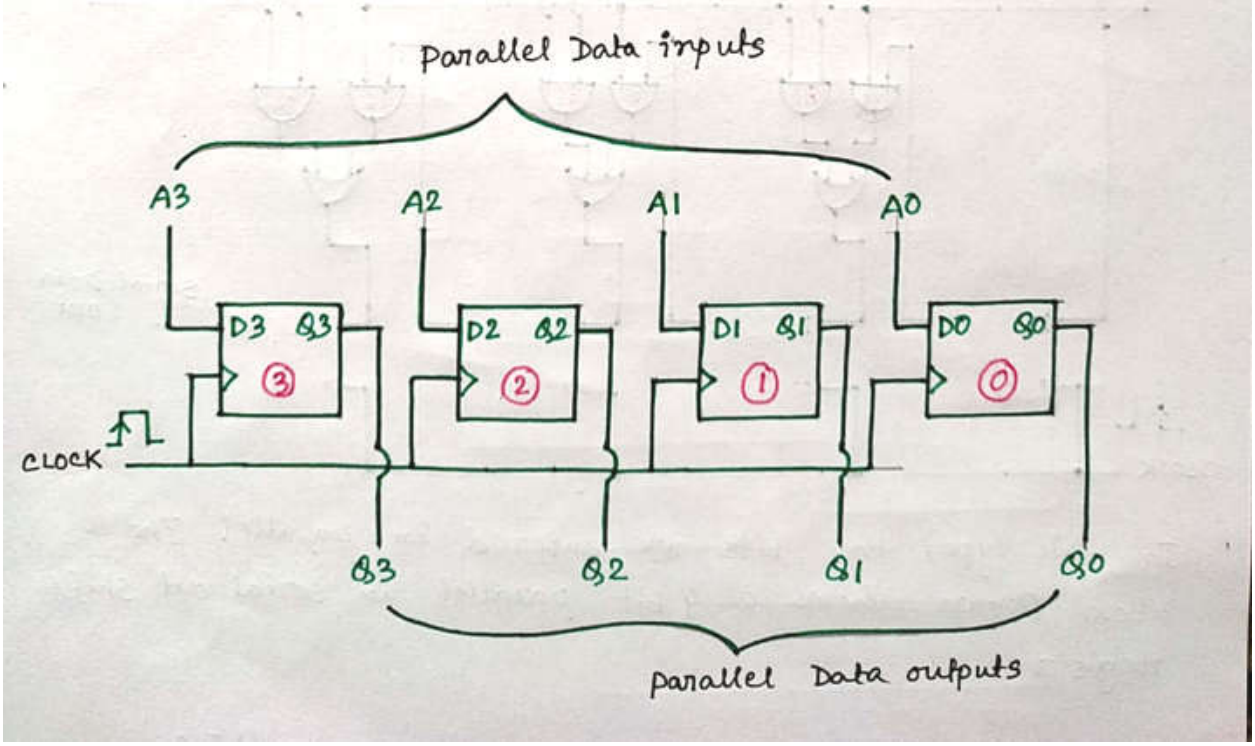
P. T. O →

→ There are 4 input lines A3, A2, A1, A0. M is the control input which decides shift or loading operation of the Register.

→ When M = 0, Gates G1, G2 and G3 are enabled allowing each input data bit to be applied to D input of its respective flip flop. Thus all four bits are stored / loaded to the flip flops.

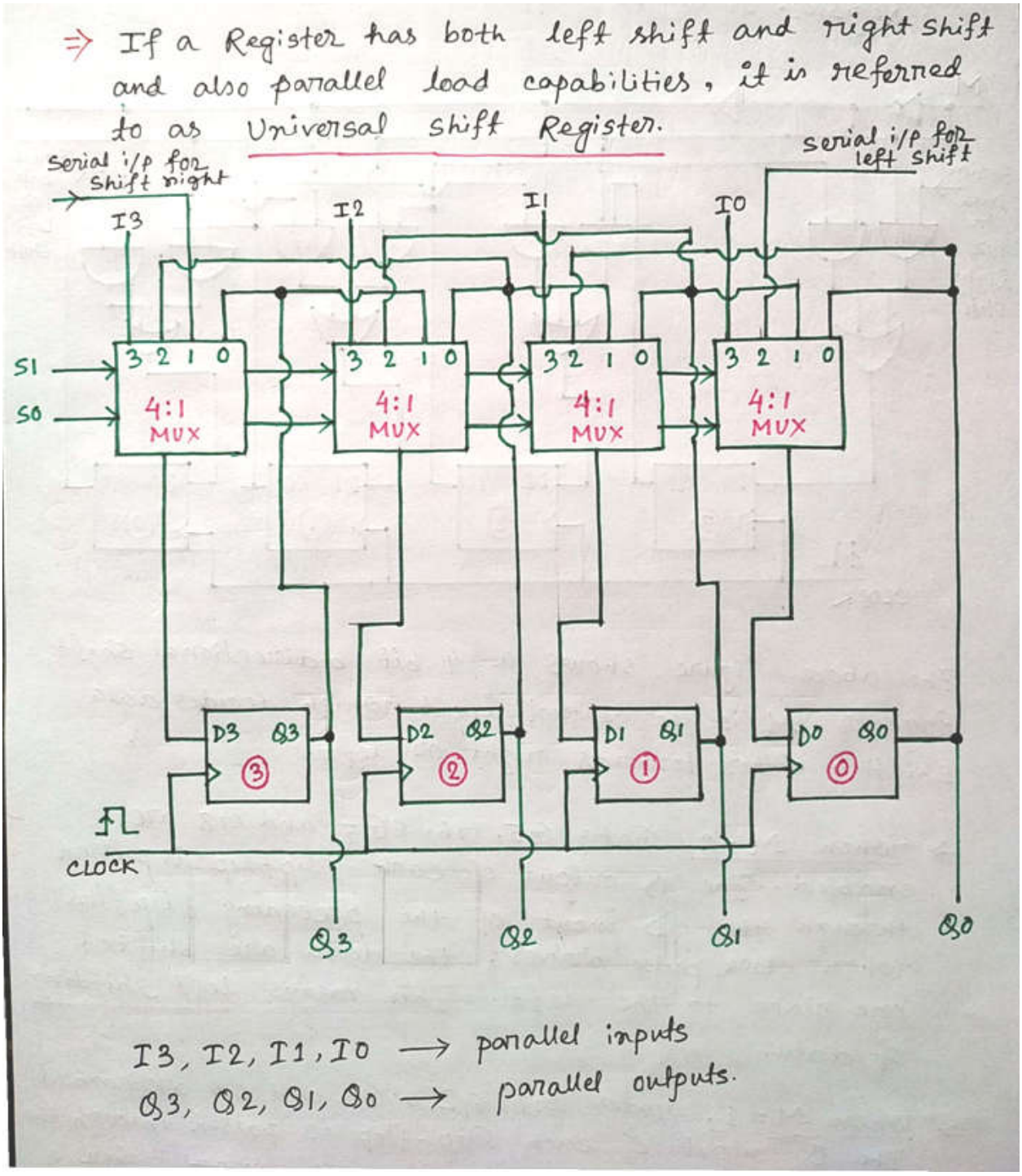
→ when M = 1, gates G1, G2 and G3 are disabled and gates G4, G5 and G6 are enabled. This allows the data bits to shift right from one stage to the next. This corresponds to shifting of data.

(iv) PIPO :- In PIPO shift register, there is simultaneous entry of all data bits and the bits appear on parallel outputs simultaneously. It is shown in below figure :-



2. With neat logic diagram explain the operation of Universal shift register with Mode control table.

Solution:



→ It consists of 4 flip flops and 4 Multiplexers. The four Multiplexers have two common select inputs S1 and S0. and they select appropriate input for D flip-flop. The below table shows the register operation depending on the select lines of multiplexer.

Mode Control		Register Operation
S1	S0	
0	0	No change
0	1	Shift Right
1	0	Shift Left
1	1	parallel Load

→ When $S_1S_0 = 00$, input 0 is selected and the present value of the register is applied to the D inputs of the flip-flops. This results no change in Register value.

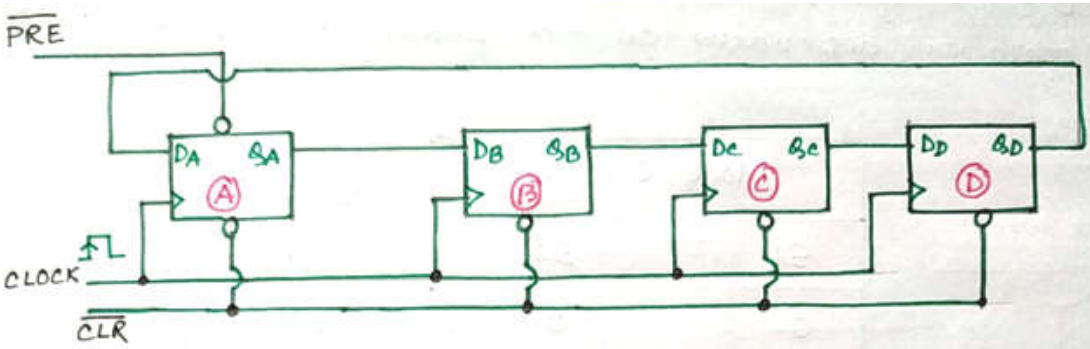
→ When $S_1S_0 = 01$, input 1 is selected and circuit connections are such that it operates as a right shift Register.

→ When $S_1S_0 = 10$, input 2 is selected and circuit connections are such that it operates as a left shift Register.

→ Finally when $S_1S_0 = 11$, the binary information on the parallel input lines is transfered into the register simultaneously and it is a parallel load operation.

3. Analyze the operation of Ring Counter (MOD-4 or 4 bit) with logic diagram, truth table, timing diagram and state diagram.

Solution:



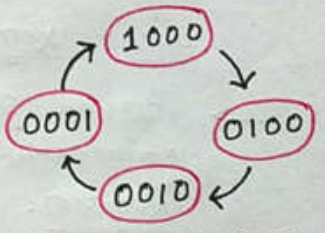
→ The above shows the diagram for 4 bit ring counter where Q output of each stage is connected D input of next flip-flop and the output of last stage is fed back to the input of first stage.

→ $\overline{PRE}$ makes the output of first stage as 1 and the remaining outputs are made 0 by $\overline{CLR}$. Let us consider initially $Q_A Q_B Q_C Q_D = 1000$.

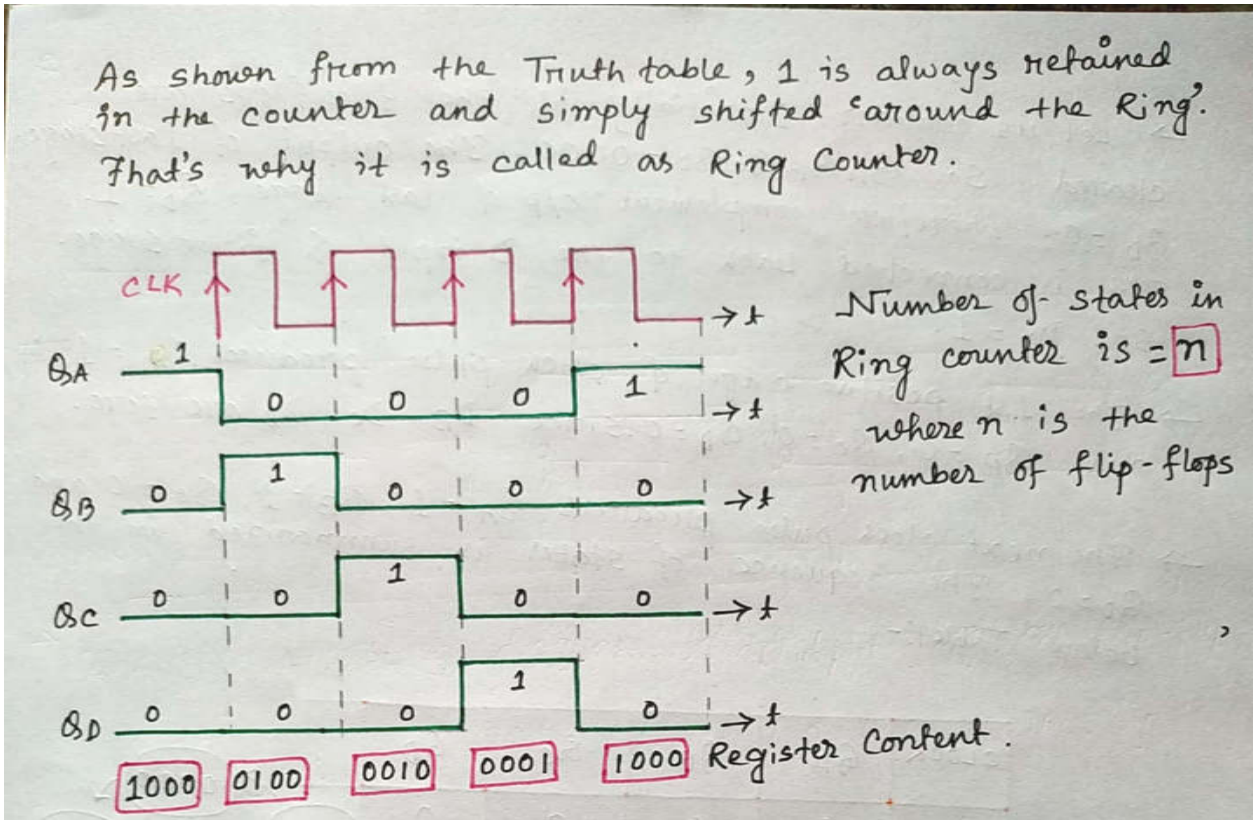
→ The 1st clock pulse produces $Q_B = 1$ and the remaining outputs are 0. According to the clock pulses, a sequence of four states are produced which is listed below:-

CLOCK	Q_A	Q_B	Q_C	Q_D
–	1	0	0	0
1↑	0	1	0	0
2↑	0	0	1	0
3↑	0	0	0	1
4↑	1	0	0	0

Truth Table

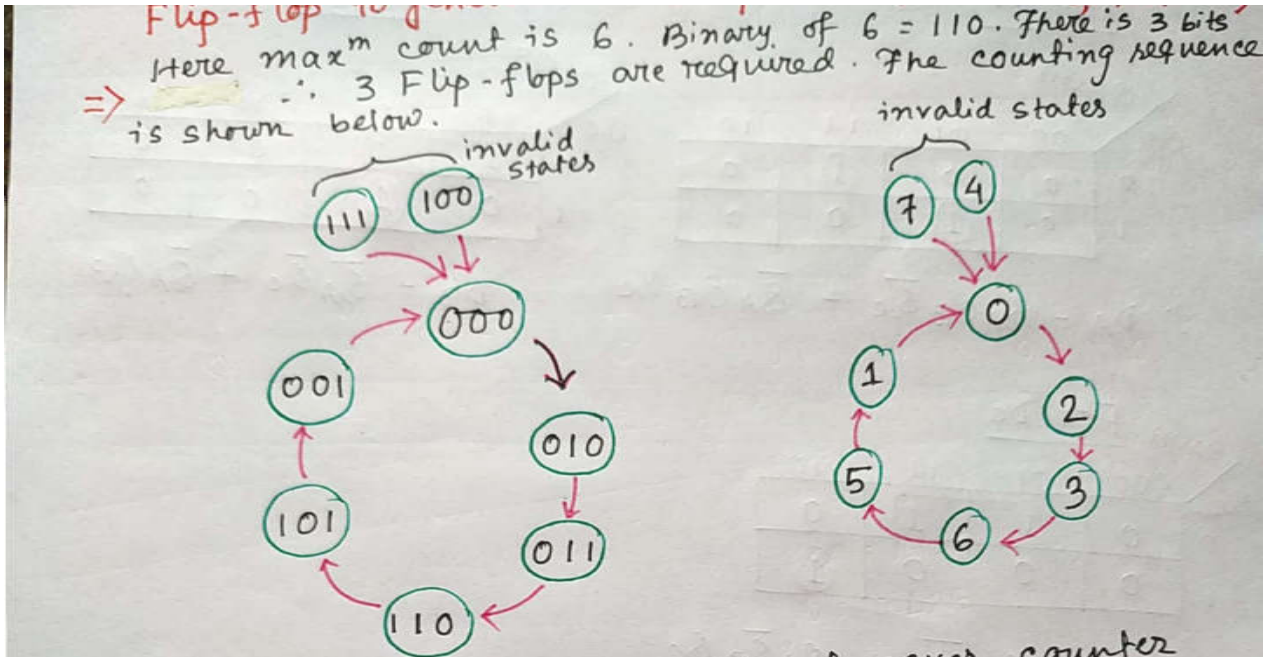


State Diagram



4. Design a synchronous counter with counting sequence 0, 2, 3, 6, 5, 1, 0… using D Flip-flop.

Solution:



* * Here, we are considering that whenever counter gets an invalid state then it will reset to initial value.

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

	Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	D_A	D_B	D_C
	0	0	0	0	1	0	0	1	0
	0	0	1	0	0	0	0	0	0
	0	1	0	0	1	1	0	1	1
	0	1	1	1	1	0	1	1	0
invalid	1	0	0	0	0	0	0	0	0
	1	0	1	0	0	1	0	0	1
	1	1	0	1	0	1	1	0	1
invalid	1	1	1	0	0	0	0	0	0

For D_A

Q_C \ Q_AQ_B	00	01	11	10
0	0	0	1	0
1	0	1	0	0

$\therefore D_A = Q_A Q_B \overline{Q_C} + \overline{Q_A} Q_B Q_C$

For D_B

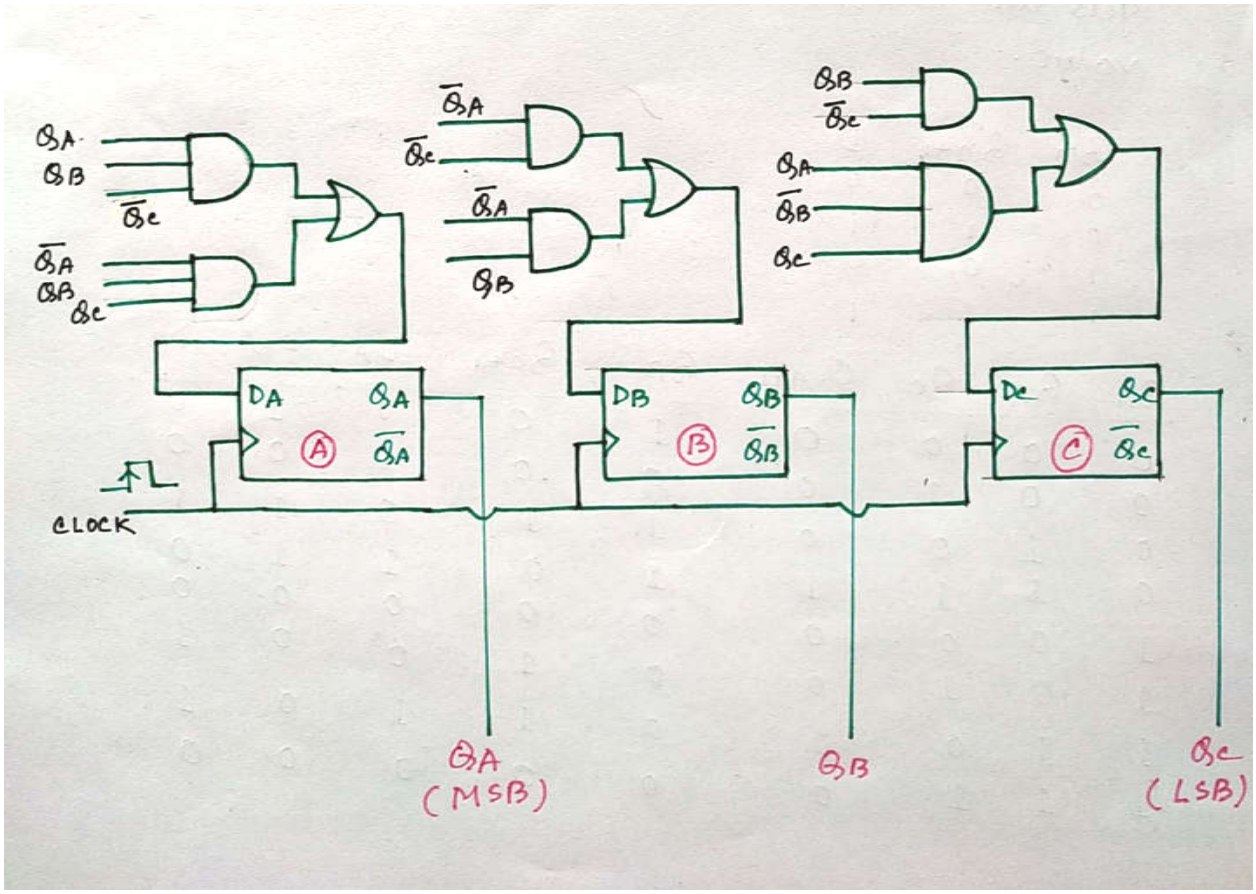
Q_C \ Q_AQ_B	00	01	11	10
0	1	1	0	0
1	0	1	0	0

$\therefore D_B = \overline{Q_A}\,\overline{Q_C} + \overline{Q_A} Q_B$

For D_C

Q_C \ Q_AQ_B	00	01	11	10
0	0	1	1	0
1	0	0	0	1

$D_C = Q_B \overline{Q_C} + Q_A \overline{Q_B} Q_C$



5. Design a Synchronous MOD-6 counter using T flip-flop.

Solution:

For designing of counter using clocked T flip-flop we have to follow a similar procedure as that for the design using clocked JK flip-flop.

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Table 4.10.2

Step 1 : Find number of flip-flops required to build the counter.

Flip-flops required are : $2^n \geq N$

Here $N = 6 \quad \therefore \quad n = 3$

i.e. three flip flops are required.

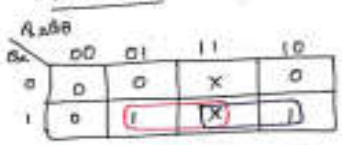
Step 2 : Write an excitation table for T flip-flop.

Step 3 : Determine the transition table.

Present state			Next state			Flip-flop inputs		
Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	T_A	T_B	T_C
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	0	0	0	1	0	1
1	1	0	x	x	x	x	x	x
1	1	1	x	x	x	x	x	x

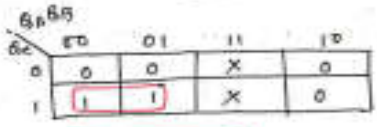
K-Map simplification

for T_A



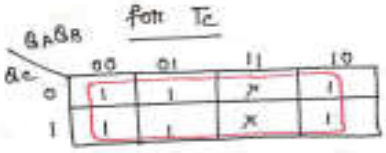
$T_A = Q_B Q_C + Q_A Q_C$

for T_B



$T_B = \overline{Q_A}\, Q_C$

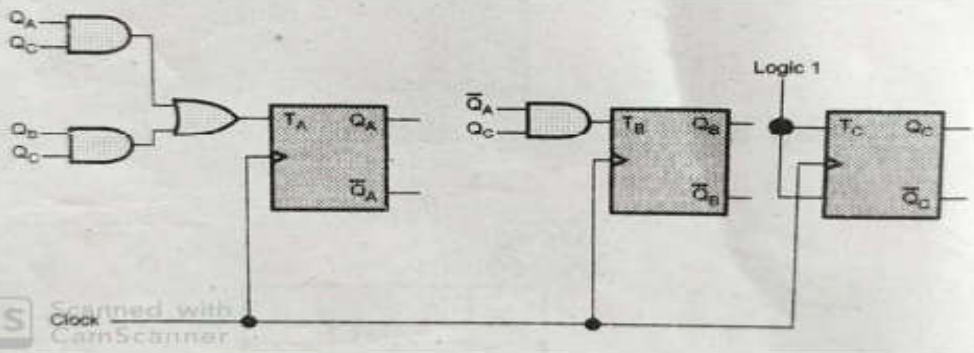
for T_C



$T_C = 1$

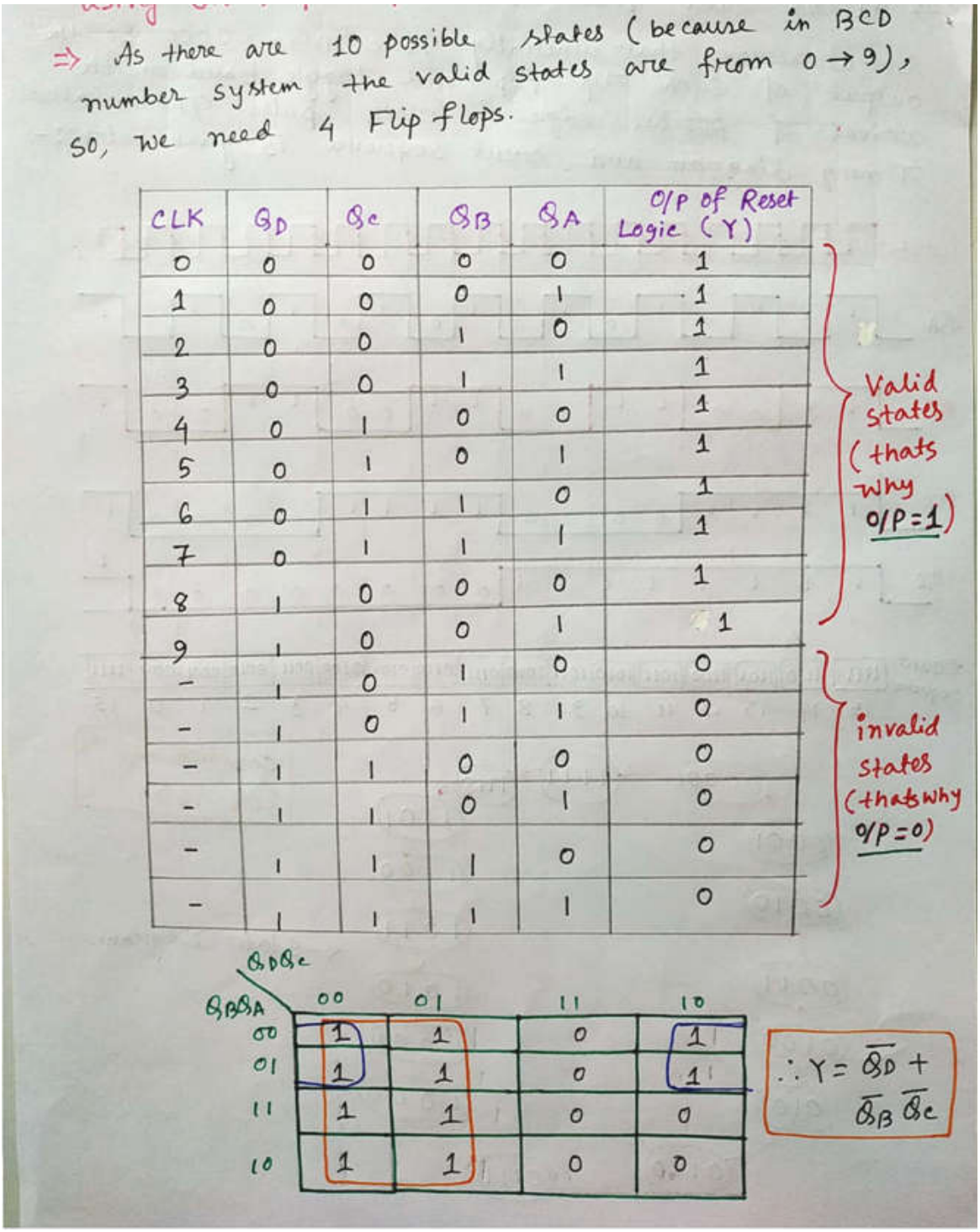
Step 5 : Implement the counter.

Q_A (MSB), Q_C (LSB)



6. Design a MOD-10 (BCD) Asynchronous counter with logic diagram, timing diagram and state diagram.

Solution:

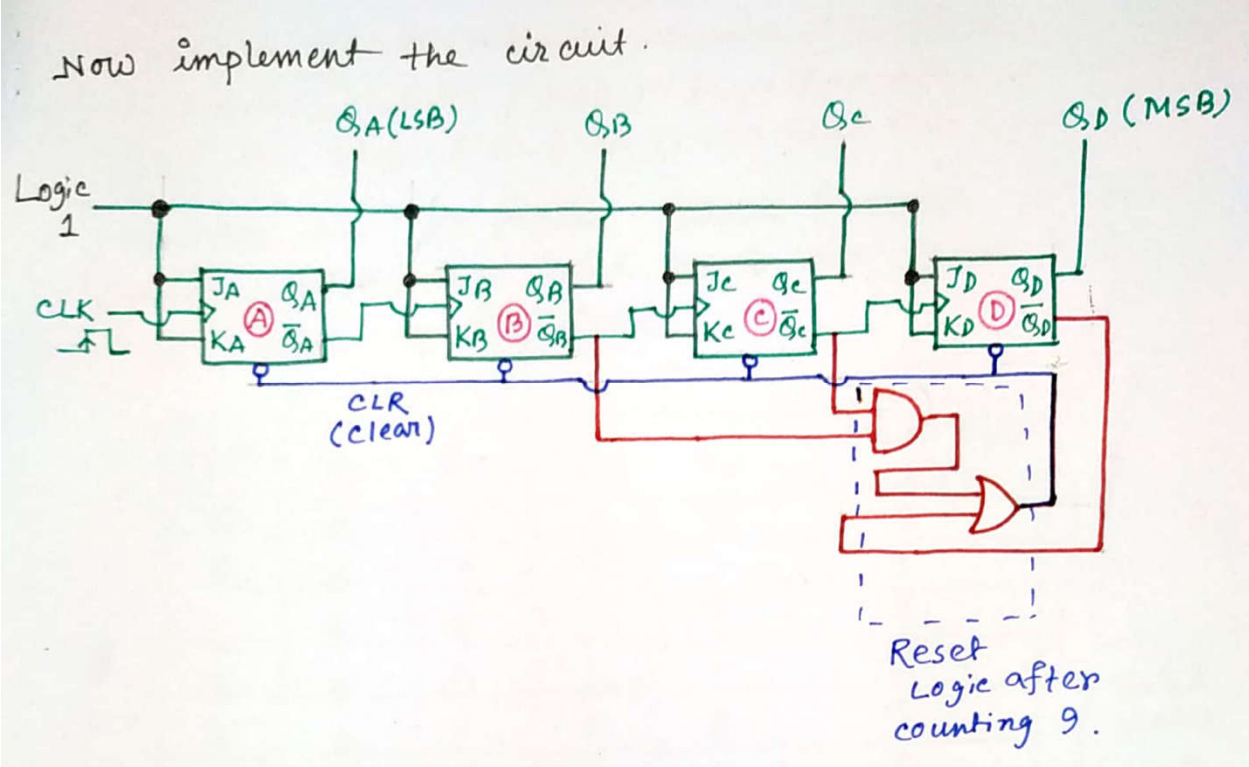


⇒ As there are 10 possible states (because in BCD number system the valid states are from 0 → 9), so, we need 4 Flip flops.

CLK	Q_D	Q_C	Q_B	Q_A	O/P of Reset Logic (Y)	
0	0	0	0	0	1	Valid states (thats why O/P=1)
1	0	0	0	1	1	
2	0	0	1	0	1	
3	0	0	1	1	1	
4	0	1	0	0	1	
5	0	1	0	1	1	
6	0	1	1	0	1	
7	0	1	1	1	1	
8	1	0	0	0	1	
9	1	0	0	1	1	
-	1	0	1	0	0	invalid states (thatswhy O/P=0)
-	1	0	1	1	0	
-	1	1	0	0	0	
-	1	1	0	1	0	
-	1	1	1	0	0	
-	1	1	1	1	0	

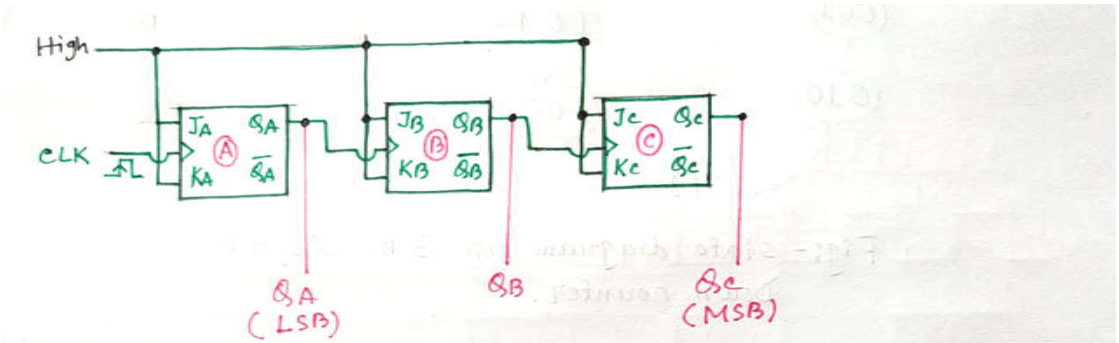
$Q_B Q_A$ \ $Q_D Q_C$	00	01	11	10
00	1	1	0	1
01	1	1	0	1
11	1	1	0	0
10	1	1	0	0

$\therefore Y = \overline{Q_D} + \overline{Q_B}\,\overline{Q_C}$



7. Explain the working of 3-bit Asynchronous down counter configured using JK flip-flop with logic diagram, timing diagram and state diagram.

Solution:



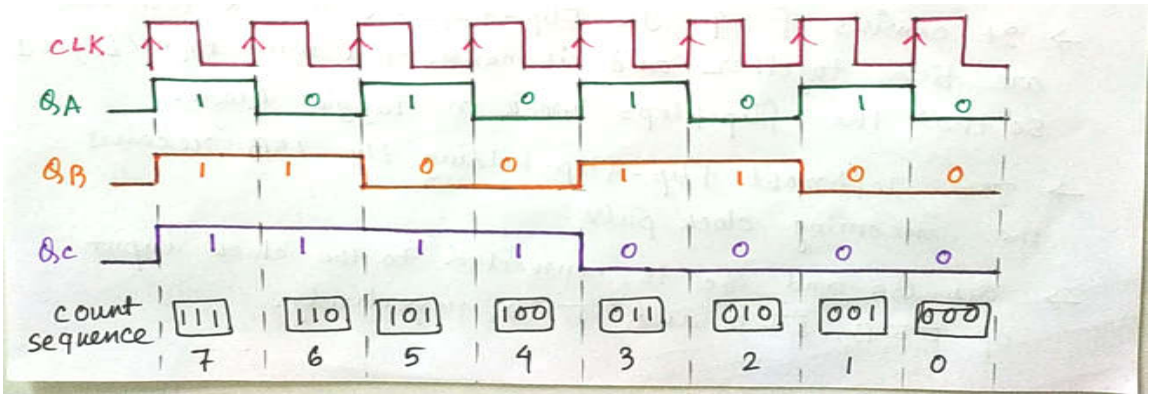
→ It consists of a series of 3 JK Flip-flops. J and K terminals are tied together and is connected to Logic 1. so that the flip-flops work in Toggle Mode.

→ The flip-flop holding the LSB receives the incoming clock pulse.

→ Q_A, Q_B is connected to the clock input of FFB and FFC, respectively.

→ It is a 3 Bit counter. so, number of possible states are $8(2^3)$. It can count from $7 \rightarrow 0$.

→ Let us assume that initially $Q_C Q_B Q_A = 000$. The output will toggle based on the positive edge of clock which is shown below:-



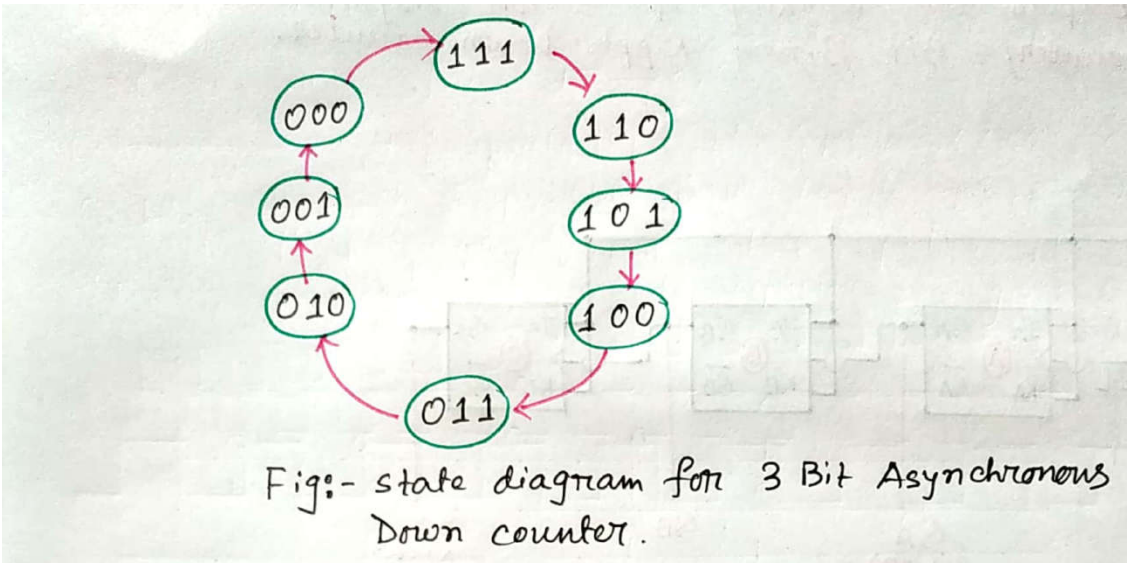


Fig:- state diagram for 3 Bit Asynchronous Down counter.