CMR INSTITUTE OF TECHNOLOGY

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Internal Assesment Test - III

Sub:	DIGITAL SYSTEM DESIGN (DSD)							Code:	18EE35
Date:	19/11/2019	Duration:	90 mins	Max Marks:	50	Sem:	3rd	Branch:	EEE

Answer Any **FIVE FULL** Questions

		Marks	OBE	
			CO	RBT
1	Draw the logic diagram for the following modes of Shift Register: (a) SISO, (b) SIPO, (c) PISO, (d) PIPO	2.5x4=10	C O3	L2
2	With neat logic diagram explain the operation of Universal shift register with Mode control table.	10	CO3	L2
3	Analyze the operation of Ring Counter (MOD-4 or 4 bit) with logic diagram, truth table, timing diagram and state diagram.	10	CO3	L4
4	Design a synchronous counter with counting sequence 0, 2, 3, 6, 5, 1, 0… using D Flip-flop.	10	CO3	L6
5	Design a Synchronous MOD-6 counter using T flip-flop.	10	CO3	L6
6	Design a MOD-10 (BCD) Asynchronous counter with logic diagram, timing diagram and state diagram.	10	CO3	L6
7	Explain the working of 3-bit Asynchronous down counter configured using JK flip-flop with logic diagram, timing diagram and state diagram.	10	CO3	L2

1) Draw the logic diagram for the following modes of Shift Register: (a) SISO, (b) SIPO, (c) PISO, (d) PIPO.

Ans: Basically shift registers are four types as (I) SISO, (II) SIPO, (III) PISO, (IV) PIPO which are explained below one by one.

(I) SISO (Serial in Serial out Shift Register):- SISO is two types as (a) SISO right shift and (b) SISO left shift registers.

(a) SISO right shift register: This type of shift register accepts data serially i.e. one bit at a time and also outputs data serially by shifting every output data of individual flip-flops (FFs) in right directon. Fig.1 is showing the logic diagram of a 4-bit serial in serial out right shit regiater for storing 4 bit where 4 numbers of FFs are connected together and the output of one flip-flop is connected to the input of next FF. Here we are using D flip-flop using negative edge triggered clock pulse. When serial data is transferred to the second register, each new bit is clocked into the first FF at the negative-edge of each clock pulse. The bit that was previously stored by the first FF is transferred to the second FF. The bit that was stored by the last FF is shifted out.

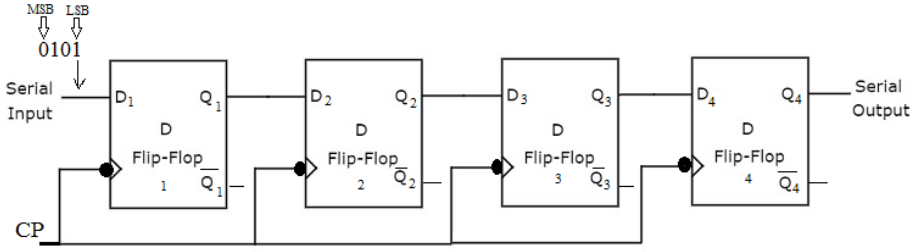


Fig.1. Logic diagram of a 4-bit SISO right shift register

(b) SISO left shift register:This type of shift register accepts data serially i.e. one bit at a time and also outputs data serially by shifting every output data of individual flip-flops (FFs) in left directon. Fig.1 is showing the logic diagram of 4-bit serial in serial out left shift register for storing 4 bit where 4 numbers of flip-flops are connected together and the output of one flip-flop is connected to the input of next flip-flop. Here we are using D fli-flop using negative edge triggered clock pulse.

When serial data is transferred to the second register, each new bit is clocked into the first FF at the negative-edge of each clock pulse. The bit that was previously stored by the first FF is transferred to the second FF. The bit that was stored by the last FF is shifted out.

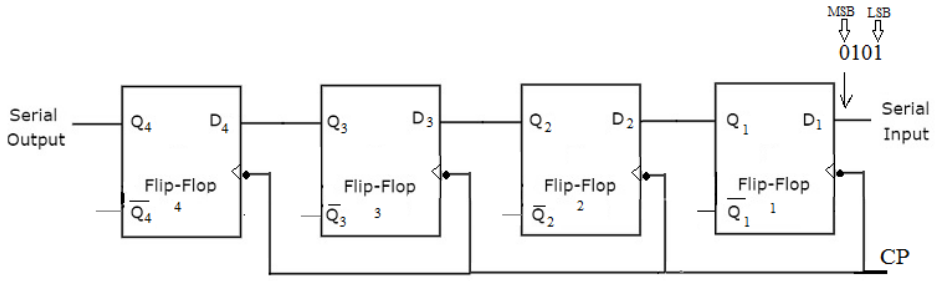


Fig.2. Logic diagram 4-bit SISO left shift register

(II) Serial in Parallel out shift Register (SIPO): This type of shift register accepts data serially i.e. one bit at a time and outputs data parallely. Fig.1 is showing the logic diagram of 4-bit serial in parallel out shift register for storing 4 bit data. This circuit consists of four D flip-flops, which are cascaded. That means, output of one D flip-flop is connected as the input of next D flip-flop. All these flip-flops are synchronous with each other since, the same clock signal is applied to each one. Here we are using D flip-flop by considering negative edge triggered clock pulse.

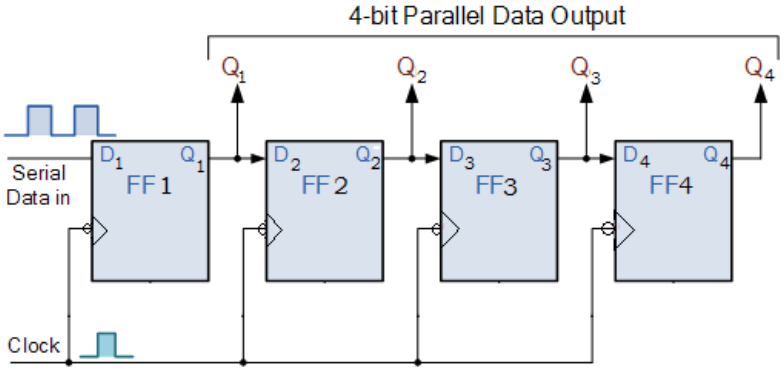


Fig.3. Logic diagram 4-bit SIPO shift register

(III) PISO Parallel in Serial out shift Register (PISO): This type of shift register accepts data parallely and outputs data serially. Fig.1 is showing the logic diagram of 4-bit parallel in serial out shift register for storing 4 bit data where 4 numbers of flip-flops are connected together by a common clock pulse. The output of one flip-flop is connected to the input of next flip-flop by using some combinational logic circuit. Here we are using D flip-flop using negative edge triggered clock pulse.

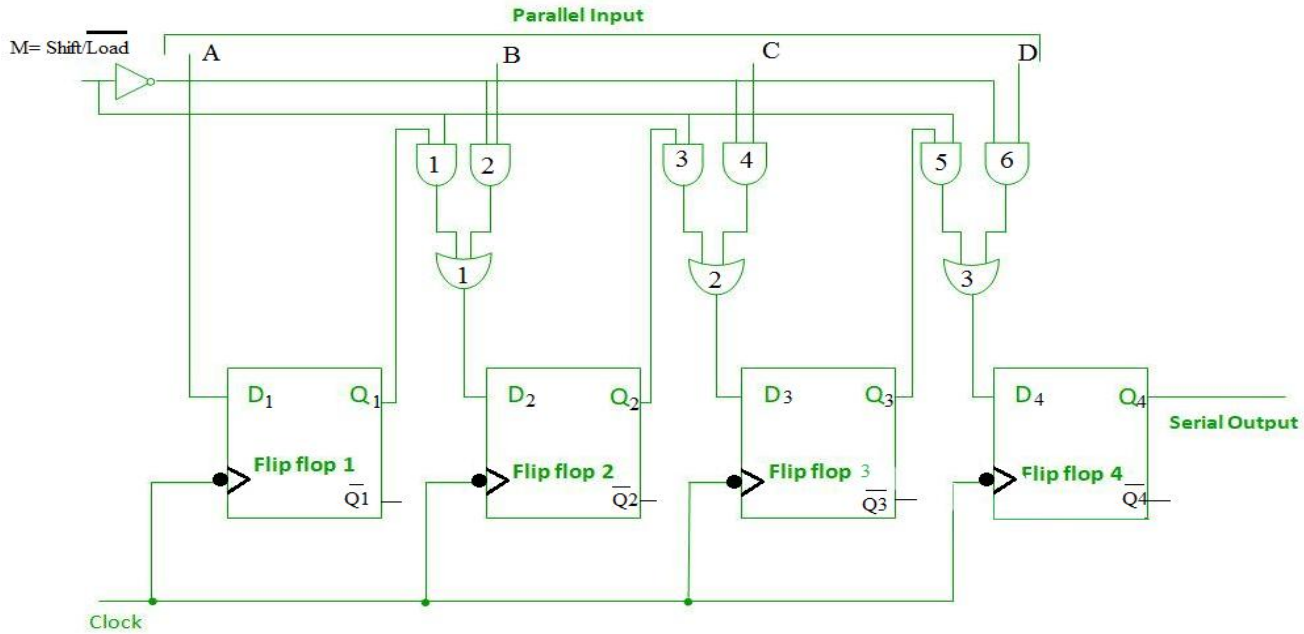


Fig.4. Logic diagram 4-bit PISO shift register

Two modes of operations are done in this logic diagram circuit as (a) Loading Mode, (b) Shifting Mode.

(a) **Loading Mode:** When M=0, then Load mode is activated.Then points a, b, c are 1 (activated) and d, e, f are 0 (deactivated). So AND gates 1, 3, 5 will give zero output and AND gates 2, 4, 6 will give B, C, D respectively. So, outputs of OR gates 1, 2, 3 will be respectively B, C, D. So ultimately each flip-flop is loading and storing input data.
(b) **Shifting Mode:** When M=1, then shift mode is activated.Then points a, b, c are 0 (deactivated) and d, e, f are 1 (activated). So AND gates 1, 3, 5 will give Q1, Q2, Q3 outputs respectively and AND gates 2, 4, 6 will give zero. So, outputs of OR gates 1, 2, 3 will be respectively Q_1, Q_2, Q_3. So ultimately each flip-flop is shifting input data. Let us consider, Din=1011, so when M=0, then four flip-flops will store 1011 as input data is parallely loaded ABCD=$D_1D_2D_3D_4$=1011. And when M=1, then data are shifted right from one flip-flop to next flip-flop.

(IV) Parallel in Parallel out shift Register (PIPO): This type of shift register accepts data parallely and outputs data parallely. Fig.1 is showing the logic diagram of 4-bit parallel in parallel out shift register for storing 4 bit data where 4 numbers of flip-flops are connected together by using a common clock input pulse. Here we are using D fli-flop.

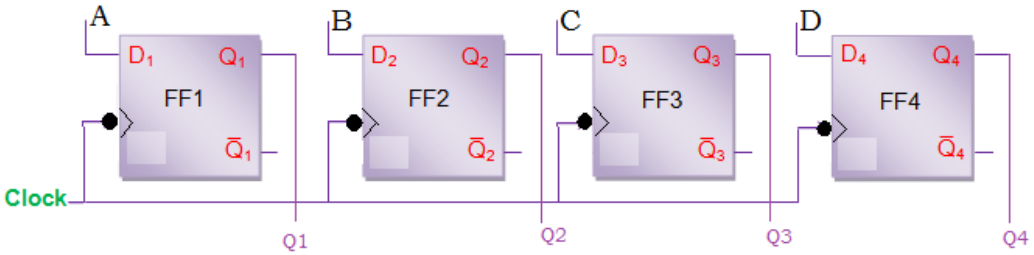


Fig.5. Logic diagram 4-bit PIPO shift register

2. With neat logic diagram explain the operation of Universal shift register with Mode control table.

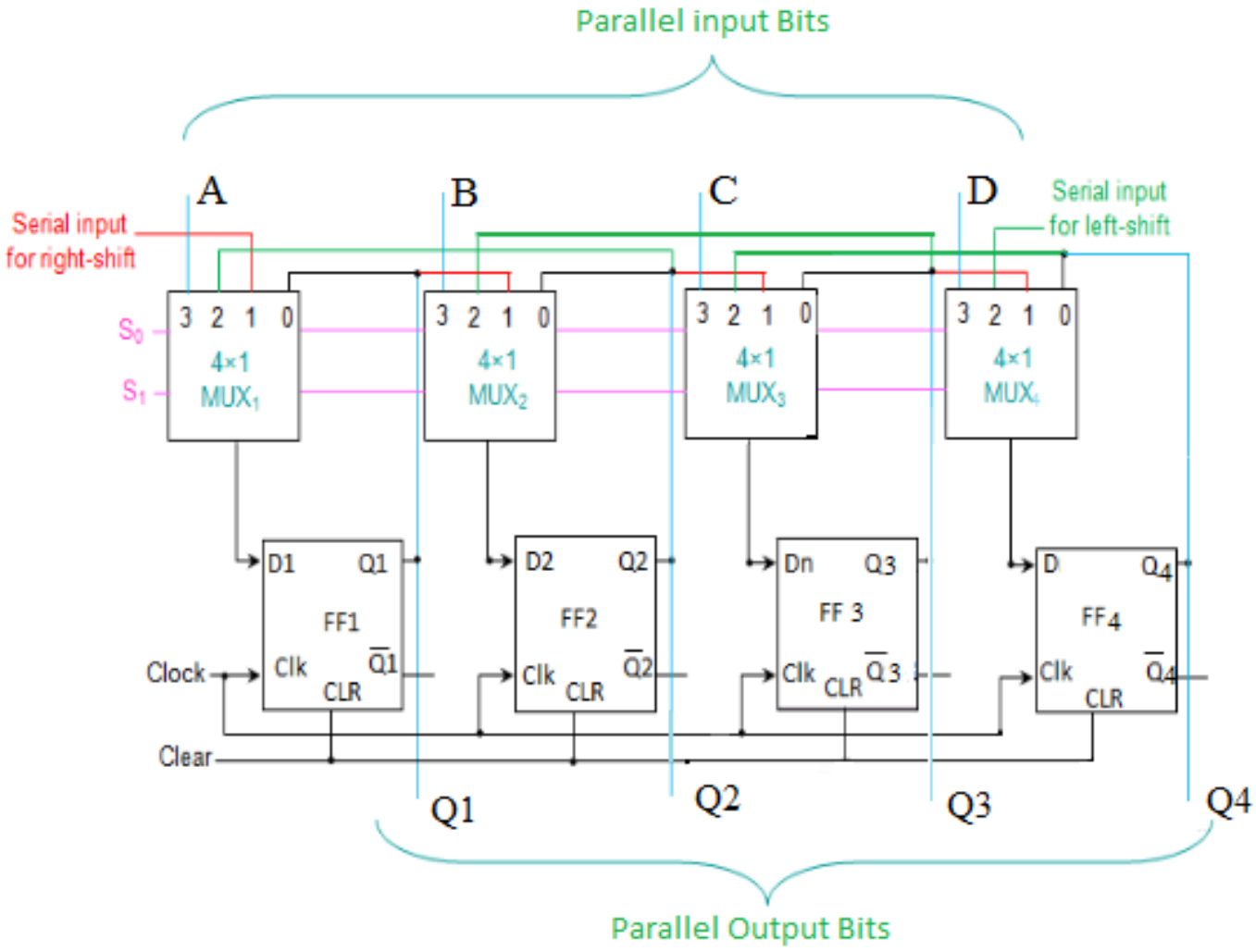


Fig. 4-bit Universal ShifftRegister

A universal shift register is a register which has both the right shift and left shift with parallel load capabilities. It is used as memory elements in computers. A unidirectional shift register is capable of shifting in one direction. A bidirectional shift register is capable of shifting in both the directions. The universal shift register is a combination design of unidirectional (either right or left side of data bits as in case of SISO, SIPO, PISO, PIPO) and bidirectional shift register along with parallel load and provision of reference to as universal shift register. Such a shift register

Capable of storing input bits. Fig. is showing the logic diagram of 4-bit universal register. The working of the universal shift register depends on the inputs given to the select lines. The register operations performed for the various inputs of select lines are as given in table.

Mode Control		Register Operation
S_1	S_0	
0	0	No Change
0	1	Shift Right
1	0	Shift Left
1	1	Parallel Load

When S_1S_0=00, input 0 is selected and the present value of the register is applied to the D inputs of the flip-flops. This results "no change" in register value.

When S_1S_0=01, input 1 is selected and the connections are such that it operates as a "Right Shift Register".

When S_1S_0=10, input 2 is selected and the connections are such that it operates as a "Left Shift Register".

When S_1S_0=11, the binary information on the parallel input lines is transferred into the register simultaneously and it is "Parallel Load" operation.

Q3. Analyze the operation of Ring Counter (MOD-4 or 4 bit) with logic diagram, truth table, timing diagram and state diagram.

Ans.

Fig. 5.4.1 shows the logic diagram for four-bit ring counter. As shown in the Fig. 5.4.1, the Q output of each stage is connected to the D input of the next stage and the output of last stage is fed back to the input of first stage. The $\overline{CLR}$ followed by $\overline{PRE}$ makes the output of first stage to '1' and remaining outputs are zero, i.e. Q_A is one and Q_B, Q_C, Q_D are zero.

The first clock pulse produces Q_B = 1 and remaining outputs are zero. According to the clock pulses applied at the clock input CP, a sequence of four states is produced. These states are listed in Table 5.4.1.

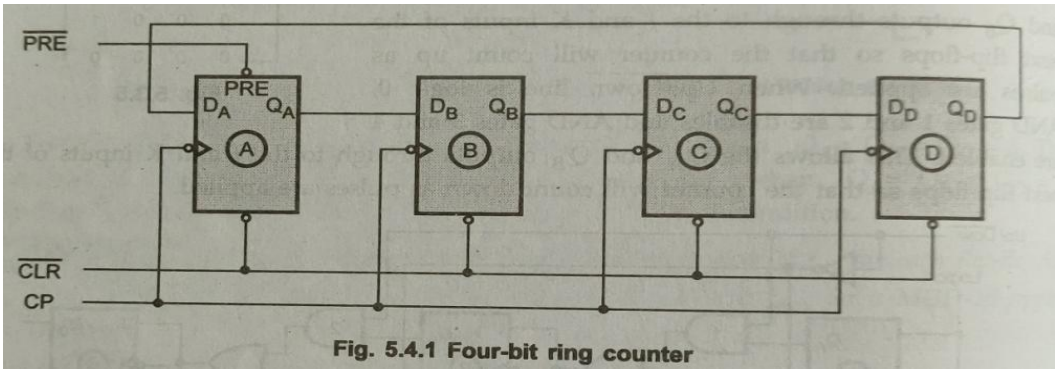
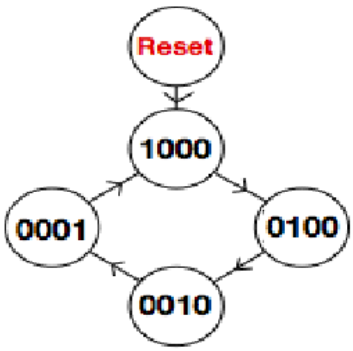


Fig. 5.4.1 Four-bit ring counter



As shown in Table 5.4.1, 1 is always retained in the counter and simply shifted 'around the ring', advancing one stage for each clock pulse. In this case four stages of flip-flops are used. So a sequence of four states is produced and repeated. Fig. 5.4.2 gives the timing sequence for a four-bit ring counter.

Clock pulse	Q_A	Q_B	Q_C	Q_D
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1
4	1	0	0	0

Table 5.4.1 Ring counter sequence 4-bits

The ring counter can be used for counting the number of pulses. The number of pulses counted is read by noting which flip-flop is in state 1. No decoding circuitry is required. Since there is one pulse at the output for each of the N clock pulses, this circuit is also referred to as a divide-by-N-counter or an N : 1 scalar. Ring counters can be instructed for any desired MOD number, that is MOD-N ring counter requires N flip-flops.

4) Design a synchronous counter with counting sequence 0, 2, 3, 6, 5, 1, 0… using D Flip-flop.
Ans.

Solution : N = 6 ∴ 3 flip-flops are required.

Transition table

Present state			Next state		
A	B	C	A+	B+	C+
0	0	0	0	1	0
0	0	1	0	0	0
0	1	0	0	1	1
0	1	1	1	1	0
1	0	0	0	0	0
1	0	1	0	0	1
1	1	0	1	0	1
1	1	1	0	0	0

Note : It is assumed that the next state for unused states 4 and 7 is zero.

K-map simiplifcation

For D_A

A \ BC	00	01	11	10
0	0	0	(1)	0
1	0	0	0	(1)

$D_A = \bar{A}BC + AB\bar{C}$

For D_B

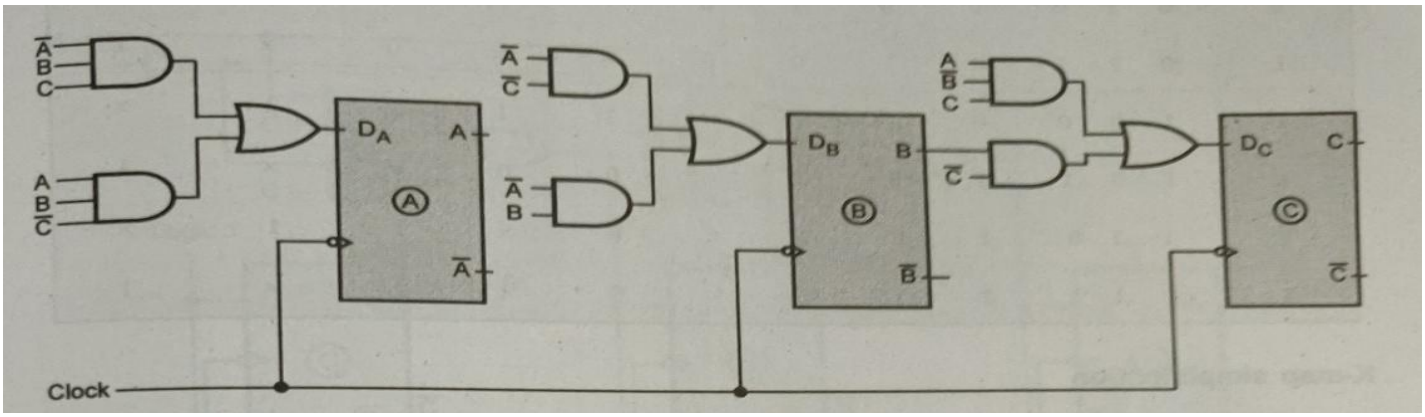
A \ BC	00	01	11	10
0	(1)	0	(1)	(1)
1	0	0	0	0

$D_B = \bar{A}\bar{C} + \bar{A}B$

For D_C

A \ BC	00	01	11	10
0	0	0	0	(1)
1	0	(1)	0	(1)

$D_C = A\bar{B}C + B\bar{C}$



5) Design a Synchronous MOD-6 counter using T flip-flop.

Ans.

Design of a Synchronous Mod-6 Counter using Clocked T Flip-Flops

For designing of counter using clocked T flip-flop we have to follow a similar procedure as that for the design using clocked JK flip-flop.

Step 1 : Find number of flip-flops required to build the counter.

Flip-flops required are : $2^n \geq N$

Here $N = 6 \quad \therefore \quad n = 3$

i.e. three flip flops are required.

Step 2 : Write an excitation table for T flip-flop.

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Table

Step 3 : Determine the transition table.

Present state			Next state			Flip-flop inputs		
Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	T_A	T_B	T_C
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	0	0	0	1	0	1
1	1	0	x	x	x	x	x	x
1	1	1	x	x	x	x	x	x

Step 4 : K-map simplification for flip-flop inputs.

For T_A

Q_A \ Q_BQ_C	00	01	11	10
0	0	0	1	0
1	0	1	X	X

$T_A = Q_AQ_C + Q_BQ_C$

For T_B

Q_A \ Q_BQ_C	00	01	11	10
0	0	1	1	0
1	0	0	X	X

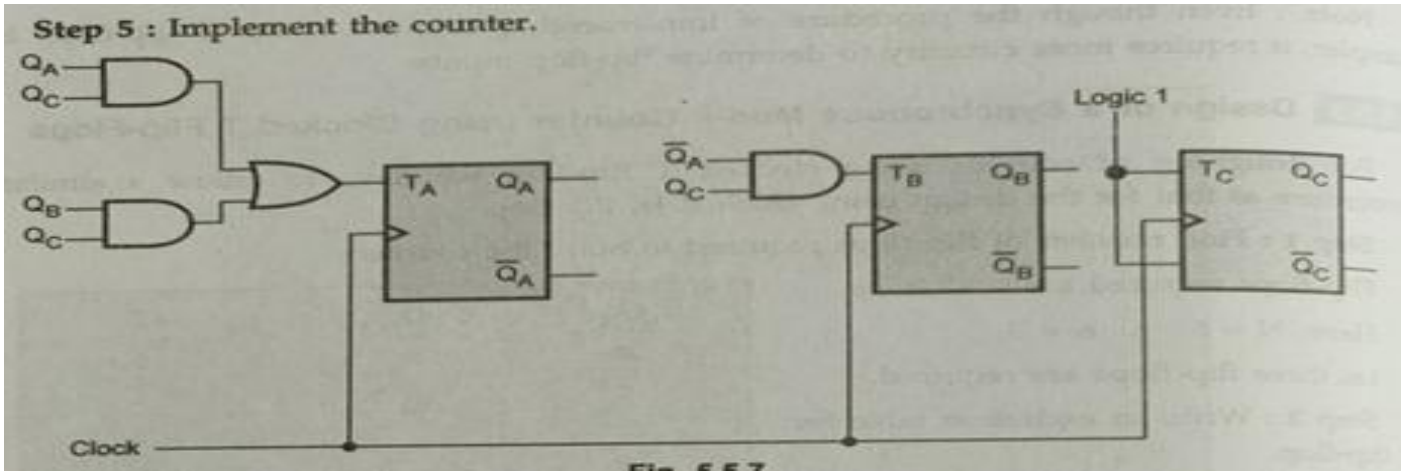
$T_B = \overline{Q}_AQ_C$

For T_C

Q_A \ Q_BQ_C	00	01	11	10
0	1	1	1	1
1	1	1	X	X

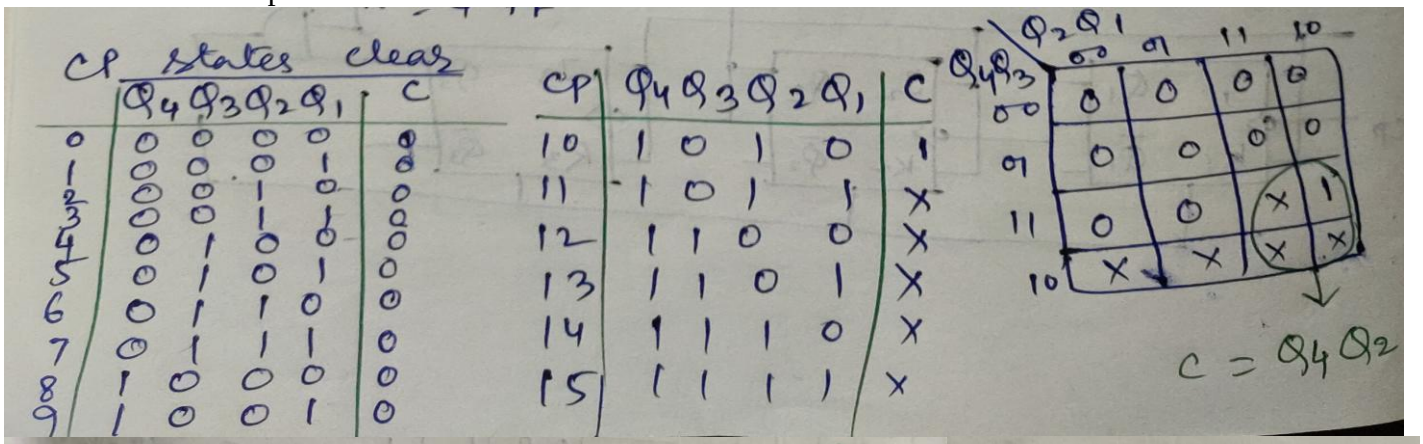
$T_C = 1$

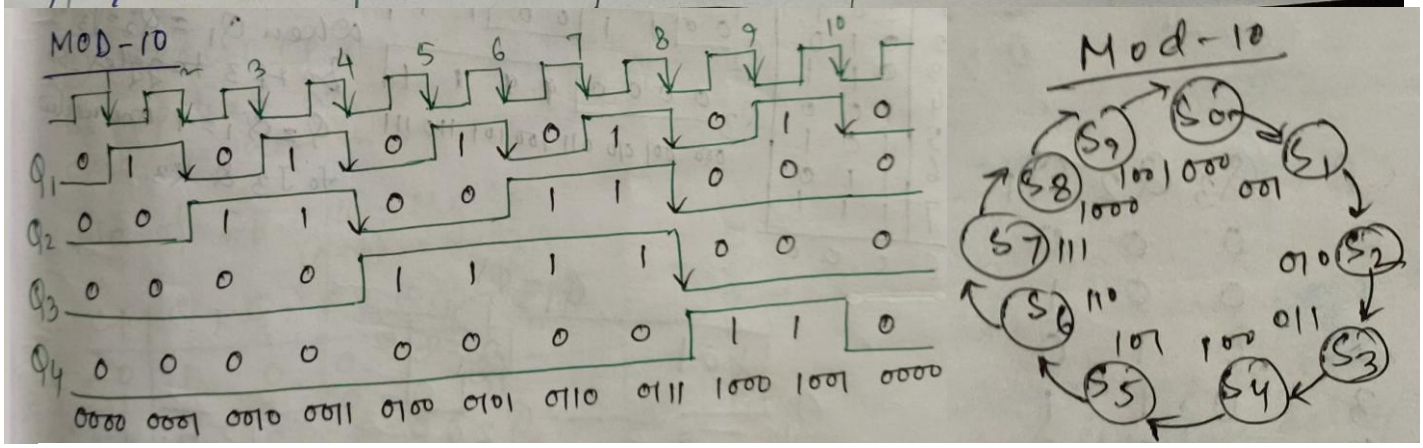
Fig.

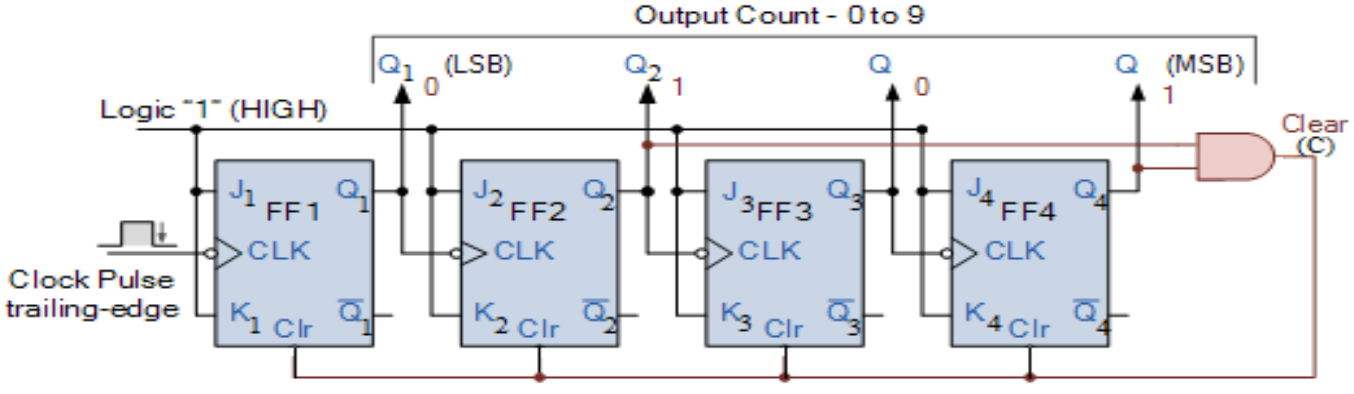


6) Design a MOD-10 (BCD) Asynchronous counter with logic diagram, timing diagram and state diagram.
Ans.

- No. of valid states: 10 (0-9). At 10th clock pulse output will be temporarily 1010 but immediately every flip-flops will be cleared to zero and clear input will be activated (1). 11^{th}-15^{th}states will be invalid.
- No. of flip-flops: 2^n>=N,
  - if n=4, then the condition, 16>=10 (N=10) will be valid.
- No. of sequence states total: 16 (0-15).
- No. of clock pulse: 16.







7) Explain the working of 3-bit Asynchronous down counter configured using JK flip-flop with logic diagram, timing diagram and state diagram.

Ans. Asynchronous down counter will count downward from maximum count to zero.

No. of bit → 3.
No. of sequence states → 2^3 → 8 → (0 - 7) / (1 - 8).
No. of ffs → 3.
No. of clock pulses → 8.

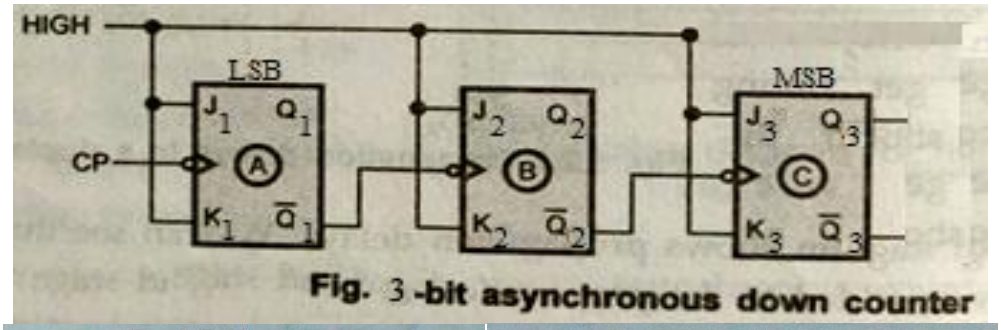


Fig. 3-bit asynchronous down counter

Truth Table

CP	Q_3	Q_2	Q_1
0	1	1	1
1	1	1	0
2	1	0	1
3	1	0	0
4	0	1	1
5	1	0	1
6	1	1	0
7	0	0	1
8	0	0	0

Decreasing (Down Counter)

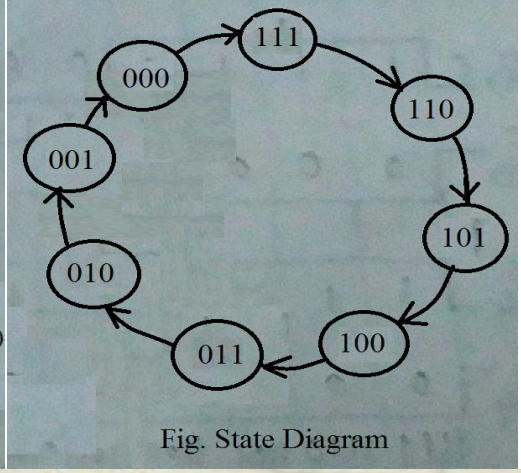


Fig. State Diagram