Modified

CBCS SCHEME

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18EE34

Third Semester B.E. Degree Examination, Dec.2019/Jan.2020
Analog Electronics Circuits

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Draw a double ended clipper circuit and explain the working principle with transfer characteristics. **(10 Marks)**

b. Draw and explain the working of clamper circuit which clamps the positive peak of a signal to zero. **(10 Marks)**

OR

2 a. Derive the expression for stability factors S′ and S″ for fixed bias circuit. **(08 Marks)**

b. A voltage divider biased circuit has $R_1 = 39K\Omega$, $R_2 = 82K\Omega$, $R_C = 3.3K\Omega$, $R_E = 1K\Omega$ and $V_{CC} = 18V$. The silicon transistor used has $\beta = 120$. Find Q-point and stability factor. **(07 Marks)**

c. Explain the operation of transistor as switch with suitable circuit and necessary waveforms. **(05 Marks)**

Module-2

3 a. State and prove Millers theorem. **(06 Marks)**

b. Compare the characteristics of CB, CE and CC configurations. **(06 Marks)**

c. For the collector feedback configuration having $R_F = 180K\Omega$, $R_C = 2.7K\Omega$, $C_1 = 10\mu F$, $C_2 = 10\mu F$, $\beta = 200$, $r_0 = \infty\Omega$ and $V_{CC} = 9$volts. Determine the following parameters:
i) re ii) z_i iii) z_o iv) A_v **(08 Marks)**

OR

4 a. Derive suitable expression to explain the effect of cascading of amplifiers on lower and upper cut off frequencies. **(08 Marks)**

b. Derive equations for miller input capacitance and miller output capacitance. **(08 Marks)**

c. A transistor in CE mode has h-parameters $h_{ie} = 1.1K\Omega$, $h_{re} = 2 \times 10^{-4}$, $h_{fe} = 100$ and $h_{oe} = 25\mu A/V$. Determine the equivalent CB parameters. **(04 Marks)**

Module-3

5 a. Derive expression for Zi and Ai for a Darlington Emitter follower circuit. **(10 Marks)**

b. Explain the need of a cascading amplifier. Draw and explain the block diagram of two stage cascade amplifier. **(06 Marks)**

c. Write a note on cascade amplifier. **(04 Marks)**

OR

6 a. List the general characteristics of negative feedback amplifier. **(04 Marks)**

b. A given amplifier arrangement has the following voltage gain $AV_1 = 10$, $AV_2 = 20$ and $AV_3 = 40$. Calculate the overall voltage gain and determine the total voltage gain in dBS. **(08 Marks)**

c. For the voltage series feedback amplifier. Derive an expression for output impedance (Resistance). **(08 Marks)**

Module-4

7 a. Show that maximum efficiency of class-B push pull amplifier (power amplifier) circuit is 78.54%. **(08 Marks)**

b. Explain the classification of power amplifier with a neat circuit diagram and waveforms. **(07 Marks)**

c. A class-B push pull amplifier operating with $V_{CC} = 25V$ provides a 22V peak signal to 8Ω load. Calculate the circuit efficiency and power dissipated per transistor. **(05 Marks)**

OR

8 a. Draw the circuit of wein bridge oscillator and explain its operation. **(10 Marks)**

b. With a neat circuit diagram and waveform, explain the working principal of crystal oscillator operating in series resonant mode. A crystal has the following parameters L = 0.334H, C = 0.065pF and R = 5.5KΩ. Calculate its resonant frequency. **(10 Marks)**

Module-5

9 a. With the help of neat diagram, explain the working and characteristics of N-channel JFET. **(10 Marks)**

b. For a self bias JFET circuit, $V_{DD} = +12V$, $R_D = 2.2K\Omega$, $R_G = 1M\Omega$, $R_S = 1K\Omega$, $I_{DSS} = 8mA$, $V_P = -4$ Volts. Determine the following parameters: i)V_{GS} ii) I_D iii) V_{DS} iv) V_S v) V_G vi) V_D **(10 Marks)**

OR

10 a. With neat sketches, explain the operation and characteristics of n-channel depletion type MOSFET. **(10 Marks)**

b. Derive expression for V_{GS}, I_D, V_{DS}, V_D and V_S for a voltage divider bias circuit using FET. **(10 Marks)**

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Modification in Scheme and Solution

1 message

Dr. A.Manjunath <manjuprinci@gmail.com>
To: pmanjunath p <pmanjunathvtu@gmail.com>

Thu, Jan 9, 2020 at 10:21 AM

Good morning
The modification of scheme and solution in subject Analog Electronics circuits 18EE34 are

3.c.

r_e=11.21ohms-----1marks

I_B=11.53Microamps-----2marks

I_E=2.32milli amps-------1marks

A_V=-227.2----------2marks

A_i=-47.53----------2marks

5.c. Award Marks for cascade amplifier

9. b. Full Marks may be awarded if student have solved the problem considering fixed bias circuit

10.b. Full Marks may be awarded if student have derived the expression for fixed bias circuit

Dr.A.Manjunatha

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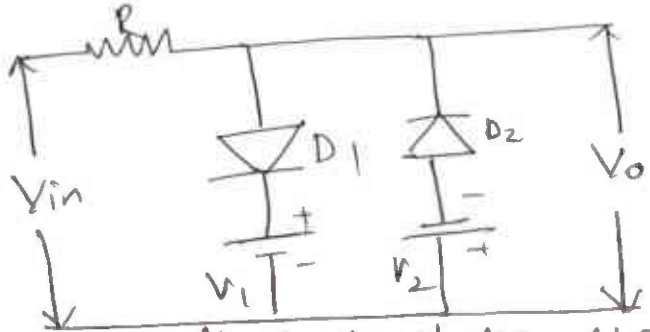
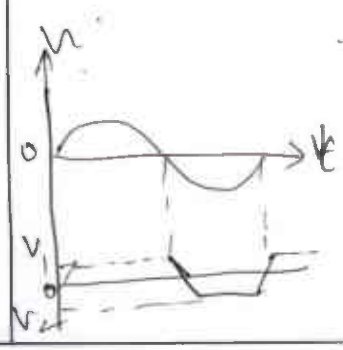
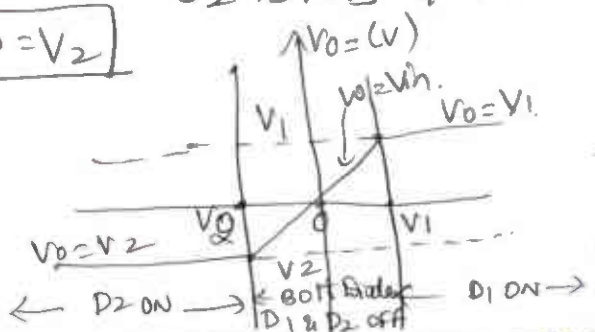
Signature of Scrutinizer

Scheme & Solution

Subject Title : Analog Electronics Circuits **Subject Code :** 18EE34

Question Number	Solution	Marks Allocated
(1) a.	Module-01 The ckt shown is a double ended clipper which is used to clipp both (+ve) and (-ve) half cycle of the i/p among that the i/p is pure sinusoidal. $V_{in} = V_m \sin \omega t$ The diodes D_1 & D_2 are ideal diodes	(10 Marks)
		— (5M)
	During the half cycle of the i/p Case 1 : when $V_{in} < V_1$, both diodes are R.B $\therefore \boxed{V_o = V_i}$	— (2M)
	Case 2 when $V_{in} > V_1$, D_1 becomes F.B & is ON, Conducts & D_2 is R.B, is OFF. $\therefore \boxed{V_o = V_1}$	
	During -ve half cycle Case 1 : when $V_{in} > V_2$, both diodes are RB $\therefore \boxed{V_o = V_i}$	— (2M)
	Case 2 : when $V_{in} < V_2$, D_1 is R.B & is OFF D_2 is F.B & ON $\therefore \boxed{V_o = V_2}$	
	 	— (1M)

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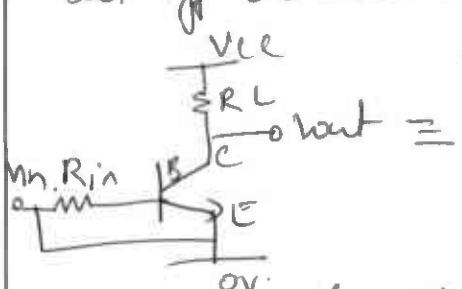
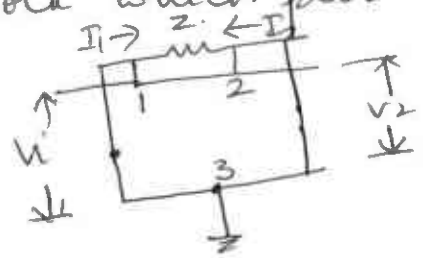
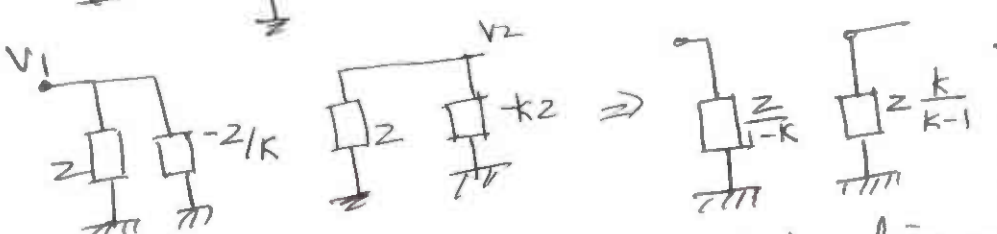
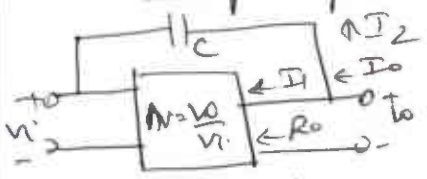
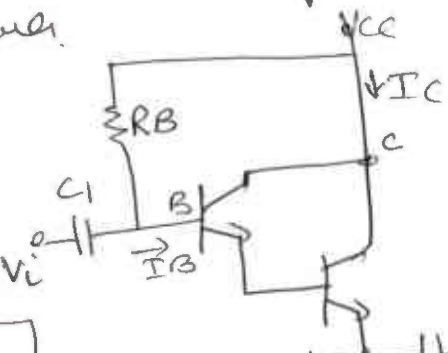
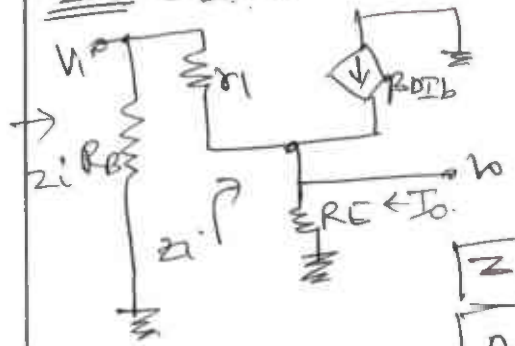
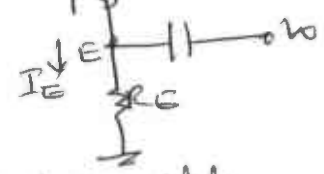
Subject Title : Analog Electronics circuits Subject Code : 18EE34

Question Number	Solution	Marks Allocated
b.	The circuit which clamps the positive peak of a signal to as zero level is called as negative clamper. It consists of Capacitor diode & resistor	10 Marks
	During +ve half cycle D is forward biased so max V_m $\therefore$ $V_{in} = V_m$, $V_o = 0$ $V_{in} = -V_m$, $V_o = 2V_m$ — (3M) $V_o = V_{in} - V_m$	(4M) 3M
	During -ve half cycle → The diode is reverse biased & starts discharging to a time constant $T = R_L C$	(3M)
	(OR)	
2(a)	Fixed bias Apply KVL to base & collector ckt $V_{BE} = V_{CC} - I_B R_B$ →(1) $V_{CE} = V_{CC} - I_C R_C$	(08 Marks) (02M)
	$S' = -\frac{\beta}{R_B}$ — (3M)	$S'' = \frac{dI_C}{d\beta} = \frac{I_C}{\beta}$ — (3M)
(b)	$R_{TH} = R_1 \| R_2 = 6.775\,k\Omega$, $I_{CQ} = 2.28mA$ = βI_B $V_T = \frac{R_2 V_{CC}}{R_1 + R} = 3.127V$ $V_{CE} = 8.196V$ $I_B = V_T - V_{BE} / R_{TH} + (1+\beta) R_E = 19\mu A$ $\therefore S = 1+\beta / 1+\beta\left[\frac{R_E}{R_C + R_B}\right] = 9.372$	7 marks Each (2M) (1M) (1M) (1M)

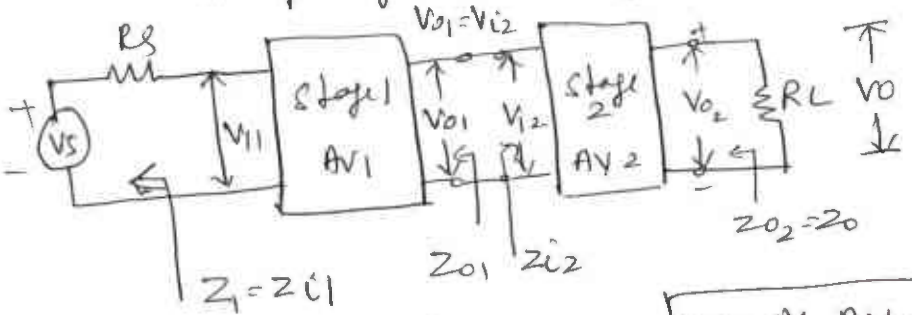
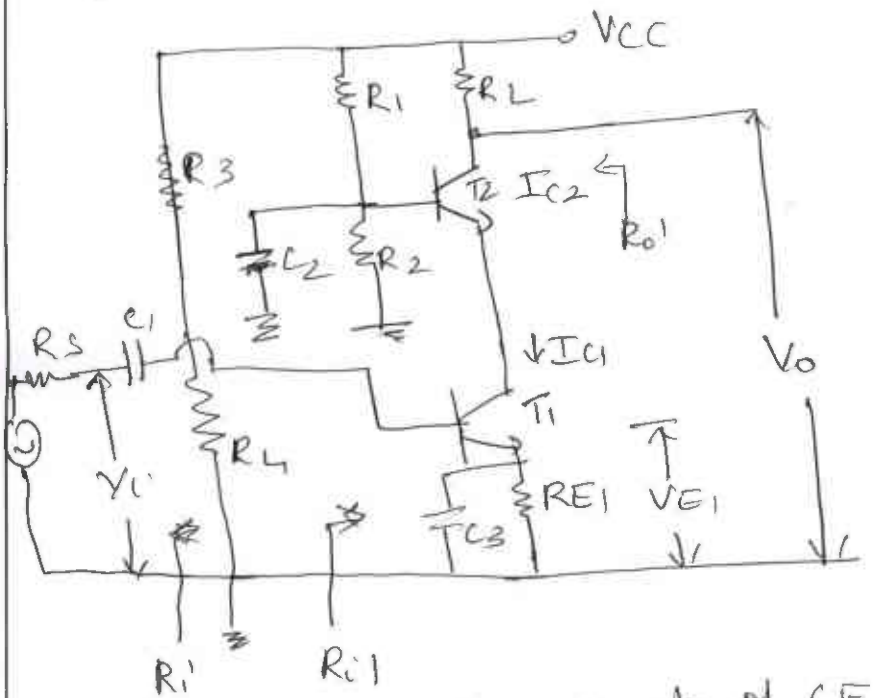
Subject Title : Analog Electronic Circuits Subject Code : 18EE34

Question Number	Solution	Marks Allocated
c.	Cut-off characteristics  (3M) (1) o/p Base are 0V (2) $V_{BE} < 0.7V$ (3) B.E is R.B (4) B.C is R.B (5) Transistor is OFF (6) $I_C = 0$ (7) $V_{out} = V_{CE} = V_{CC} = 1$	5 Mark 2M
	Module-02	
(3) a.	Statement :- when an impedance Z is connected between the i/p (1) & o/p (2) terminals of a network which provides a voltage gain A_V.	(6 Mark) (3M)
	 $Z_1 = \frac{Z}{1-A_V}$, $Z_2 = \frac{ZA_V}{A_V - 1}$	
	 	(3M)
b	Comparision of CB, CE & CC Configuration	(6 Marks) Each (01M)
c.	(i) $r_e = \frac{26mV}{2.32mA} = \boxed{11.21\,\Omega}$ (→2M), $I_B = (\beta+1) I_B = 2.32mA$	(8M)
	(iii) $\boxed{Z_0 = R_F = 180K}$ (→2M)	
	(iv) $A_V = \frac{V_0}{V_i} = \boxed{-227.2}$ (→2M)	
	$\boxed{A_i = -47.53}$ (→2M) $\quad \therefore R_0 \| R_F = 45K$	
	(OR)	
(4) a.	Cascading of amplifier	8 Marks
	(i) Lower cut-off frequency $f_{L(n)} = \frac{f_L}{\sqrt{2^{1/n}-1}}$	(4M)
	(ii) Higher cut-off frequency $f_{H(n)} = f_H \sqrt{2^{1/n}-1}$	(4M)

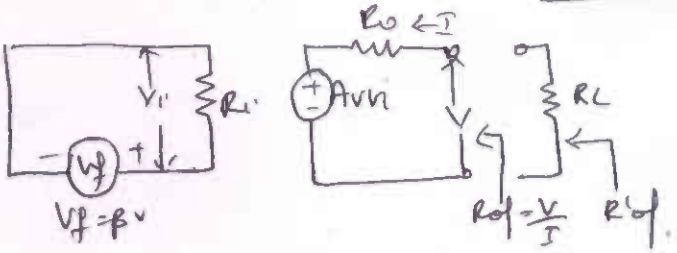
Subject Title : Analog Electronic Circuits Subject Code : 18EE34.

Question Number	Solution	Marks Allocated
b.	Miller i/p capacitance  $C_M = (1 - A_V)C$ — (4M)	(8 Marks)
	Miller o/p capacitance $I_o = I_1 + I_2$ $I_1 = \frac{V_o}{R_o}$; $I_2 = \frac{V_o - V_i}{X_C}$ $\therefore C_{Mo} = C(1 - 1/A_V)$ — (4M)	
	$\frac{R_o}{V_o} = \frac{X_C}{1 - 1/A_V}$ $X_{CMo} = \frac{X_C}{1 - 1/A_V}$	
c.	$h_{Tb} = h_{ie}/(1+h_{fe}) = 10.89$ — Each (1M)	(6 Marks)
	$h_{rb} = (h_{ie} h_{oe}/(1+h_{fe})) - h_{re} = 2.22 \times 10^{-5}$ — (1M)	
	$h_{fb} = -h_{fe}/(1+h_{fe}) = -0.99$ — (1M)	
	$h_{ob} = h_{oe}/(1+h_{fe}) = 0.24 \times 10^{-6}$ — 1M	
	Module 03	
(5) a.	Expression for Z_i & A_i for Darlington emitter follower.  $\beta_D = \beta_1 \cdot \beta_2$ $\beta_D = \beta^2$ — (5M)	10 Marks
	Z_i (Equivalent) ckt   Darlington ckt	
	$Z_i = r_1 + \beta_D R_E$ // — (5M)	
	$A_i = \frac{\beta_D R_B}{R_B + \beta_D R_E}$ //	

Subject Title : Analog Electronic ckt Subject Code : 18EE34

Question Number	Solution	Marks Allocated
b.	When the amplification from a single stage amplifier is not sufficient for a particular purpose or when the i/p or o/p impedance is not of suitable magnitude for the intended application, two or more amplifier stages may be connected in cascade in the o/p of a given stage is connected.	6 Marks (3M)
		(3M)
	$A_V = \frac{V_{o2}}{V_{i1}} = \frac{V_{o2}}{V_{i2}} \frac{V_{i2}}{V_{i1}}$ $\therefore A_V = A_{V_2} A_{V_2}$	
c.	Cascode Connection	4 marks
		(2M)
	The Cascode Connection Consists of CE amplifier. It gives the high i/p impedance of CE amp as well as the good voltage gain & high frequency performance of CE ckt	(2M)

Subject Title : Analog Electronic circuit Subject Code : 18EE34

Question Number	Solution	Marks Allocated
(6) a	→ Stabilize the gain. → reduced the distortion → Serves negative feedback Increases the o/p resist. → Stabilizes operating point	6 Marks Each (01M)
b.	$A_V = A_{V1} \times A_{V2} \times A_{V3}$ $\boxed{A_V = 8000}$ —(4M) $A_{V1}(dB) = 20\log 10 = 20$ $A_{V2}(dB) = 26$ $A_{V3}(dB) = 32$ $\therefore A_V(dB) = A_{V1} + A_{V2} + A_{V3}$ $\boxed{A_{V(dB)} = 78\,dB}$ —(4M)	(8Marks)
c.	 output Resistance $R_{of} = \frac{R_o}{1+\beta A_V}$ $\boxed{R'_{of} = \frac{R'_o}{1+\beta A_V}}$ $R'_o = \frac{R_o R_L}{R_o + R_L}$ —(4M) $A_V = \frac{A_V R_L}{R_o + R_L}$	8Marks —(4M)
	Module - 04	
(7) a.	class B push pull amplifier ckt.	8Marks —(4M)
	Derivation of maximum efficiency 78.5 %	—(4M)
b.	classification of power amplifier	7marks —(02M)
	with neat graph load line waveform	—(5M)
c.	$I_m = 2.75A$. $P_{dc} = 43.7675$ W.	5 marks Each (01M)
	$I_D = \frac{V_m}{R_L} = 1.7507A$ $P_{ac} = 30.25$ W	
	$\boxed{P_{d/2} = 6.758W}$ $\boxed{\%\eta = 69.11}$ % $\boxed{P_d = 13.517W}$	

Subject Title : Analog Electronic Circuits Subject Code : 18EE34.

Question Number	Solution	Marks Allocated
	(OR)	10 Marks
(8) a.	Wein bridge oscillator Circuit – (5M) Explanation & operation – (5M)	
b.	Crystal oscillator Circuit — (2M) Explanation & operation of crystal. — (4M)	10m
	$f_s = \frac{1}{2\pi\sqrt{LC}} = 1.0795\,MHz$ $\quad Q = \frac{W_s L}{R} = 412.388$ $C_{eq} = 0.06103\,pF$ — (1M) $f_p = \frac{1}{2\pi\sqrt{LC_{eq}}} = 1.114\,MHz$ — (1M)	Each (01) (1M)
	— (1M)	
	Module – 05	
(9) a.	N-channel JFET diagram — (5M) Working & Characteristics of JFET — (5M)	10 Marks
b.	Given $V_{DD} = +12V$, $R_D = 2.2k\Omega$, $R_G = 1M\Omega$, $R_S = 1k\Omega$ $I_{DSS} = 8mA$, $V_P = -4$ volts (1) $I_D = 8mA$ or $2A$ (4) $V_{DS} = 5.6V$ (2) $V_{GSQ} = -2V$ (3) $V_{GS} : V_S = I_D R_S = 2V$ (5) $V_D = 7.6V$.	(10 Marks) Each (02M)
	(OR)	
(10) a.	N-channel depletion type MOSFET diagram — (4M) Explanation & operation — (3M) Characteristics — (3M)	10 Mark
b.	Voltage divider bias of FET. ckt derivation — 5M of $V_{GS} = V_G - I_D R_S$ — (1M) $I_{DQ} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$ — (1M) $V_{DSQ} = V_{DD} - I_D(R_D + R_S)$ — (1M) $V_G = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD}$ — (1M) $V_{DS} = V_{DD} - I_D(R_D + R_S)$ — (1M)	(Each 01M)

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