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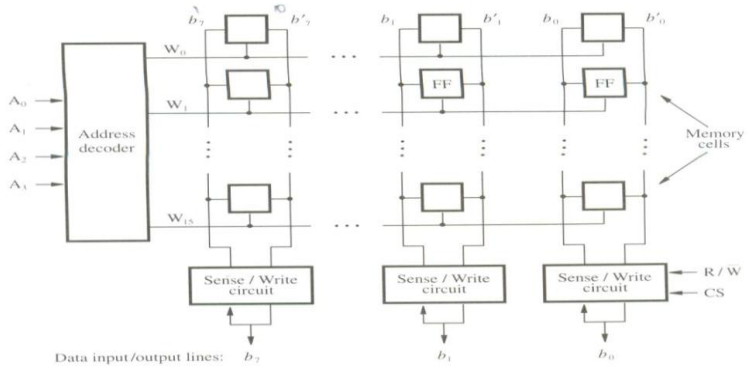
Internal Assesment Solution- for IAT III

Sub:	Computer Organization and Architecture							Code:	18EC35
Date:	15/10/ 2019	Duration:	90 mins	Max Marks:	50	Sem:	3rd	Branch:	ECE
Answer Any FIVE FULL Questions									

1. With the help of necessary diagrams explain the internal organization of a 16*8 bit RAM chip.
2. Memory cells are usually organized in the form of array, in which each cell is capable of storing one bit of in formation.
3. Each row of cells constitute a memory word and all cells of a row are connected to a common line called as **word line**.
4. The cells in each column are connected to Sense / Write circuit by two bit lines. The Sense / Write circuits are connected to data input or output lines of the chip. During a write operation, the sense / write circuit receive input information and store it in the cells of the selected word.



2. Compare static and dynamic RAM with reference to Cell structure, performace and properties. Include necessary diagrams

Static RAM

Two inverters are cross connected to form a batch

The batch is connected to two bit lines by transistors T_1 and T_2.

These transistors act as switches that can be opened / closed under the control of the word line.

- When the wordline is at ground level, the transistors are turned off and the latch retain its state.

Read Operation:

In order to read the state of the SRAM cell, the word line is activated to close switches T_1 and T_2.

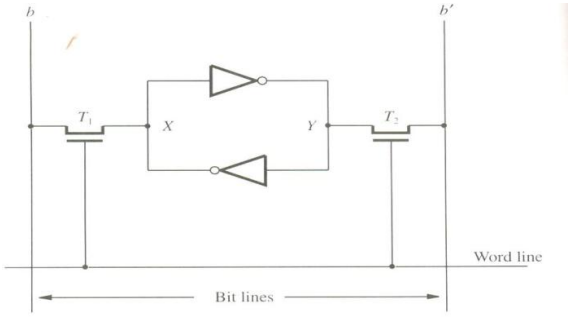
- If the cell is in state 1, the signal on bit line b is high and the signal on the bit line b is low.Thus b and b are complement of each other.
- Sense / write circuit at the end of the bit line monitors the state of b and b‟ and set the output accordingly.

Write Operation:

- The state of the cell is set by placing the appropriate value on bit line b and its complement on b and then activating the word line. This forces the cell into the corresponding state.
- The required signal on the bit lines are generated by Sense / Write circuit.

Asynchronous DRAMS:-

- Less expensive RAM‟s can be implemented if simplex calls are used such cells cannot retain their state indefinitely. Hence they are called **Dynamic RAM's (DRAM).**
- The information stored in a dynamic memory cell in the form of a charge on a capacitor and this charge can be maintained only for tens of Milliseconds. The contents must be periodically refreshed by restoring by restoring this capacitor charge to its full value.



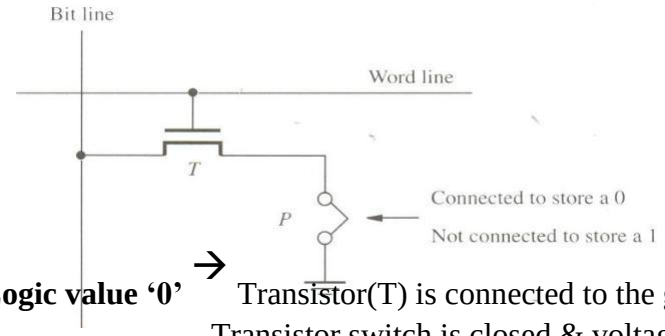
- In order to store information in the cell, the transistor T is turned „on‟ & the appropriate voltage is applied to the bit line, which charges the capacitor.
- After the transistor is turned off, the capacitor begins to discharge which is caused by the capacitor‟s own leakage resistance.
- Hence the information stored in the cell can be retrieved correctly before the threshold value of the capacitor drops down.
  During a read operation, the transistor is turned „on‟ & a sense amplifier connected to the bit line detects whether the charge on the capacitor is above the threshold value.

  If charge on capacitor > threshold value -> Bit line will have logic value „1‟.
  If charge on capacitor < threshold value -> Bit line will set to logic value „0‟.

3)Write notes on i)ROM,ii)PROM, iii)EPROM, iv) EEPROM, v)Flash memory

READ ONLY MEMORY:

- Both SRAM and DRAM chips are volatile,which means that they lose the stored information if power is turned off.
- Many application requires Non-volatile memory (which retain the stored information if power is turned off).
- Eg:Operating System software has to be loaded from disk to memory which requires the program that boots the Operating System ie. It requires non-volatile memory.
- Non-volatile memory is used in embedded system.
- Since the normal operation involves only reading of stored data ,a memory of this type is called ROM.



At Logic value '0' → Transistor(T) is connected to the ground point(P).
Transistor switch is closed & voltage on bitline nearly drops to zero.

At Logic value '1' → Transistor switch is open.
The bitline remains at high voltage.

- To read the state of the cell,the word line is activated.
- A Sense circuit at the end of the bitline generates the proper output value.

Types of ROM:

- Different types of non-volatile memory are,
  - PROM
  - EPROM
  - EEPROM
  - Flash Memory

PROM:-Programmable ROM:

- PROM allows the data to be loaded by the user.
- Programmability is achieved by inserting a „fuse" at point P in a ROM
- cell. Before it is programmed, the memory contains all 0"s
- The user can insert 1"s at the required location by burning out the fuse at these locations using high-current pulse.
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This process is irreversible.

Merit:

- It provides flexibility.
- It is faster.
- It is less expensive because they can be programmed directly by the user.

EPROM:-Erasable reprogrammable ROM:

- EPROM allows the stored data to be erased and new data to be loaded.
  It requires different voltage for erasing ,writing and reading the stored data.

Flash Memory:

- In EEPROM, it is possible to read & write the contents of a single cell.
- In Flash device, it is possible to read the contents of a single cell but it is only possible to write the entire contents of a block.
- Prior to writing,the previous contents of the block are erased.
- Eg.In MP3 player,the flash memory stores the data that represents sound.
- Single flash chips cannot provide sufficient storage capacity for embedded system application.
- There are 2 methods for implementing larger memory modules consisting of number of chips.They are,
  - Flash Cards
  - Flash Drives.

Merits:

- Flash drives have greater density which leads to higher capacity & low cost per bit.
- It requires single power supply voltage & consumes less power in their operation.

Flash Cards:

- One way of constructing larger module is to mount flash chips on a small card.
- Such flash card have standard interface.

Flash Drives:

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- Larger flash memory module can be developed by replacing the hard disk drive.
- The flash drives are designed to fully emulate the hard disk.
- The flash drives are solid state electronic devices that have no movable parts.

Merits:

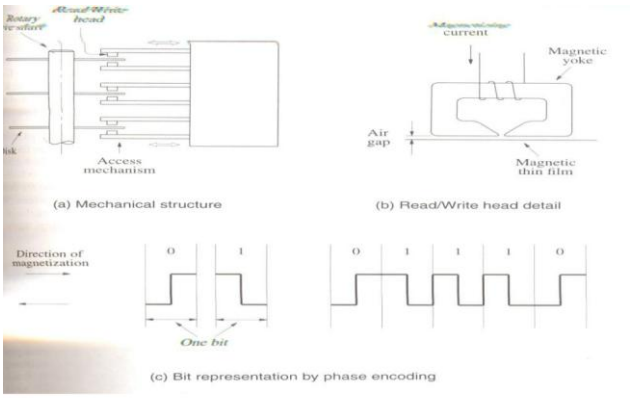
- They have shorter seek and access time which results in faster response.
- They have low power consumption which makes them attractive for battery driven application.
- They are insensitive to vibration.

Demerit:

- The capacity of flash drive (<1GB) is less than hard disk(>1GB).
- It leads to higher cost perbit.
- Flash memory will deteriorate after it has been written a number of times(typically atleast 1 million times.)

Characteristics	**SRAM**	**DRAM**	**Magnetis Disk**
Speed	Very Fast	Slower	Much slower than DRAM
Size	Large	Small	Small
Cost	Expensive	Less Expensive	Low price

4) Explain the mechanical structure of Magnetic Hard disk . Write notes on organising and accessing data on a magnetic disk.



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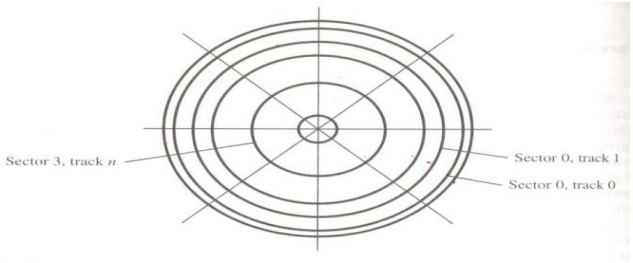
The Read/Write heads must be maintained at a very small distance from the moving disk surfaces in order to achieve high bit densities.

- When the disk are moving at their steady state, the air pressure develops between the disk surfaces & the head & it forces the head away from the surface.
- The flexible spring connection between head and its arm mounting permits the head to fly at the desired distance away from the surface.

Wanchester Technology:

- Read/Write heads are placed in a sealed, air –filtered enclosure called the Wanchester Technology.

In such units, the read/write heads can operate closure to magnetic track surfaces because the dust particles which are a problem in unsealed assemblies are absent.



Merits:

- It have a larger capacity for a given physical size.
- The data intensity is high because the storage medium is not exposed to contaminating elements.
- The read/write heads of a disk system are movable.
- The disk system has 3 parts.They are,
  - **Disk Platter**(Usually called Disk)
  - **Disk Drive(**spins the disk & moves Read/write heads)
  - **Disk Controller**(controls the operation of the system.)

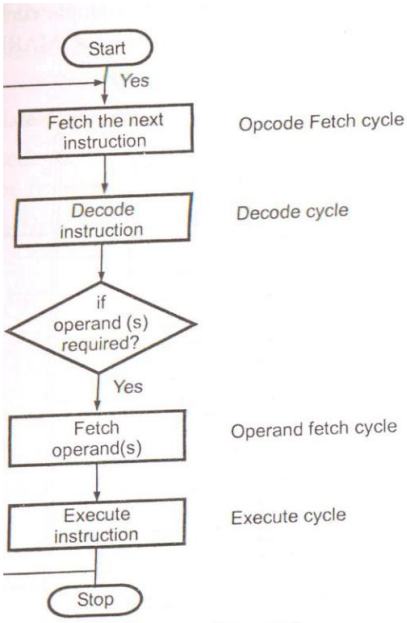
Organizing & Accessing the data on disk

5) With the help of Single bus organisation of data path inside a processor explain the steps followed by the processor to execute an instruction.

The primary function of a processor unit is to execute sequence of instructions stored in a memory, which is external to the processor unit.

- The sequence of operations involved in processing an instruction constitutes an instruction cycle,which can be subdivided into 3 major phases:

1. Fetch cycle
2. Decode cycle
3. Execute cycle

- 

g. 3.1 Basic instruction cycle

To perform fetch, decode and execute cycles the processor unit has to perform set of operations called micro-operations.

- Single bus organization of processor unit shows how the building blocks of processor unit are organised and how they are interconnected.

  They can be organised in a variety of ways, in which the arithmetic and logic unit and all processor registers are connected through a single common bus.
- It also shows the external memory bus connected to memory address(MAR) and data register(MDR).

6) a) Explain Gating signals associated with MDR and MAR.

b) Give Control sequence for the execution of instruction ADD (R2),R1

Let us find the complete control sequence for execution of the instruction Add R_1,(R_2) for the single bus processor.

- This instruction adds the contents of register R_1 and the contents of memory location specified by register R_2 and stores results in the register R_1.
- To execute bus instruction it is necessary to perform following actions:
  1. Fetch the instruction
  2. Fetch the operand from memory location pointed by R_2.
  3. Perform the addition
  4. Store the results in R_1.

The sequence of control steps required to perform these operations for the single bus architecture are as follows;

1.PC_{out}, MAR_{in} Y_{in}, select C, Add, Z_{in}
2. Z_{out}, PC_{in}, MAR_{out} , MAR_{inM}, Read
3. MDR_{out} P,MAR_{in}
4. R_{2out} , MAR_{in}
5. R_{2out} , Y_{in},MAR_{out} , MAR_{inM}, Read
6. MDR_{out} P, select Y, Add, Z_{in}
7. Z_{out}, R_{1in}

(i) Step1, the instruction fetch operation is initiated by loading the controls of the PC into the MAR.

- PC contents are also loaded into register Y and added constant number by activating select C input of multiplexer and add input of the ALU.
- By activating Z_{in} signal result is stored in the register Z

(ii) Step2 , the contents of register Z are transferred to pc register by activating Z_{out} and pc_{in} signal.

- This completes the PC increment operation and PC will now point to next instruction,
- In the same step (step2), MARout , MDR $_{inM}$ and Read signals are activated.
- Due to MARout signal , memory gets the address and after receiving read signal and activation of MDR in M Signal ,it loads the contents of specified location into MDR register.

(iii) Step 3 contents of MDR register are transferred to the instruction register(IR) of the processor.

- The step 1 through 3 constitute the instruction fetch phase.
- At the beginning of step 4, the instruction decoder interprets the contents of the IR.
- This enables the control circuitry to activate the control signals for steps 4 through 7, which constitute the execution phase.

(iv) Step 4, the contents of register R_2 are transferred to register MAR by activating R_{2out} and MAR in signals.

(v) Step 5, the contents of register R_1 are transferred to register Y by activating R_{1out} and Y_{in} signals. In the same step, MAR_{out}, MDR_{inM} and Read signals are activated.

- Due to MAR_{out} signal, memory gets the address and after receiving read signal and activation of MDR_{inM} signal it loads the contents of specified location into MDR register.

(vi) Step 6 MDR_{outP}, select Y, Add and Z_{in} signals are activated to perform addition of contents of register Y and the contents of MDR. The result is stored in the register Z.

(vii) Step 7, the contents of register Z are transferred to register R_1 by activating Z_{out} and R_{1in} signals.

7) With a block diagram, describe the three bus organization of the datapath inside a processor. Give the control sequence forexecution of the instruction ADD R3,R2.R1

1. PC_{out}, MAR_{in}
2. MAR_{out}, MDR_{inM}, Read
3. MDR_{outP},IRin
4. R_{2out},R_{3out},Add,R_{1in}

Step 1: The contents of PC are transferred to MAR through bus B.

Step 2: The instruction code from the addressed memory location is read into MDR.

Step 3: The instruction code is transferred from MDR to IR register. At the beginning of step 4, the instruction decoder interprets the contents of the IR.

This enables the control circuitry to activate the control signals for step 4, which constitute the execution phase.

Step 4: two operands from register R_2 and register R_3 are made available at A and B inputs of ALU through bus A and bus B.

These two inputs are added by activation of Add signal and result is stored in R_1 through bus C.

8) Explain Hardwired control unit organisation with the help of necessary diagrams

The control units use fixed logic circuits to interpret instructions and generate control signals from them.

The fixed logic circuit block includes combinational circuit that generates the required control outputs for decoding and encoding functions.

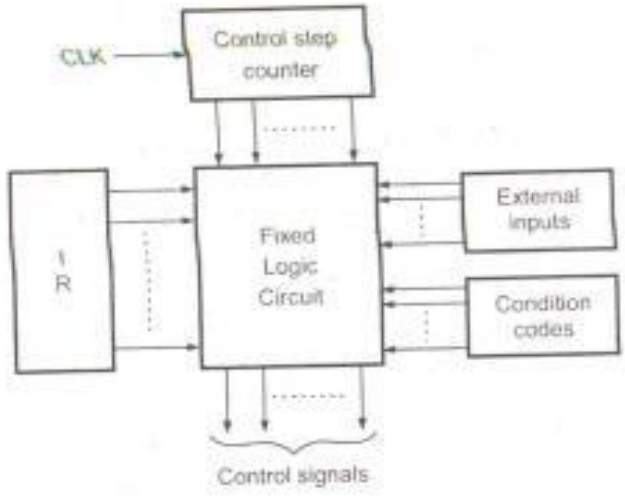


Fig. 3.10 Typical hardwired control unit

decoder decodes the instruction loaded in the IR

Instruction decoder

It decodes the instruction loaded in the IR.

If IR is an 8 bit register then instruction decoder generates 2^8(256 lines); one for each instruction.

According to code in the IR, only one line amongst all output lines of decoder goes high (set to 1 and all other lines are set to 0).

Step decoder

It provides a separate signal line for each step, or time slot, in a control sequence.

Encoder

It gets in the input from instruction decoder, step decoder, external inputs and condition codes.

It uses all these inputs to generate the individual control signals.

After execution of each instruction end signal is generated this resets control step counter and make it ready for generation of control step for next instruction.

The encoder circuit implements the following logic function to generate

Y_{in} $\mathbf{Y_{in} = T_1 + T_5 . Add + T . BRANCH+…}$

The Y_{in} signal is asserted during time interval T_1 for all instructions, during T_5 for an ADD instruction, during T_4 for an unconditional branch instruction, and so on.

As another example, the logic function to generate Z_{out} signal can given by

$\mathbf{Z_{out} = T_2 + T_7 . ADD + T_6 . BRANCH +….}$

The Z_{out} signal is asserted during time interval T_2 of all instructions, during T_7 for an ADD instruction, during T_6 for an unconditional branch instruction, and so on.

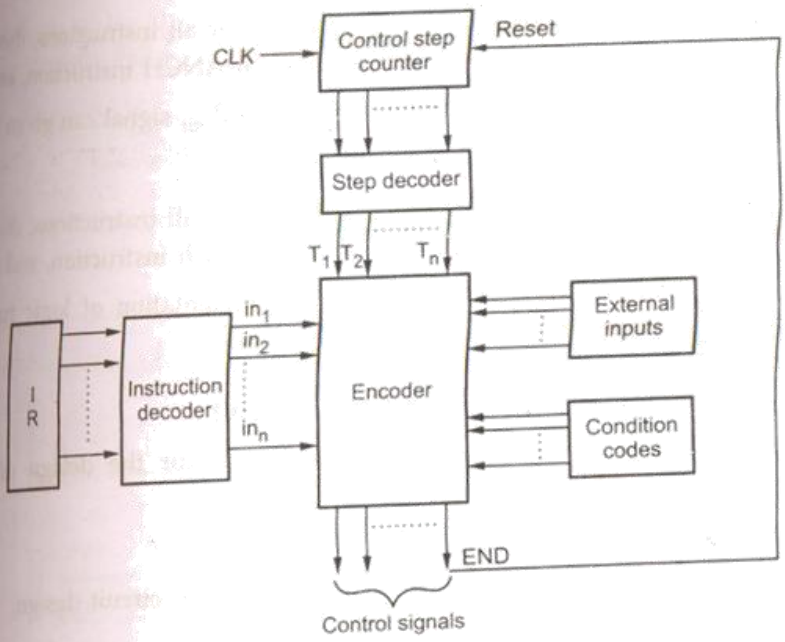
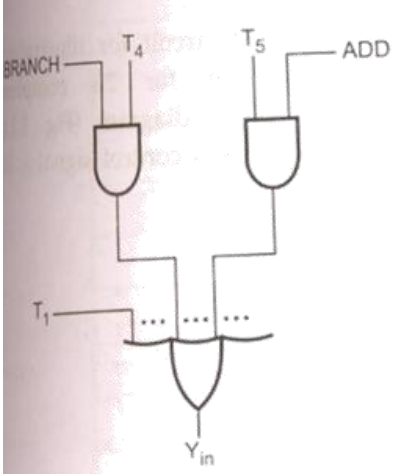


Fig. 3.11 Detail block diagram for hardwired control unit

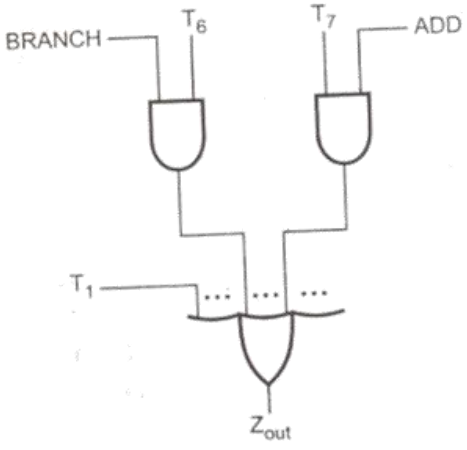
Let us see how the encoder generates signal for single bus processor organisation wn in Fig. 3.12 Y_{in}. The encoder circuit implements the following logic function to erate Y_{in}.

$$Y_{in} = T_1 + T_5 \cdot ADD + T_4 \cdot BRANCH + \cdots$$



Generation of the Y_{in} control signal

Fig. 3.12



Generation of the Z_{out} control signal

Fig. 3.13