CMR INSTITUTE OF TECHNOLOGY

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Internal Assesment Test - III

Sub:	**Basic Electronics**							Code: 18ELN14

Marks

1.a Explain the working of transistor as Voltage amplifier **[6]**

BJT as an Amplifier: (Voltage Amplifier)

→ Amplification is the process of linearly increasing the amplitude of an electrical signal and is one of the major properties of Transistor.

→ BJT is biased in Active region (linear region), the EB Junction has low resistance due to forward bias (F.B) and CB Junction has a high resistance due to R.B.

→ Transistor amplifies Current because the Collector Current is equal to the base Current multiplied by Current gain 'β'.

$$i.e \quad I_c = \beta \cdot I_b$$

→ The Base Current is small Compared to the Collector Current & Emitter Current, Because of this Collector Current approximately equal to the Emitter Current.

→ An A.C Voltage V_s, Super imposed on the dc bias vtg V_{BB} by Capacitive Coupling as shown in figure.

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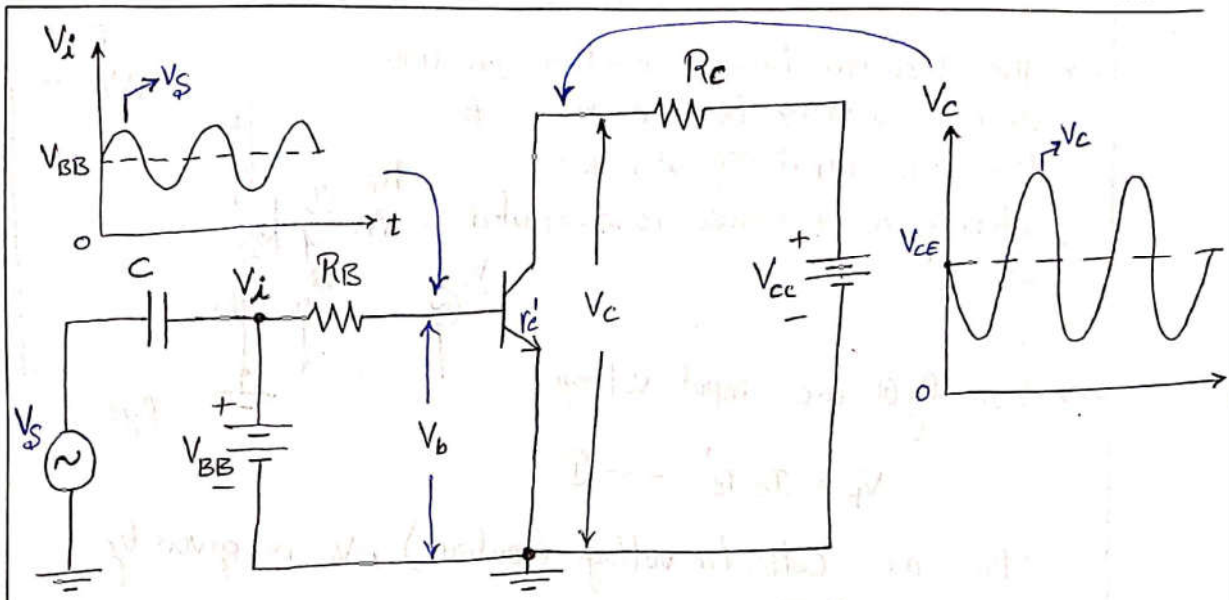

Basic Tr Amplifier Circuit

r_e' – internal ac emitter resistance

→ An A.C voltage V_s to be amplified is super imposed on the d.c bias voltage V_{BB} by capacitive coupling shown above. The d.c bias voltage V_{cc} is connected to the collector through collector resistor R_c.

→ The a.c input voltage V_s produces an a.c base current which results in much larger a.c voltage across R_c, which is amplified and inverted version of ac input voltage as shown in above waveform.

→ A.C equivalent ckt is written to analyze the voltage gain of amplifier.

→ Equivalent circuit can be obtained by making all D.C bias voltage equal to zero i.e. $V_{BB}=0$ and $V_{cc}=0$.

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→ The forward biased emitter junction exibits a very low resistance to the a.c input signal, this internal A.c resistance is designated as r_e'

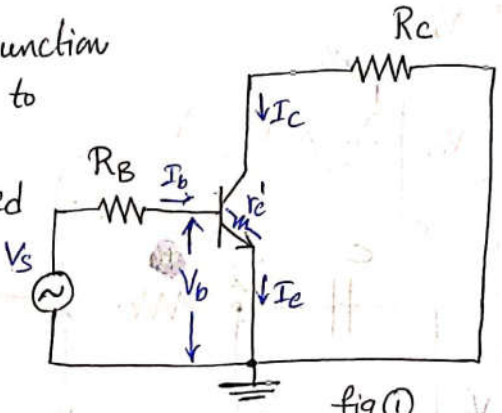

fig ①

→ from fig ① a.c input voltage

$$V_b = I_e \cdot r_e' \quad \text{—①}$$

the a.c Collector voltage (output), V_c is given by

$$V_c = I_c \cdot R_c$$

since $I_c \simeq I_e$, the Collector vtg is

$$V_c \simeq I_e \cdot R_c \quad \text{—②}$$

and also we can write $V_b = V_s - I_b \cdot R_B$

→ V_b can be Considered as tr a.c input vtg and
V_c can be " as transistor output voltage

→ Since the vtg gain is the ratio of the output voltage to the input voltage, the ratio of V_c to V_b is the vtg gain, A_v

from eq ① & ②

$$A_v = \frac{V_c}{V_b} = \frac{I_e \cdot R_c}{I_e \cdot r_e'}$$

So $$\boxed{A_v \simeq \frac{R_c}{r_e'}}$$

since $R_c \gg r_e'$, the output is always grater than input voltag i.e the output voltage V_c is amplified version of V_b.

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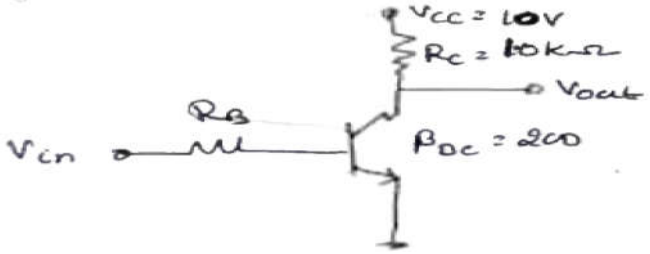
1 (b) The transistor in CE Configuration is shown in figure. With R_C = 10 KΩ, β_{DC} = 200, V_{CC} = 10 V, $V_{CE(sat)}$ is neglected. Determine when V_{in} = 5V (i) $I_{B\,min}$ (ii) R_{Bmax} [4] CO1



(a) When V_{IN} = 0 V, the transistor is in cutoff (acts like an open switch) Therefore, $V_{CE} = V_{CC} = 10$ V

(b) Since $V_{CE(sat)}$ is neglected , assume $V_{CE(sat)}$ =0 V

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$$I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{10\text{ V}}{1.0\text{ k}\Omega} = \text{10 mA}\ \ 1\text{mA}$$

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta} = \frac{10\text{ mA}}{200} = \text{50 µA}\ \ 5\mu\text{A}$$

This is the value of I_B necessary to drive the transistor to the point of saturation. Any further increase in I_B will ensure the transistor remains the saturation but there cannot be any further increase in I_C

(c) When the transistor is on, $V_{BE} \sim$ 0.7 V. The voltage across R_B is

$$V_{R_n} = V_{IN} - V_{BE} \simeq 5\text{V} - 0.7\text{ V} = 4.3\text{ V}$$

Calculate the maximum value of R_B needed to allow a minimum I_B of 50 µA using Ohm's law as follows:

$$R_{B(max)} = \frac{V_{R_n}}{I_{B(min)}} = \frac{4.3\text{ V}}{\text{50 µA}} = 86\text{k}\Omega \quad 860\text{K}\Omega$$

$5\mu A$

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2 **List the types of feedback system. Derive the gain with feedback expression for Voltage series feedback amplifier.** **[10]**

Types of Feedback :-

There are four basic types :-

1. Voltage Series feedback
2. Voltage-Shunt feedback
3. Current-Series feedback.
4. Current-Shunt feedback.

→ Here, voltage refers to connecting the output volta as input to the feedback network.
→ Current refers to tapping off some output curre through the feedback network.
→ Series refers to connecting the feedback signal i series with the input signal voltage.
→ Shunt refers to connecting the feedback signal i Shunt (parallel) with an input current source.

NOTE :- (1) Series feedback connection increases the input Res while Shunt feedback connections decreases the input Res

(2) Voltage Feedback (3) decreases the output impedan while current feedback increases the output impedan

→ Typically higher input and lower output impedanc are desired. Both of these are provided us Voltage-Series feedback connection.

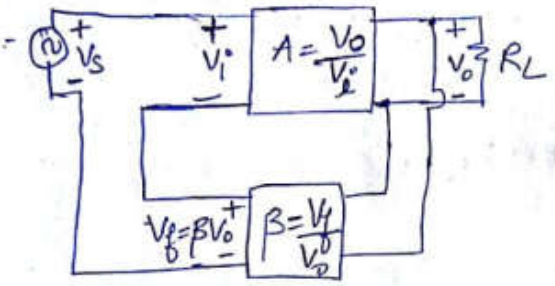
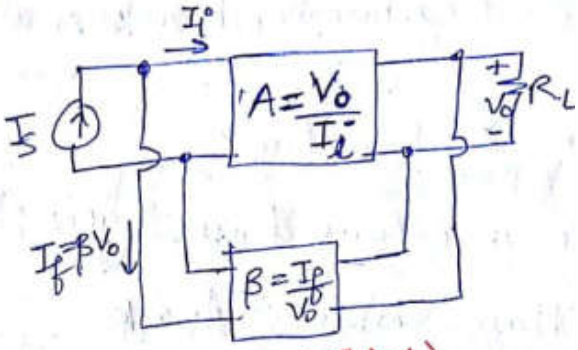
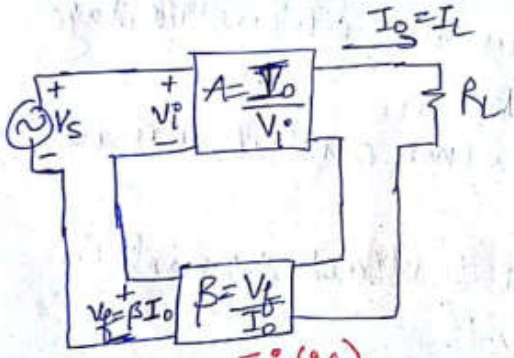


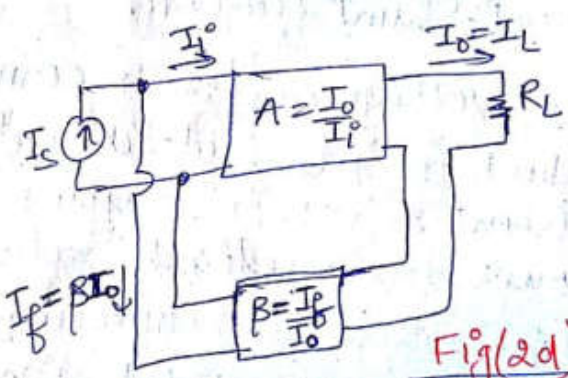
Fig 2(a)
Voltage-Series Feedback Amplifier ($A_f = \frac{V_o}{V_s}$)



Fig(2b)
Voltage-Shunt Feedback Amplifier. ($A_f =$



Fig(2c)
Current-Series Feedback Amplifier ($A_f = \frac{I_o}{V_s}$)



Fig(2d)
Current-Shunt Feedback Amplifier ($A_f =$

Fig(2):- Different Types of feedback Amplifier/Conne

Voltage Series feedback :- (4)

As shown in Fig(a) ie Voltage Series feedback circuit

If $V_f = 0$, the voltage gain of Amplifier Stage i

$$A = \frac{V_o}{V_s} = \frac{V_o}{V_i} \quad \text{— (1)}$$

with

V_s V_i

If feedback signal V_f is connected in series with input, then,

$$V_i = V_s - V_f \quad \text{---} (2)$$

$$\Rightarrow \boxed{V_o = AV_i} = A(V_s - V_f)$$

eq^n (1)

$$V_o = AV_s - AV_f \Rightarrow V_o = AV_s - A(\beta V_o)$$

since $\beta = \frac{V_f}{V_o}$

$$\Rightarrow V_o(1 + A\beta) = AV_s$$

$$\Rightarrow \frac{V_o}{V_s} = \frac{A}{1+A\beta}$$

$$\Rightarrow \boxed{A_f = \frac{V_o}{V_s} = \frac{A}{1+A\beta}} \quad \text{---} (3)$$

A_f is the overall gain with feedback.

→ eq^n (3) shows that gain with feedback is the amplifier gain reduced by factor $(1+A\beta)$.

A_f → is voltage gain with feedback.

3 **Explain Barkhausen's criteria. Explain the working of Wien Bridge oscillator with the help of circuit and derive the frequency of oscillation.** **[10]**

Barkhausen Criterion for Oscillation

Consider a basic inverting Amplifier with an open loop gain A. The feedback network attenuation factor β is less than unity. As basic amplifier is inverting, it produces a phase shift of 180° between input and output. as shown in fig (a).

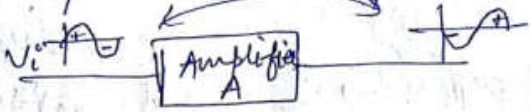


Fig (a) :- Inverting Amplifier

→ But the feedback must be +ve ie voltage derived from output using feedback network must be in phase with V_i. Thus feedback network must introduce a phase shift of 180°. This ensures positive feedback.

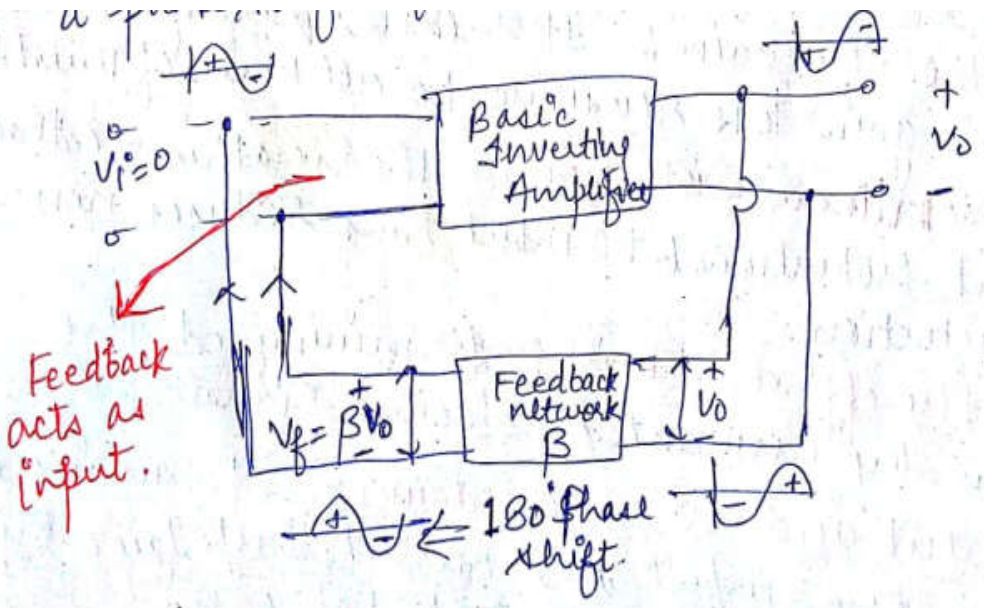


Fig (b) :- Basic Block diagram of oscillator circuit.

Consider a fictitious voltage V_i applied at input of amplifier so,

$$V_o = A V_i' \quad \text{— (1)}$$

now $V_f = \beta V_o$ — (2)

so Put V_f from eq^n (2) into eq^n (1)

$$\boxed{V_f = \beta A V_i'}$$

For oscillator, we want that feedback should drive the Amplifier hence V_f acts as V_i'

→ V_f is sufficient to act as V_i' when

$$|A\beta| = 1$$

The two condition are required to work the circuit as an oscillator, are called Barkhausen Criterion for Oscillation.

Barkhausen Criterion states that :-

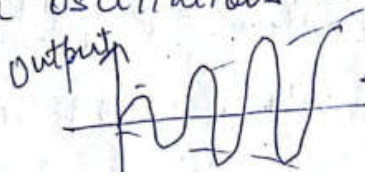
(1) The total phase shift around a loop, as signal proceeds from input through amplifier, feedback network back to input again, completing a loop is precisely 0° or 360°.

(2) The magnitude of the product of the open loop gain of amplifier (A) and magnitude of the feedback factor β is unity $|A\beta| = 1$

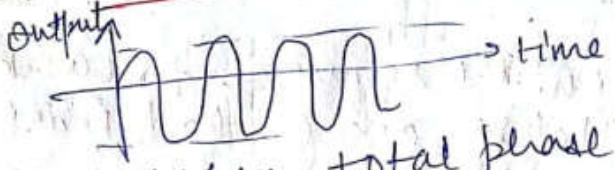
Satisfying above conditions, circuit works as an oscillator producing sustained oscillations of

constant frequency and amplitude.

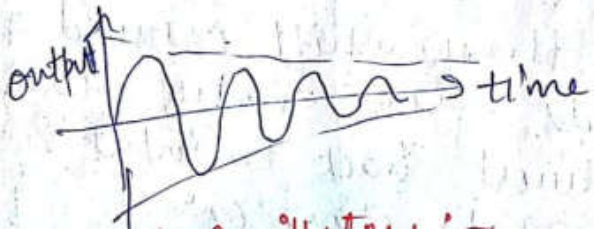
① $|AB| > 1$ → when total phase shift around a loop is 0° or 360° and $|AB| > 1$, then output oscillates but the oscillations are of growing type.



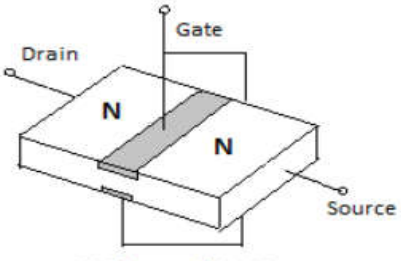
② $|AB| = 1$ → when total phase shift around the loop is 0° or 360° and $|AB| = 1$, then oscillations are with constant frequency and amplitude called as sustained oscillations.



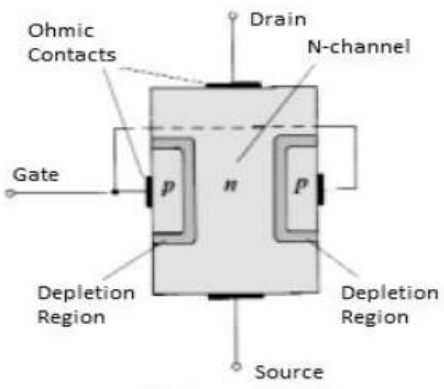
③ $|AB| < 1$ → when total phase shift is 0 or 36
but $|AB| < 1$ then oscillations are of decaying type.



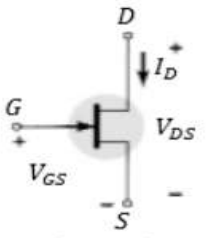
4 Explain the construction and working of JFET with drain characteristics and transfer characteristics. **[10]**



N-Channel JFET



N-Channel JFET

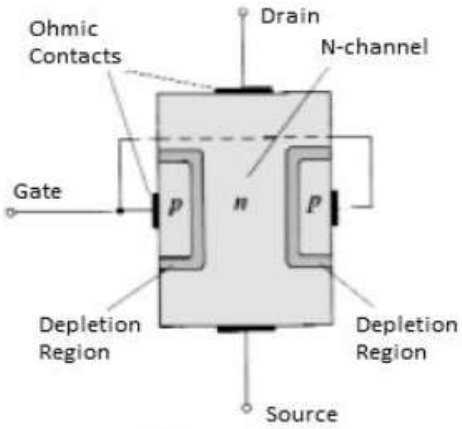


N-Channel JFET

FABRICATION OF N-CHANNEL JFET: (Construction)

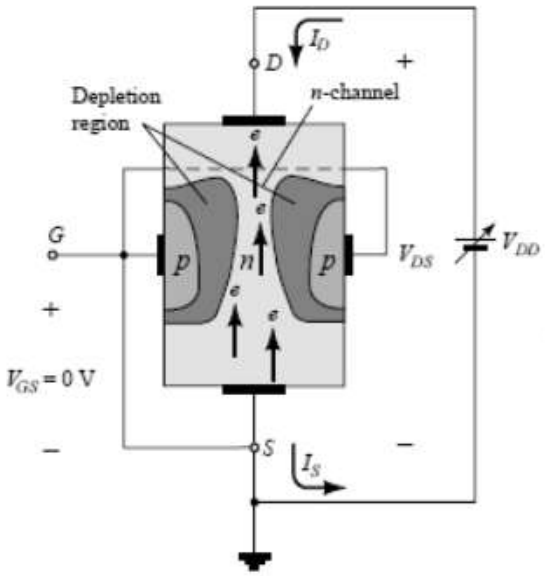
1. A narrow bar of N-type semiconductor material is taken. At its middle part, two havily doped p-type regions are formed by diffusion.
2. The junction form two P-N diodes or gates. The area between the gates is called a channel.
3. One end of the N-type bar is called as source terminal 'S'.
4. The other end of the N-type bar is called as drain terminal 'D'.
5. The souce and drain terminal may be interchanged.
6. When a potential difference is established between source and drain, a current flows from one end to the other end in N-type material.
7. This current consists of majority carriers i.e. electrons.
8. Following notations for FET should be remembered.
    a) SOURCE: The source 'S' is the terminal through which majority carrier enter the bar.
    b) DRAIN: The drain 'D' is the terminal through which the majority carrier leave the bar.
    c) GATE: These are heavily doped regions which forms two P-N junctions.
    d) CHANNEL: The space between two gates through which majority carriers pass.

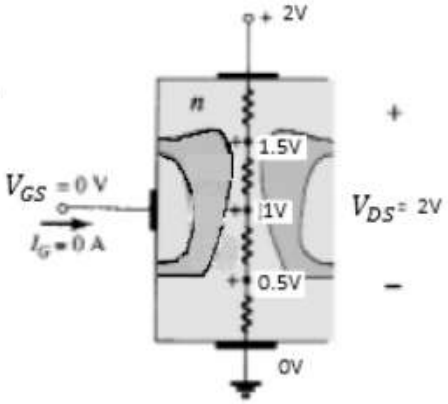
OPERATION OF N-CHANNEL FET:



N-Channel JFET

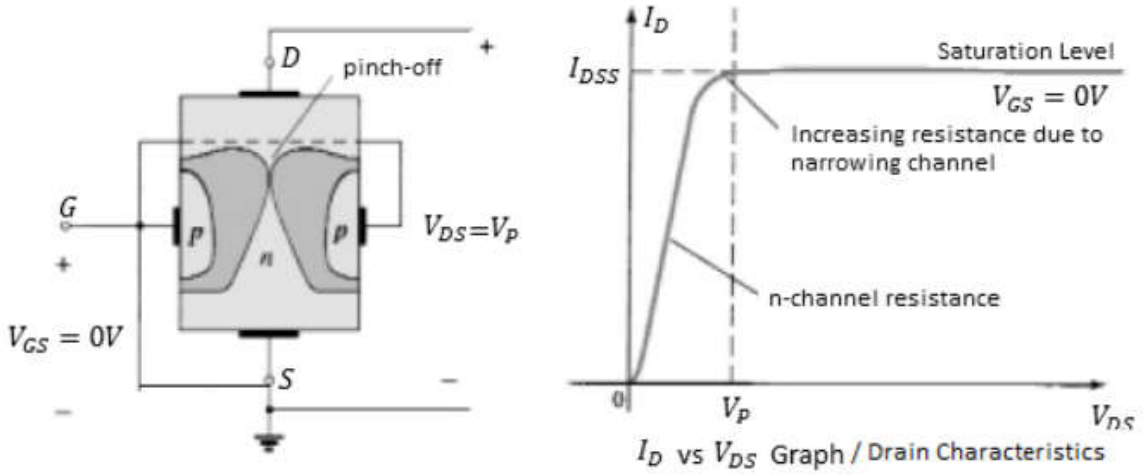
1. When no volatges are applied, the depletion regions were uniformly distributed.
2. As a positive voltage is applied across the channel and the gate is connected directly to the source to establish the condition $V_{GS} = 0V$. Then the width of the depletion region starts increasing.
3. As V_{DD} is applied , the electrons are drawn to the drain terminal, hence a current will flow in a defined direction.
4. The path of charge flow clearly define that $I_D = I_S$
5. The depletion region is wider near the top of both the P-type material.





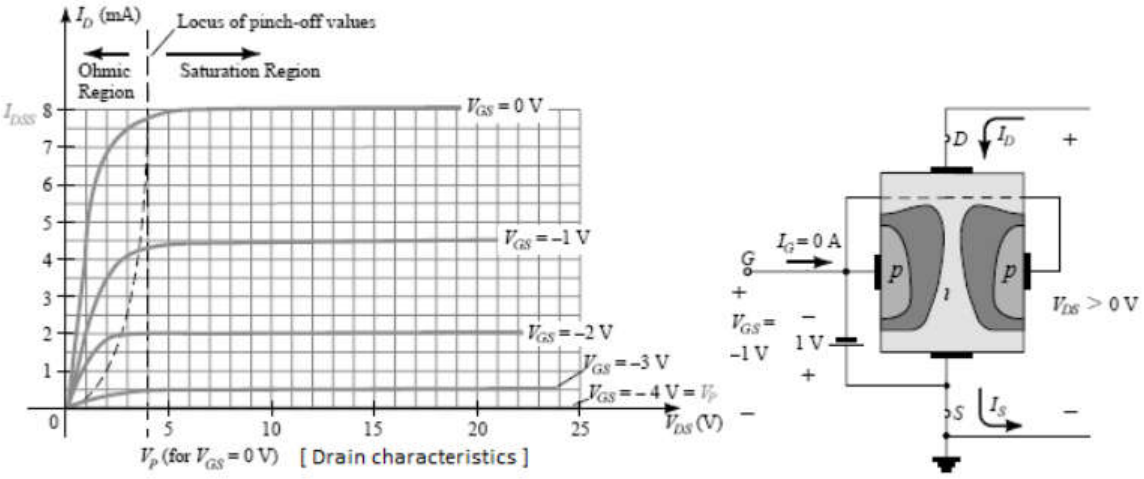
6. Assume a uniform resistance in the N-channel, we can break down the resistance into some division.
7. The upper region of the P-type material will be reverse biased by 1.5V comparision with the lower region.
8. We know from the diode operation, the greater the applied reverse bias, the wider is the depletion region. Hence the depletion region is shown like this.
9. As V_{DS} increases and approaches a level referred as V_P, the depletion region will widen, causing a reduction in channel width. The reduced path of conduction causes the resistance to increase.
10. When two depletion region touch the condition is referred to as pinch-off.

11. The level of V_{DS} that establishes this condition is known as pinch-off voltage and denoted as V_P
12. In actuallity pinch-off suggests, the current I_D is pinched off and drop to 0V, but in reality a very small channel still exists, with a very high current density. Hence the I_D doesn't drop at pinch-off but maintains the saturation level.

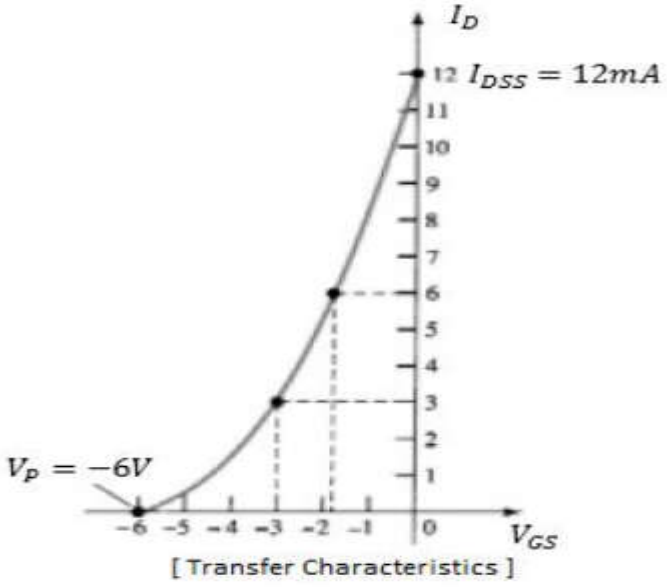


I_D vs V_{DS} Graph / Drain Characteristics

13. I_{DSS} is the maximum drain current for a JFET and is defined by the condition $V_{GS} = 0V$ and $V_{DS} \geq |V_P|$
14. The voltage from gate to source V_{GS} is the controlling voltage of JFET. The reason to apply –ve bias V_{GS} is to establish depletion region similar to those obtained with $V_{GS} = 0V$ but at lower level of V_{DS}. Hence saturation level can be achieved at lower V_{DS}.



TRANSFER CHARACTERISTICS:



[Transfer Characteristics]

5 (a) Explain the working of CMOS Inverter with relevant circuit. **[5]**

→CMOS is Complementary Metal Oxide Semiconductor which is a technology used for constructing integrated circuits.

→CMOS circuitry has advantages :-

(i) Low static power consumption.

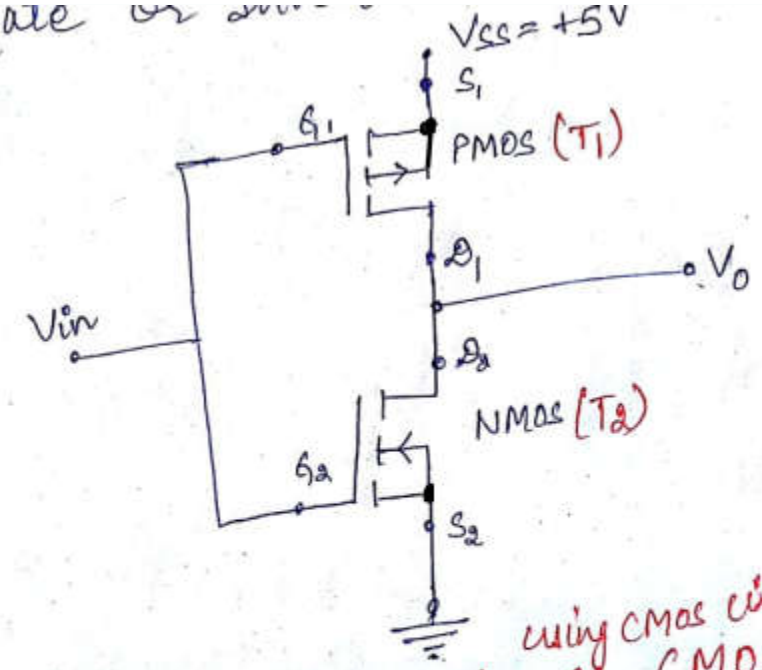
(ii) High Noise Immunity.

→CMOS circuits use a combination of P-type and N-Type MOSFET's to implement logic gates and other digital circuits.

CMOS circuit can be used to implement NOT Gate or Inverter as shown in the figure below.

$V_{SS} = +5V$

gate or



Fig(a) :- NOT Gate using CMOS circuit or CMOS Inverter

→ Fig(a) shows CMOS Inverter which uses an enhancement Type NMOS and an enhancement type PMOS.

→ The source of PMOS (T_1) is connected to V_{SS} = +5V, while the source of NMOS(T_2) is grounded.

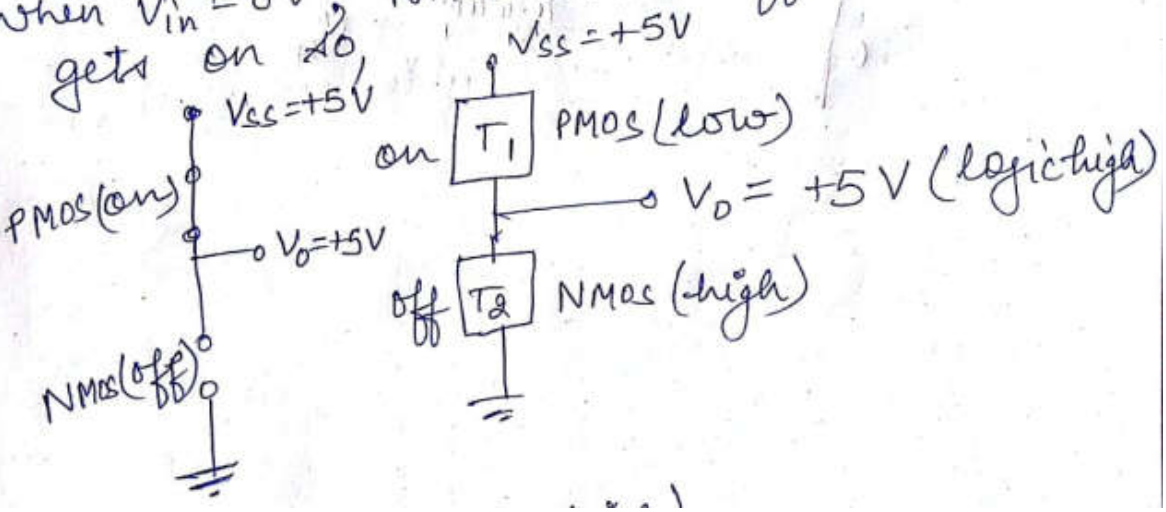
→ The Gates G_1 and G_2 are shorted together and input is provided at the gate.

→ The Drains D_1 and D_2 are shorted and output is obtained at drain as V_o.

Operation :-

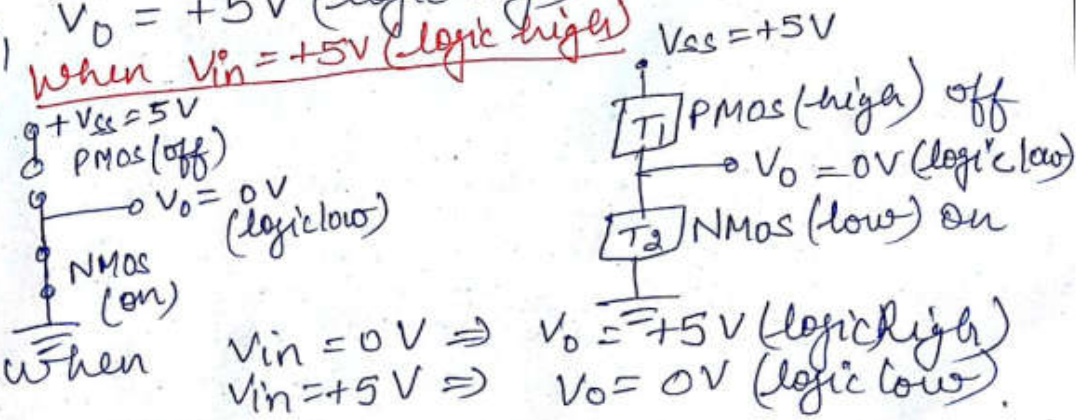
Case-1 When $V_{in} = 0V$ (logic low),

→ When $V_{in} = 0V$, NMOS will be off and PMOS gets on so,



So, $V_o = +5V$ (logic high)

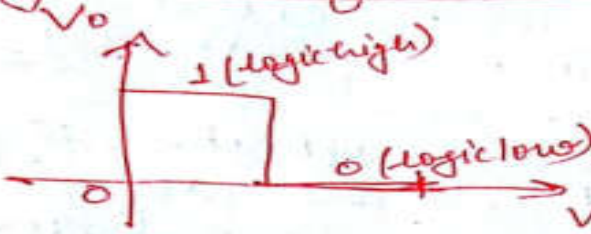
Case-2 When $V_{in} = +5V$ (logic high)



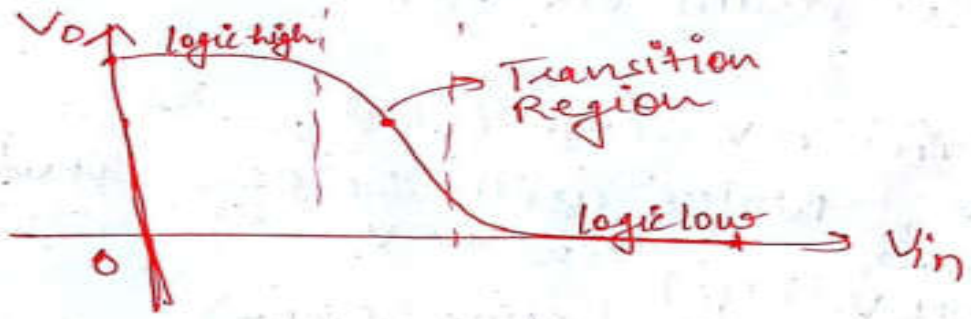
So, when $V_{in} = 0V \Rightarrow V_o = +5V$ (logic High)

$V_{in} = +5V \Rightarrow V_o = 0V$ (logic low).

Voltage Transfer characteristics



Ideal characteristics

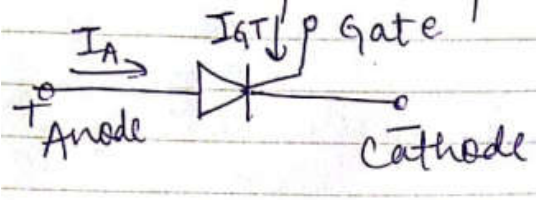


[5]

5 (b) Explain SCR as two transistor model.

Silicon Controlled Rectifier (SCR) :-

SCR is a rectifier constructed of Silicon material with three terminals namely gate, Anode and Cathode. Silicon is choosen because of high temperature and power capabilities.



Fig(a) :- Symbol

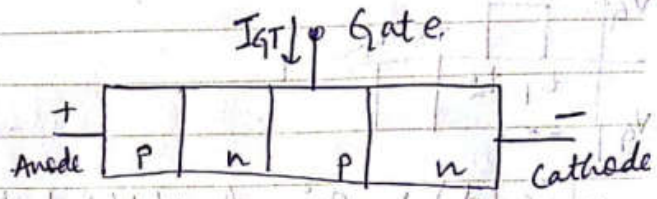
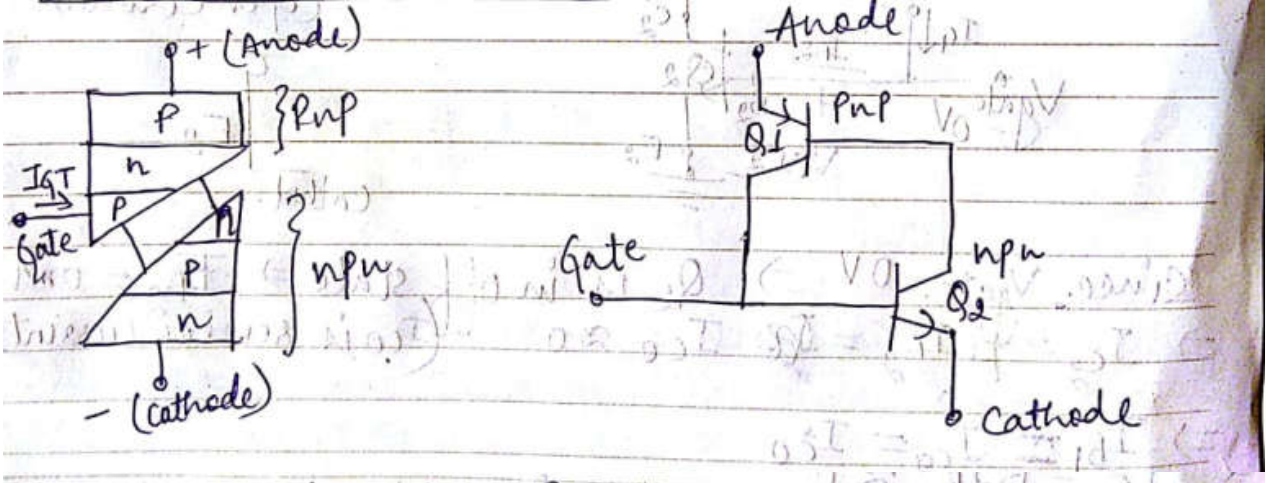


Fig (b) :- Basic Construction.

SCR is basically a four layer PnPn structure as shown in fig (b).

The operation of SCR can be explained using two transistor model.



Fig(c) SCR two transistor model

SCR is splitted into two three layer transistor

structures as shown in fig (c). One transistor is npn device while the other is pnp device.

A signal as shown in fig (d) is applied at the gate of SCR.

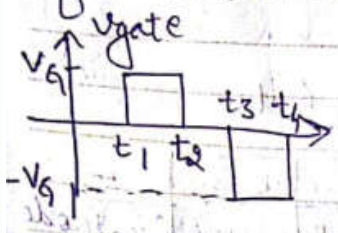
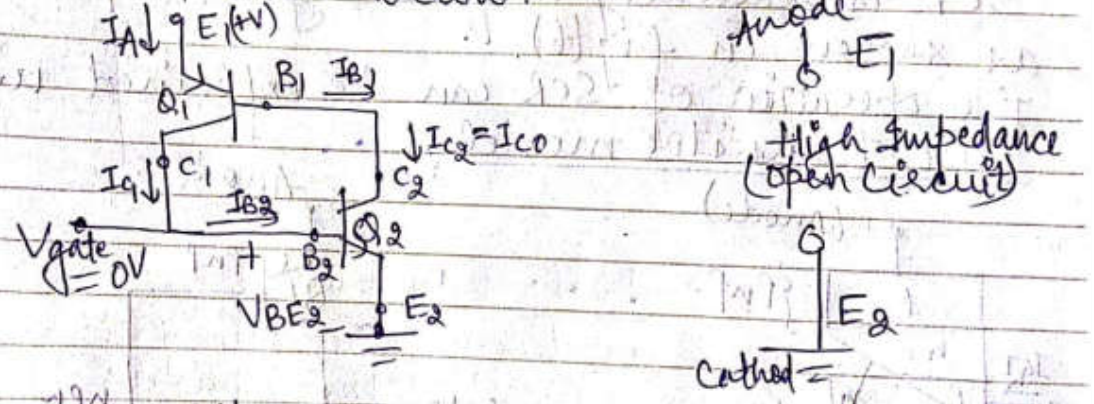


fig (d) :- Signal applied at the gate of SCR.

During the interval $0 \to t_1$, $V_{gate} = 0V$, the circuit appears as shown below.



Since $V_{gate} = 0V \Rightarrow Q_2$ is in off state $\Rightarrow I_{B_2} = 0$ mA

$\Rightarrow I_{C_2} = \beta I_{B_2} = I_{CO} \approx 0$ (I_{CO} is reverse current)

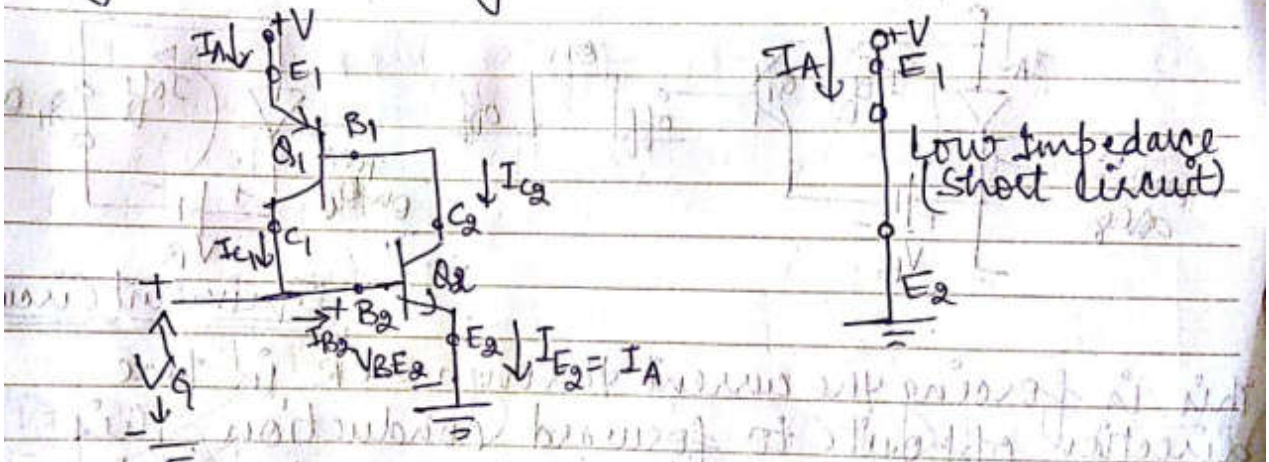
$\Rightarrow I_{B_1} \cong I_{C_2} = I_{CO}$

$\Rightarrow I_{C_1} = \beta I_{B_1} \approx 0$

So, $I_A \approx 0$ (so, transistors are in off state and thus replaced by open circuit or high impedance between collector and emitter)

(2) At $t = t_1$, a pulse of V_g volts is applied at the gate of SCR. V_g is large so, Q_2 turns on and thus there is I_{B_2} and $I_{C_2} = \beta I_{B_2}$ in the circuit.

$I_{B_1} = I_{C_2}$ so the transistor Q_1 turns on and thus a current I_{C_1} flows through it. This increase or flow of I_{C_1} corresponding increases I_{B_2}. The increase in I_{B_2} further increases I_{C_2}. The net result is regenerative increase in collector current of each transistor. Thus anode to cathode resistance ($R_{SCR} = \frac{V}{I_A}$), since I_A is large R_{SCR} is very small.



→ SCR cannot be turned off by simply removing the gate signal thus negative pulse is needed to applied at the gate of SCR. ie at $t = t_3$.

Methods to turn-off SCR :-

There are two Methods :-

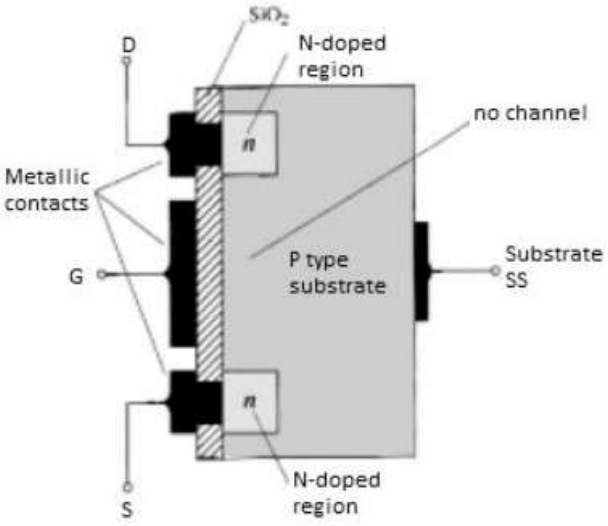
(1) Natural commutation or Anode Current Interuption Technique.

(2) Forced-Commutation Technique.

6 Explain the construction and working of n channel enhancement type MOSFET with relevant drain characteristics and transfer characteristics. [10]

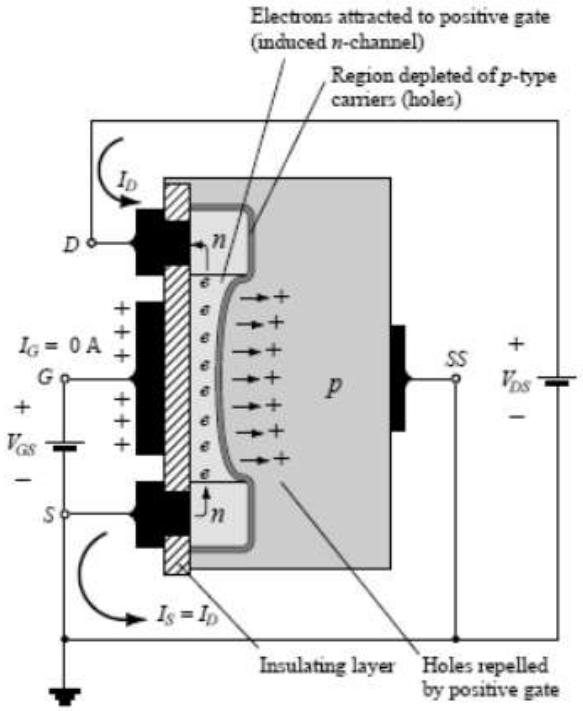
Construction of N-channel Enhancement type MOSFET:

The construction of n-channel enhancement type MOSFET is similar to the construction of depletion type MOSFET. Here the channel between the two n-doped regions is absent. This is the primary difference between the construction of depletion type and enhancement type MOSFET.

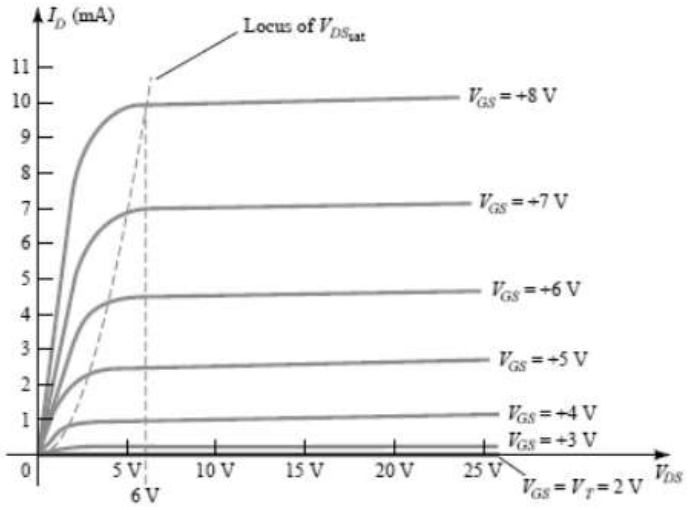


N- Channel Enhancement Type MOSFET

OPERATION:



1. Although some positive V_{DS} is applied, as the $V_{GS} = 0V$, no channel exists hence the current through the device is 0A i.e. $I_D = I_S = 0A$
2. As some positive voltage V_{GS} is applied to the gate terminal, the positive potential at the gate will pressure the holes in the p-substrate. Electron in the p substrate will be attracted to the positive gate and accumulated in the region near to the surface of SiO_2 layer.
3. As V_{GS} increases in magnitude, the concentration of electron near SiO_2surface increases.
4. V_{GS} has to be increased until the induced N-type region can support the flow of current.
5. The level of V_{GS} that results in the significant increase in drain current is called the threshold voltage and represented as V_T or $V_{GS(Th)}$



6. The current is nonexistent with $V_{GS} = 0V$ and enhanced by the application of positive gate to source voltage, this type of MOSFET is called as enhancement type MOSFET.
7. Both depletion and enhancement type MOSFET have enhancement type region.
8. If we keep V_{GS} as constant and increase the V_{DS}then the drain current will increase and reach the saturation level.

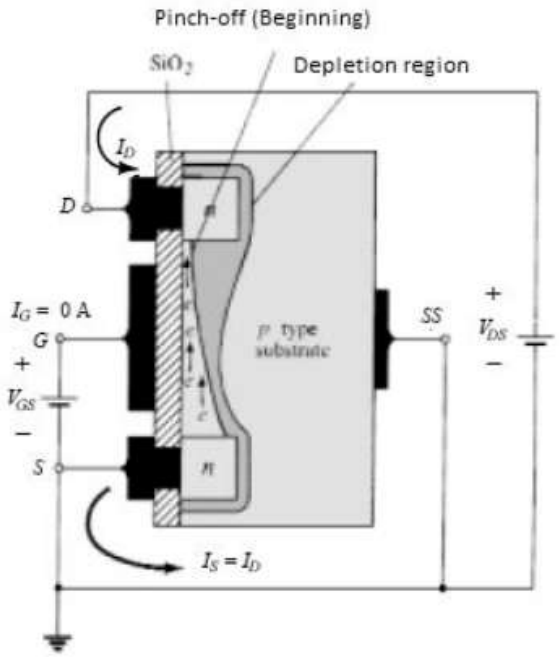
Applying KVL to the terminal

$V_{DG} = V_{DS} - V_{GS}$

$Let \quad V_{GS} = 8V \quad and \quad V_{DS} = 2 \; to \; 5V \; (i.e. increasing \; from \; 2 \; to \; 5V)$

$V_{DG} \; drops \; from -6V \; to -3V$

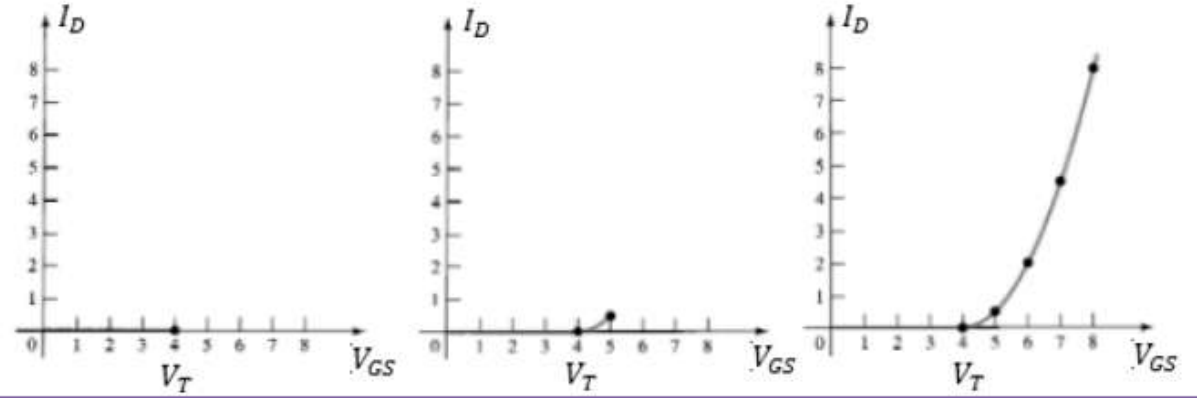
9. This reduction in gate to drain voltage will reduce the attractive force for free carriers, causes reduction in channel width.



10. The channel will be reduced to the point of pinch off and saturation condition will be established.
11. But any further increase in V_{DS} at the fixed value of V_{GS} will not affect the saturation level of I_D until breakdown condition occurs.
    $V_{DS(Sat)} = V_{GS} - V_T$
12. For fixed V_T ,higher the level of V_{GS} the greater will be the saturation level of V_{DS}
13. For V_{GS} less than the threshold voltage, the drain current of an enhancement type MOSFET is 0mA.
14. As V_{GS} increases from V_T, the resulting saturation level for I_D also increases.

15. For $V_{GS} > V_T$, the drain current is related to the applied gate to source voltage by the following relationship.
    $I_D = k(V_{GS} - V_T)^2$
    $Where \quad k = constant \; and \; it \; is \; a \; function \; of \; the \; construction \; of \; the \; device$

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$$



7(a) For a N-channel JFET if I_{DSS} = 8mA & $V_P = V_{GS(off)}$= -5V, calculate I_D at V_{GS} = -3 V and V_{GS} at I_D = 3 mA. **[5]**

⑦@ $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$

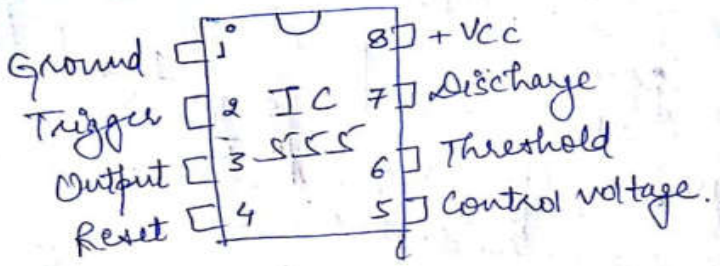
$I_D\Big|_{V_{GS}=-3V} = 1.28mA$

$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right) = -1.938V$

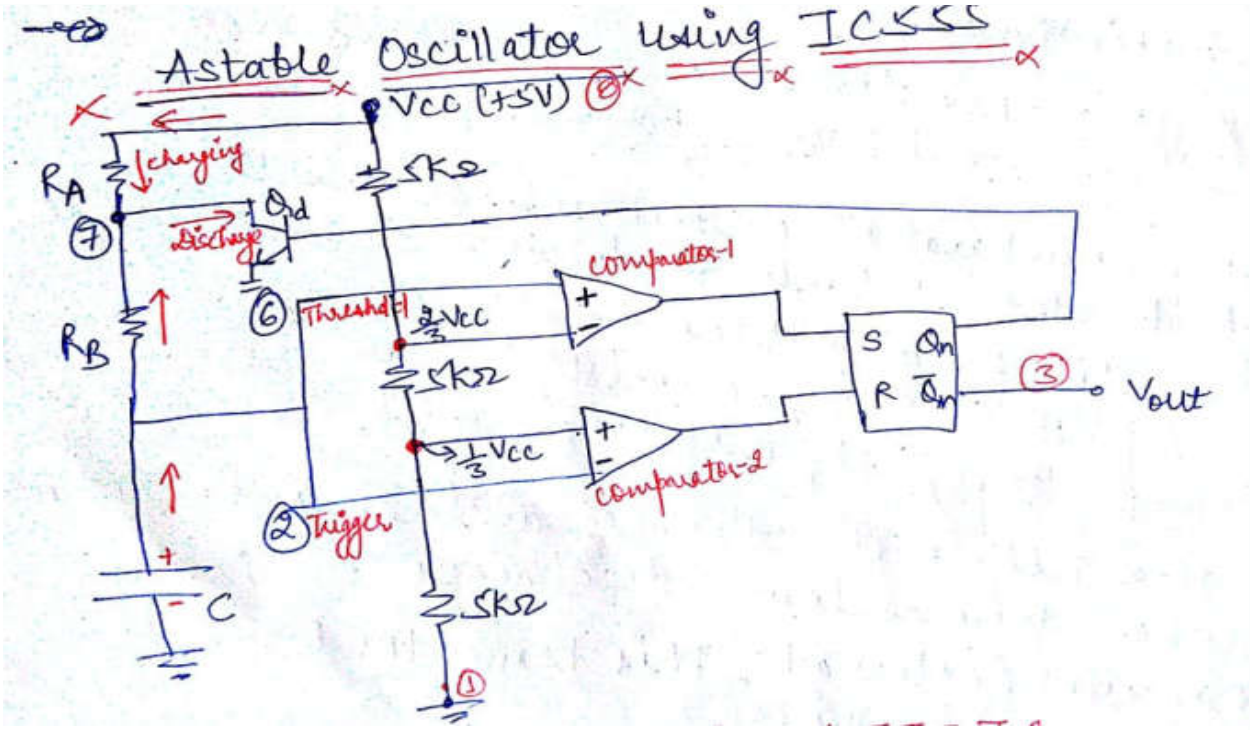
7(b) Explain the working of 555 Timer as astable oscillator with necessary equations. **[5]**

IC 555 Timer :- It is a versatile analog-digital integrated circuit. Entire circuit is housed in an 8-pin package.

Pin diagram of IC 555 :- It has 8 pins.



Astable Oscillator using IC555



Fig(a) shows IC555 connected as Astable oscillator/ Multivibrator. The threshold input is connected to trigger input. The two external resistances R_A, R_B and a capacitor C is used in the circuit.

→ The circuit has NO stable state. The circuit changes its state alternately. Hence the operation is also called free Running non-sinusoidal Oscillator.

Operation:-

→ When flip flop is set, Q_n is high which drives transistor Qd in saturation and capacitor gets discharged.

→ Now the capacitor voltage is just the trigger voltage. So, while discharging, when it becomes less than $\frac{1}{3}$Vcc, then comparator 2 output goes high. This resets the flip flop hence $\overline{Q_n}=1$ or high

→ since $\overline{Q_n}=1 \Rightarrow Q_n=0 \Rightarrow$ Qd transistor will be in cutoff and thus capacitor starts charging through the resistances R_A, R_B and Vcc.

Charging Time constant is $(R_A+R_B)C$.

charging Time constant

→ Now the capacitor voltage is also a threshold voltage. While charging capacitor voltage increases and thus threshold voltage increases. When it exceeds $\frac{2}{3}V_{CC}$, then comparator-1 output goes high which sets the flip-flop and thus Q_n is high and $\overline{Q_n}$ becomes low.

Discharging Time constant is $R_B C$.

→ When ~~comparator-2~~ capacitor voltage becomes less than $\frac{1}{3}V_{CC}$, comparator-2 output goes high, resetting the flip-flop. This cycle repeats.

→ When capacitor charges, output is high while when it is discharging the output is low.

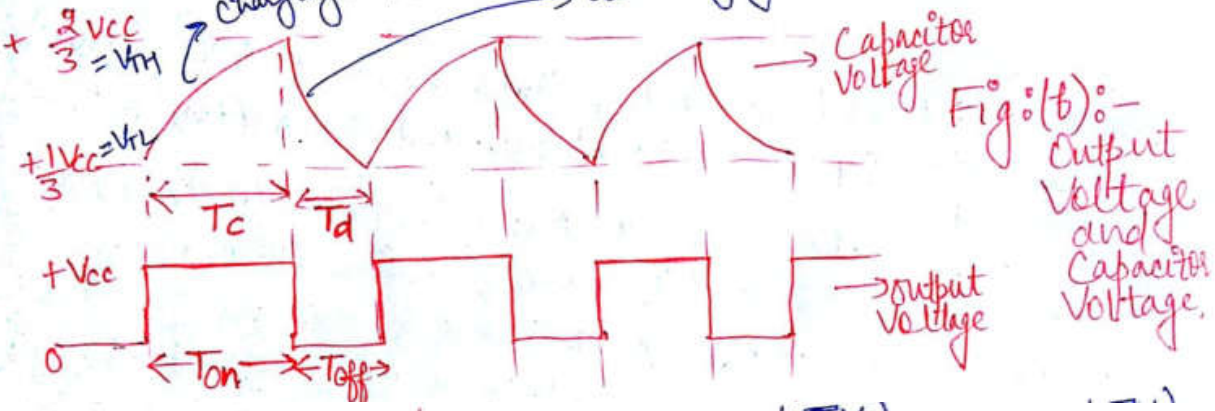
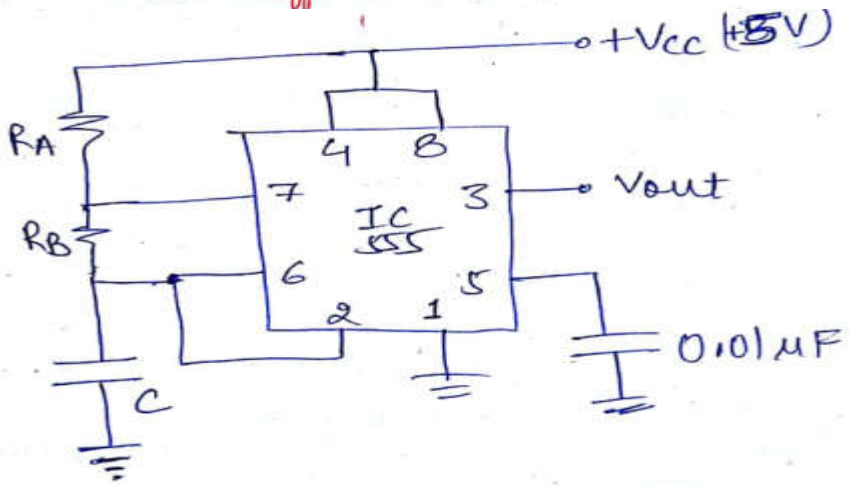


Fig:(b):- Output Voltage and Capacitor Voltage.



Fig(c):- Schematic diagram of Astable Oscillator using IC 555.

Duty cycle :-

It is defined as the ratio of high output (i.e on time) to the total time of one cycle.

$$D = \frac{T_{on}}{T_{on}+T_{off}} \times 100\% \text{ or } \frac{T_c}{T_c+T_d} \times 100\%$$

charging Time for the capacitor $(T_c) = 0.693(R_A+R_B)C$

Discharging " " " " $(T_d) = 0.693(R_B)C$

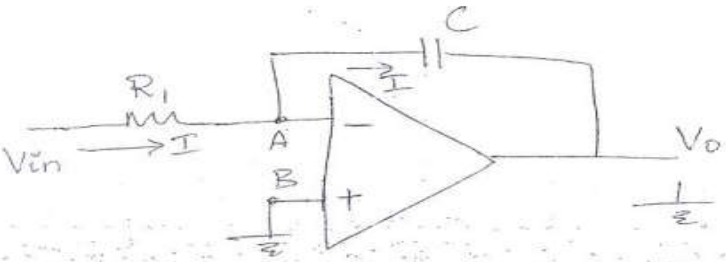
$$T = T_c + T_d = 0.693(R_A+2R_B)C$$

$$\Rightarrow D\% = \frac{0.693(R_A+R_B)C}{0.693(R_A+2R_B)C} \times 100$$

$$\boxed{D\% = \frac{R_A+R_B}{R_A+2R_B} \times 100}$$

Astable Time :-

8(a) Explain the working of Integrator using op-amp and derive the output expression. **[5]**



By virtual ground concept,

$$V_A = V_B = 0$$

As input current of op-Amp is zero, the entire current I flowing through R_1, also flows through C.

From fig

$$I = \frac{V_{in} - V_A}{R_1} = \frac{V_{in}}{R_1} \quad \text{—(1)}$$

From o/p side,

$$I = C \frac{d(V_A - V_o)}{dt}$$

$$I = -C \frac{dV_o}{dt} \quad -(2)$$

Eq (1) & (2)

$$\frac{V_{in}}{R_1} = -C \frac{dV_o}{dt}$$

Integrating both sides

$$\int_0^t \frac{V_{in}}{R_1} = -\int_0^t C \frac{dV_o}{dt}$$

$$V_o = -\frac{1}{R_1 C} \int_0^t V_{in} \cdot dt$$

Thus o/p is integration of input. hence called integrator where RC is called time constant of integrator

→ Integration of Step waveform is Ramp waveform

→ " " Square " " Triangular "

" " Sine " " neg Cosine

Also Draw wave forms

8.b) Design the circuit using opamp's for Vo= - (2V1+3V2+6V3) for Rf=10KΩ. **[5]**

(8b)

$$V_0 = -(2 \cdot V_1 + 3 \cdot V_2 + 6 \cdot V_3)$$

$$V_0 = -\left[\frac{R_f}{R_1}(V_1) + \frac{R_f}{R_2} \cdot V_2 + \frac{R_f}{R_3} \cdot V_3\right]$$

$\frac{R_f}{R_1} = 2 \qquad \frac{R_f}{R_2} = 3 \qquad \frac{R_f}{R_3} = 6$

assuming $R_f = 10\,k\Omega$

$R_1 = 5\,k\Omega \qquad R_2 = 3.3\,k\Omega \qquad R_3 = 1.66\,k\Omega$

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