18EC56/17EC53/15EC53 Verilog HDL IAT1 question Paper

Verilog HDL IAT 1 :Digital Circuits Questions and Answers – Introduction to Hardware Description Language
This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Introduction to hardware description language”.

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SECTION *

A

1.RTL means *

- ○ Resister transistor Level
- ○ Register transfer Logic
- ○ Resister transfer Level
- ◉ Register transfer Level

2. VERILOG HDL IS *

- ◉ TRUE
- ○ FALSE

Logic Synthesis means *

- [x] Mapping the HDL constructs to an equivalent digital logic components
- [ ] Verifying the desired functionality of the digital circuit
- [ ] Imitating of a digital circuit
- [ ] None of the above

Testbench is used to *

- [x] used to test the design module to check the correctness of the desired functionality
- [ ] Design a digital circuit
- [ ] Both
- [ ] None

CAD is an acronym for *

- ( ) Computer Aided Drawing
- (•) Computer Aided Design
- ( ) Capture and Design
- ( ) None of the above

- ( ) Option 1

Verilog may be written at the Behavioral, Structural, Gate, Switch, and Transistor levels. *

- (•) True
- ( ) False

How many data select lines are required for selecting eight inputs in a mux ? *

- [ ] 1
- [ ] 2
- [x] 3
- [ ] all

Verilog is case sensitive. *

- [x] True
- [ ] False

What are the symbols used to represent digits in the binary number system? *

- [ ] 0,1,2
- [x] 0,1
- [ ] 1,2
- [ ] 0 through 8

Give the decimal value of binary 10010. *

- [ ] (6)10
- [ ] (9)10
- [x] (18)10
- [ ] (20)10

How is a J-K flip-flop made to toggle? *

- ○ J = 0, K = 0
- ◉ J = 1, K = 0
- ○ J = 0, K = 1
- ○ J = 1, K = 1

The number of digits in octal system is ..... *

- ○ 16
- ◉ 8
- ○ 10
- ○ 4

A full adder can be implemented using ..... *

- [x] two half adders
- [ ] two half adders and a OR gate
- [ ] two half adders and a NOT gate
- [ ] three half adders

The full form of HDL is *

- [ ] Higher Descriptive Language
- [ ] Higher Definition Language
- [x] Hardware Description Language
- [ ] High Descriptive Language

The full form of VHDL is *

- (●) VHSIC Hardware Description Language
- ( ) Verilog Hardware Description Language
- ( ) Variable Definition Language
- ( ) None of the Mentioned
- ( ) Other: _____

VHDL is being used for *

- ( ) Documentation
- ( ) Verification
- ( ) Synthesis of large digital design
- (●) All of the Mentioned
- ( ) Other: _____

VLSI: Very Large scale integration means *

- ( ) A few gates on a chip
- ( ) Hundreds of gates on a chip
- ( ) Thousands of gates on a chip
- (•) Twenty Thousands of gates to 10 X 106 transistors on a chip
- ( ) Other: .....

EDA Stands for *

- ( ) Electronic Development Application
- (•) Electronic Design automation
- ( ) Electric Design automation
- ( ) Electronic data Anaalysis
- ( ) Other: .....

Technically, the tool CAD refers to the backend tools that performs functions *

- ( ) Placing of the chip
- ( ) routing of the chip
- ( ) layout of the chip.
- (•) All the above
- ( ) Other: _____

The term Computer Aided Enginerring (CAE) tools refer to tools that are used for frontend such as *

- (•) HDL simulation, logic synthesis and timing analysis.
- ( ) HDL simulation, logic synthesis
- ( ) HDL simulation, logic synthesis and Placing and routing
- ( ) Placing ,routing and layout of the chip
- ( ) Other: _____

Verilog HDL – Verilog was introduced in 1983 by *

- ○ US. Dept. of Defense in 1983
- ◉ Gateway Design System Corporation
- ○ DARPA Defense Advanced Research project Agency.
- ○ None of the above
- ○ Other: .....

IEEE standard IEEE 1364-1995 is the original HDL standard In 1995 *

- ○ VHDL
- ◉ Verilog
- ○ Both VHDL and Verilog
- ○ Either VHDL or Verilog
- ○ Other: .....

IEEE standard IEEE 1076-1993 is the original HDL standard *

- (●) VHDL
- ( ) Verilog
- ( ) Both VHDL and Verilog
- ( ) Either VHDL or Verilog
- ( ) Other: .....

VHSIC stands for *

- (●) Very High Speed Integrated Circuits
- ( ) Very Higher Speed Integration Circuits
- ( ) Variable High Speed Integrated Circuits
- ( ) Variable Higher Speed Integration Circuits
- ( ) Other: .....

module template consists of *

- ( ) module
- ( ) endmodule
- ( ) module name and port list
- (•) all of the above

Simulation is process of *

- ( ) Writing a verilog Module
- (•) Imitating a real world object and verifying the design functionality
- ( ) converting a high-level description of design into an optimized gate-level representation
- ( ) All of the above

Instance created when *

- ( ) A Module is written using Verilog HDL
- (•) When stimulus block is written using Verilog HDL
- ( ) When a module is invoked in another module using an instance id
- ( ) None of the above

What is the output of the following code: initial clk =1'b0; always #100 clk = ~clk; *

- ( ) clk is initialized to '0'
- ( ) clk is a periodic signal with period of one cycle will be 200 time units
- (•) clk signal has 50% duty cylce
- ( ) All of the above

Select the highest and lowest level of abstractions *

- ( ) Behavioral abstraction, Dataflow abstraction respectively
- ( ) Gate abstraction, Behavioral abstraction respectively
- ( ) Switch level abstraction, Behavioral abstraction respectively
- (•) Behavioral abstraction, Switch level abstraction respectively

In top-down design methodology, top level block is divided into sub-blocks, further sub-blocks are divided until leaf cells are obtained *

- ( ) True
- (•) False

Answer any 2 from the following Questions. Each carry 10 marks. *

1. Explain the HDL based design flow with the help of flowchart.
2. Discuss the trends and popularity of the verilog HDL.
3. Explain the top-down design methodology by taking 4-bit Ripple carry counter as an example.
4. Write the design and stimulus blocks of 4-bit Ripple Carry counter.

vhdl iat 1 - AYUS...

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Sub: V-HDL

→ Q1) * HDL's are used for Simulation of System boards, Interconnect buses, FPGA and PAL's
* Verilog HDL is a IEEE Standard. In 1995, the Original standard IEEE 1364-1995 was approved.
* IEEE 1364-2001 is the latest Verilog HDL standards.

→ Typical Design Flow

1) Specification
2) Behavioural Description
3) RTL description
   → Functional Verification and Testing
   → Logical Synthesis
4) Gate level Netlist
   → Logical Verification and Testing
   → Automatic place & Route
5) physical Layout
   → Layout Verification
   → Implementation

Levels of Design — process in Design flow

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Accurate
Date _____ Page _____

-> Specification -> Requirements / Demands of Customers.

-> Behavioural Description: Architecture doesnot need to think about how they will implement this circuit.

* Behavioural Description is manually Converted into RTL Description in HDL.

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Q2) Trends in HDLs.

* The Speed and Complexity of digital circuits have increased rapidly.
* Designers have responded by designing at higher levels of abstraction.
* The most popular trend currently is to design in HDL at an RTL level, because logic Synthesis tools can create Gate level netlists from RTL level design.
* Today RTL design continues to be very popular.
* Formal Verification and assertion checking techniques have emerged.
* Behavioural Synthesis allowed engineers to design directly in terms of algorithms and the behaviour of the circuit.

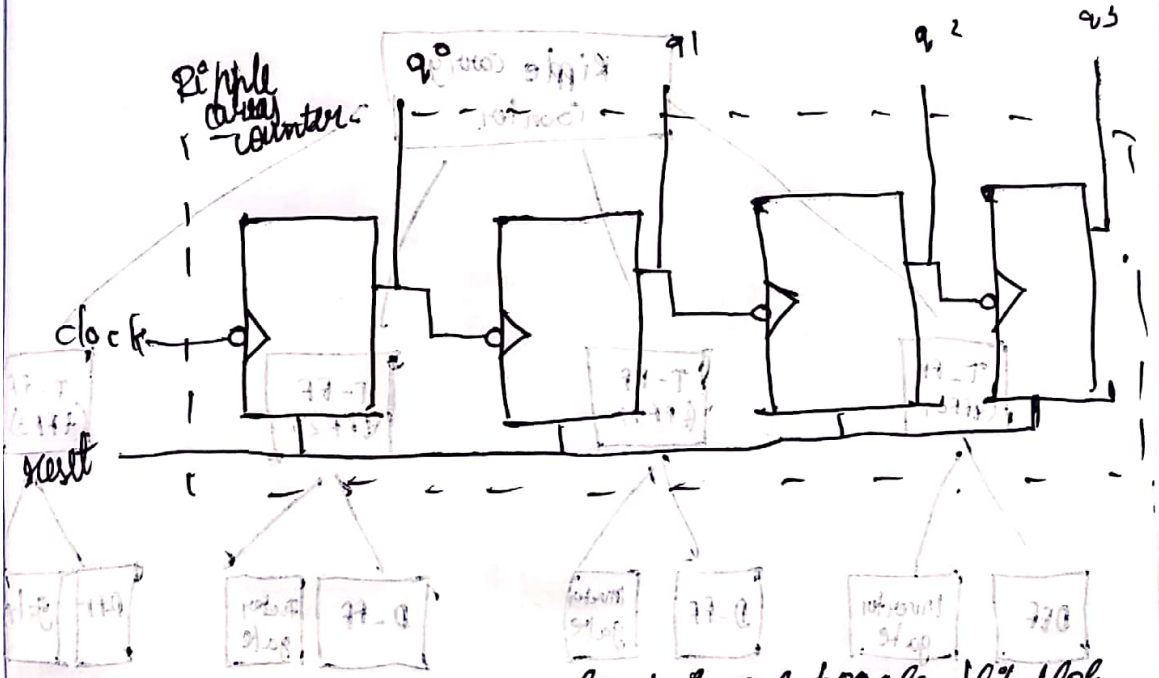
Popularity of Verilog HDL:

* Verilog HDL is General-purpose hardware description language that is easy to learn and easy to use.
* Verilog HDL allows different levels of abstraction to be mixed in the same model.
* Most popular logic Synthesis tools support Verilog HDL
* All fabrication vendors provide verilog HDL fiber libraries for post logic Synthesis Simulation.

Verilog HDL

4. Here top level module is 4-bit Ripple carry counter Ripple carry counter is constructed using T-flipflop Hence in the next level of hiracny it consists of only D-flip flops & an inverter. D flip flop can be implemented using gates like & inverter or it may be designed using only switches. If D-ff is implemented using only switches then D-ff is one of the leafcell. Inverter is implemented using switches

- The ripple carry counter shown in following



It is made up of (-)ve edge triggered toggle flip flop. Each of the T-FF can be made up from -ve edge triggered D-FF & inverters as shown in the following

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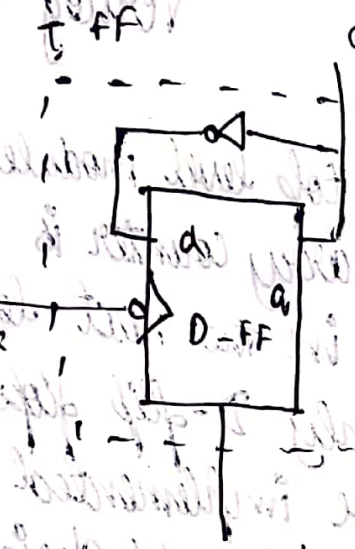
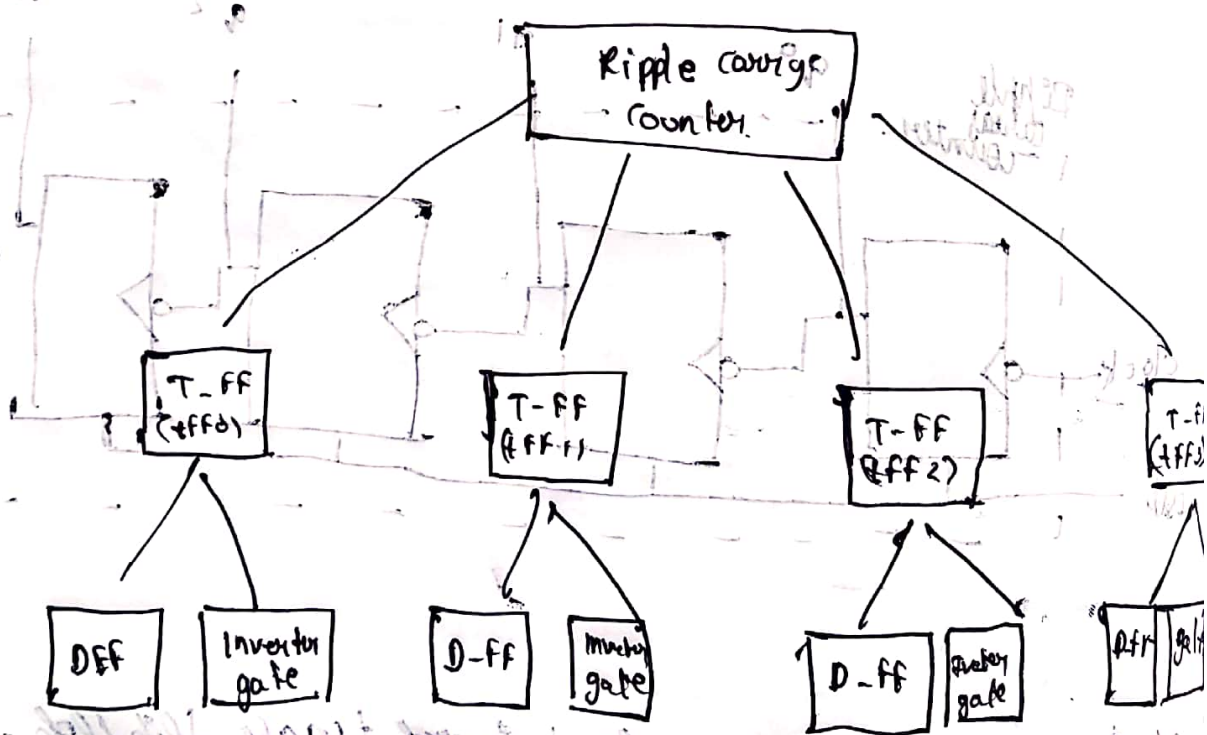
reset	q_n	q_{n+1}
1	1	0
0	0	0
0	1	0
0	0	0





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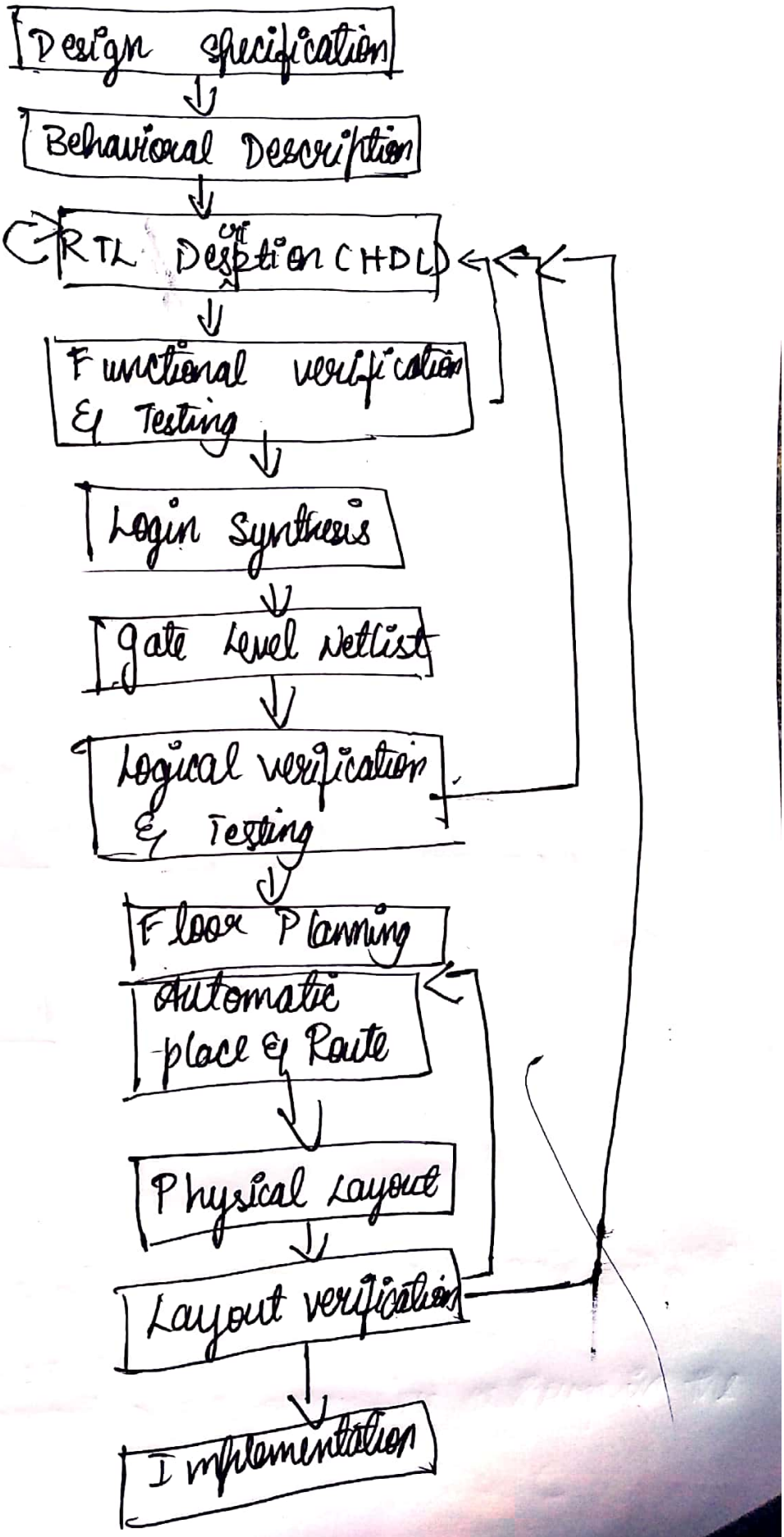
1. A typical design flow for designing VLSI IC circuits



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