

# CMOS VLSI DESIGN IAT-1 TCE

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Source and drain in nMOS device are isolated by

1 point

- single diode
- two diodes
- three diodes
- four diodes

In depletion mode MOS, source and drain are connected by

1 point

- insulating channel
- conducting channel
- Vdd
- Vss
- Option 5

MOS transistor structure is

1 point

- symmetrical
- non symmetrical
- semi symmetrical
- pseudo symmetrical

As source drain voltage increases, channel depth

1 point

- decreases
- increases
- logarithmically increases
- exponentially increases

Depletion mode MOSFETs are more commonly used as

1 point

- switches
- buffers
- resistors
- capacitors

Enhancement mode MOSFETs are more commonly used as

1 point

- switches
- resistors
- buffers
- Capacitors

Photoresist layer is formed using

1 point

- high sensitive polymer
- light sensitive polymer
- polysilicon
- silicon dioxide

CMOS inverter has \_\_\_\_\_ regions of operation

1 point

- three
- four
- two
- five

Increasing  $V_{sb}$ , the threshold voltage

1 point

- does not affect
- decreases
- increases
- exponentially increases

At threshold voltage ..... is created connecting source to drain

1 point

- Depletion layer
- Diffusion layer
- Polysilicon layer
- Inversion layer

At threshold voltage ..... is created connecting source to drain

1 point

- Depletion layer
- Diffusion layer
- Polysilicon layer
- Inversion layer

In saturation region, the current in n-channel MOSFET is ..... with increasing  $V_{ds}$

1 point

- Linearly increases
- Non linearly increases
- constant
- Others

nMOS pass transistor is

1 point

- Strong logic '1' transfer device
- Strong logic '0' transfer device
- Both Strong logic '1' and logic '0' transfer device
- Neither Strong logic '1' and logic '0' transfer device



pMOS pass transistor is

1 point

- Strong logic '1' transfer device
- Strong logic '0' transfer device
- Both Strong logic '1' and logic '0' transfer device
- Neither Strong logic '1' and logic '0' transfer device

Transmission gate is

1 point

- Strong logic '1' transfer device
- Strong logic '0' transfer device
- Both Strong logic '1' and logic '0' transfer device
- Neither Strong logic '1' and logic '0' transfer device

Current  $I_{ds}$  depends on

1 point

- Mobility of carriers
- Thickness of the gate oxide
- Channel length and width
- All of the above

## Untitled Section

NMOS transistors are fabricated on a

2 points

- N-type Silicon substrate
- Pure Silicon substrate
- P-type Silicon substrate
- None of the above

In n-well CMOS process

2 points

- N-type Silicon substrate is used
- Pure Silicon substrate is used
- P-type Silicon substrate is used
- None of the above

Diffusion regions are

2 points

- Moderately doped
- Lightly doped
- Not at all doped
- Heavily doped

Physical channel in depletion mode transistor is created using

2 points

- Diffusion process
- Oxidation process
- Ion Implantation process
- Metallization process

Masks are used to define

2 points

- Transistor area
- Patterning of PolySi
- Patterning of Metal
- All of the Above

Thinnox mask is used to define

2 points

- Transistor regions
- Patterning of PolySi
- Patterning of Metal
- All of the Above

Bipolar transistor has

2 points

- high input impedance
- High output drive current
- Scalable threshold voltage
- all

MOS structure is equivalent to

2 points

- Resistor
- Inductor
- Capacitor
- None of the above

The condition for non saturated region of nmos transistor is

2 points

- $V_{ds} = V_{gs} - V_t$
- $V_{gs}$  lesser than  $V_t$
- $V_{ds}$  lesser than  $V_{gs} - V_t$
- $V_{ds}$  greater than  $V_{gs} - V_t$

Enhancement mode device acts as \_\_\_\_\_ switch, depletion mode acts as \_\_\_\_\_ switch

2 points

- open, closed
- closed, open
- open, open
- close, close

What are the advantages of BiCMOS?

2 points

- higher gain
- high frequency characteristics
- better noise characteristics
- all of the above

Which type of CMOS circuits are good and better?

2 points

- p well
- n well
- twin tub
- all of the above

Velocity can be given as

2 points

- $\mu / V_{ds}$
- $\mu / E$
- $\mu * E$
- $E / \mu$



If  $V_{gs} = 3\text{v}$ ,  $V_{ds} = 5\text{v}$  and  $V_t = 1\text{v}$  then nMOS transistor is operating in

2 points

- Cut-off region
- Non-saturation region
- Saturation region
- None of the above

If  $V_{gs} = 3\text{v}$ ,  $V_{ds} = 1\text{v}$  and  $V_t = 1\text{v}$  then nMOS transistor is operating in

2 points

- Cut-off region
- Non-saturation region
- Saturation region
- None of the above

A fast circuit requires

1 point

- high gm
- low gm
- does not depend on gm
- low cost

If both the transistors in a CMOS Inverter are in saturation, then they act as

1 point

- current source
- voltage source
- divider
- buffer

The photoresist layer is exposed to

1 point

- visible light
- ultraviolet light
- infra-red light
- LED

Inversion layer in enhancement mode n-type consists of excess of

1 point

- positive carriers
- negative carriers
- both in equal quantity
- neutral carriers

This form was created inside of CMR Institute of Technology.

Google Forms